The TTL Data Book

for

Design Engineers

First Edition

TEXAS INSTRUMENTS

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General Information

A

THE TTL DATA BOOK

In this 640-page data book, Texas Instruments is pleased to present important technical information on the industry's broadest and most advanced family of TTL integrated circuits.

You'll find complete specifications on standard-technology TTL circuits (Series 54/74, Series 54H/74H, Series 54L/74L) and on TI's high-technology TTL families such as the Schottky-clamped† Series 54LS/74LS and Series 54S/74S, as well as radiation-hardened and beam-lead circuits. Also included are advanced technology TTL circuits consisting of high-performance random-access memories.

The indexes are designed for ease of circuit selection with margin tabs to guide you quickly to general circuit catagories, and the numerical and functional indexes will let you locate specific circuit types quickly. In addition, whenever practical, the MSI functions and the SSI pin assignment drawings are arranged in sequence by type number to further simplify the task of locating a particular function.

High-reliability TTL IC's are covered in a section devoted to the MACH IV Procurement Specification in accordance with MIL-M-38510, a program initiated by TI to ensure that quality and reliability are built into, not tested into, integrated circuits. Another section is devoted to JAN IC's and provides a table of recommended usage and cross-references from TI type-number-to-38510 slash sheet and 38510 slash sheet-to-TI type number.

Although this volume offers design and specification data only for TTL integrated circuits, complete technical data for any TI semiconductor/component product are available from your nearest TI field sales office, local authorized TI distributor, or by writing direct to: Marketing and Information Services, Texas Instruments Incorporated, P.O. Box 5012, MS 308, Dallas, Texas 75222.

We sincerely hope you will find the TTL Data Book for Design Engineers a meaningful addition to your technical library.

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

LETTER SYMBOLS, TERMS, AND DEFINITIONS

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical Commission (IEC) for international use. The definitions are grouped into sections applying to voltages, currents, switching characteristics, and classification of circuit complexity.

A

VOLTAGES

V_{IH} High-level input voltage

An input voltage level within the more positive (less negative) of the two ranges of values used to represent the binary variables. A minimum value is specified which is the least-positive (most-negative) value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Low-level input voltage

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables. A maximum value is specified which is the most-positive (least-negative) value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{T+} Positive-going threshold voltage

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} Negative-going threshold voltage

The voltage level at a transition-operated input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

V_{OH} High-level output voltage

The voltage at an output terminal for a specified output current I_{OH} with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} Low-level output voltage

The voltage at an output terminal for a specified output current I_{OL} with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ On-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ Off-state output voltage

The voltage at an output terminal for a specified output current with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

CURRENT

I_{IH} High-level input current

The current flowing into* an input when a specified high-level voltage is applied to that input.

I_{IL} Low-level input current

The current flowing into* an input when a specified low-level voltage is applied to that input.

I_{OH} High-level output current

The current flowing into* the output with a specified high-level output voltage V_{OH} applied.

Note: This parameter is usually specified for open-collector outputs intended to drive other logic circuits.

*Current flowing out of a terminal is a negative value.

CURRENTS (continued)

$I_{O(off)}$ Off-state output current
The current flowing into* an output with a specified output voltage applied and input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits or for three-state outputs.

I_{OS} Short-circuit output current
The current flowing into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CCH} Supply current, output(s) high
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} Supply current, output(s) low
The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

DYNAMIC CHARACTERISTICS

f_{max} Maximum clock frequency
The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause a change of output state with each clock pulse.

t_{HZ} Output disable time (of a three-state output) from high level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.

t_{LZ} Output disable time (of a three-state output) from low level
The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.

t_{PLH} Propagation delay time, low-to-high-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} Propagation delay time, high-to-low-level output
The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

t_{TLH} Transition time, low-to-high-level output
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} Transition time, high-to-low-level output
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

t_w Average pulse width
The time between 50-percent-amplitude points (or other specified reference points) on the leading and trailing edges of a pulse.

t_{hold} Hold time
The time interval for which a signal or pulse is retained at a specified input terminal after an active transition occurs at another specified input terminal.

*Current flowing out of a terminal is a negative value.

DYNAMIC CHARACTERISTICS (continued)

$t_{release}$ Release time

The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

t_{setup} Setup time

The time interval for which a signal is applied and maintained at a specified input terminal before an active transition occurs at another specified input terminal.

t_{ZH} Output enable time (of a three-state output) to high level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.

t_{ZL} Output enable time (of a three-state output) to low level

The time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY

Gate equivalent circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

LSI Large-scale integration

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether logical or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

MSI Medium-scale integration

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

SSI Small-scale integration

Integrated circuits of less complexity than medium-scale integration (MSI).

THERMAL INFORMATION

THERMAL RESISTANCE OF TTL CIRCUIT PACKAGES

PACKAGE	PINS	$R_{\theta JC}$ (°C/W) Junction-to-case thermal resistance		$R_{\theta JA}$ (°C/W) Junction-to-ambient thermal resistance	
		50% CONFIDENCE MAX VALUE	90% CONFIDENCE MAX VALUE	50% CONFIDENCE MAX VALUE	90% CONFIDENCE MAX VALUE
J ceramic dual-in-line	14	24	28	80	92
	16	22	26	73	85
	24	18	22	45	53
N plastic dual-in-line	14	35	41	85	97
	16	33	39	80	92
	24	28	34	57	66
T metal flat	14	60	80	109	129
W ceramic flat	14	51	60	110	126
	16	50	59	108	124
	24	44	52	74	86

Junction-to-case thermal resistance, $R_{\theta JC}$, is measured with the device immersed in a freon bath.
Junction-to-ambient thermal resistance, $R_{\theta JA}$, is measured in still air with the device soldered into a printed-circuit board.
Special test chips were used to obtain the above information.

A

Indexes

- Numerical
- Functional/Selection Guide
- Cross-Reference

B

B

NUMERICAL INDEX

NUMERICAL INDEX

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SN54110	SN74110	120	80
SN54111	SN74111	120	80
SN54LS112	SN74LS112	130	81
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†Redesignated SN29000
‡Redesignated SN29001

FUNCTIONAL INDEX/SELECTION GUIDE

The following sixteen pages contain functional indexes and selection guides designed to simplify the choice of a particular function to fit a specific application. Essential characteristics of similar or like functions are grouped for comparative analysis, and the electrical specifications are referenced by page number. The following catagories of functions are covered:

POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS

ELECTRICAL TABLES–PAGE 86

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PIN ASSIGNMENTS PAGE NO.
HEX INVERTERS	3 ns	19 mW	SN54S04	SN74S04	J, N, W	63
	6 ns	22 mW	SN54H04	SN74H04	J, N, W	
	9.5 ns	2 mW	SN54LS04	SN74LS04	J, N, W	
	10 ns	10 mW	SN5404	SN7404	J, N, W	
	33 ns	1 mW	SN54L04	SN74L04	J, N, T	
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S00	SN74S00	J, N, W	62
	6 ns	22 mW	SN54H00	SN74H00	J, N, W	
	9.5 ns	2 mW	SN54LS00	SN74LS00	J, N, W	
	10 ns	10 mW	SN5400	SN7400	J, N, W	
	33 ns	1 mW	SN54L00	SN74L00	J, N, T	
TRIPLE 3-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S10	SN74S10	J, N, W	64
	6 ns	22 mW	SN54H10	SN74H10	J, N, W	
	9.5 ns	2 mW	SN54LS10	SN74LS10	J, N, W	
	10 ns	10 mW	SN5410	SN7410	J, N, W	
	33 ns	1 mW	SN54L10	SN74L10	J, N, T	
DUAL 4-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S20	SN74S20	J, N, W	66
	6 ns	22 mW	SN54H20	SN74H20	J, N, W	
	9.5 ns	2 mW	SN54LS20	SN74LS20	J, N, W	
	10 ns	10 mW	SN5420	SN7420	J, N, W	
	33 ns	1 mW	SN54L20	SN74L20	J, N, T	
8-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S30	SN74S30	J, N, W	68
	6 ns	22 mW	SN54H30	SN74H30	J, N, W	
	17 ns	2 mW	SN54LS30	SN74LS30	J, N, W	
	10 ns	10 mW	SN5430	SN7430	J, N, W	
	33 ns	1 mW	SN54L30	SN74L30	J, N, T	
13-INPUT POSITIVE-NAND GATES	3 ns	19 mW	SN54S133	SN74S133	J, N, W	84

POSITIVE-NAND GATES AND INVERTERS WITH OPEN-COLLECTOR OUTPUTS

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DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PIN ASSIGNMENTS PAGE NO.
HEX INVERTERS	5 ns	17.5 mW	SN54S05	SN74S05	J, N, W	63
	8 ns	22 mW	SN54H05	SN74H05	J, N, W	
	16 ns	2 mW	SN54LS05	SN74LS05	J, N, W	
	22 ns	10 mW	SN5405	SN7405	J, N, W	
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	5 ns	17.5 mW	SN54S03	SN74S03	J, N, W	63
	8 ns	22 mW	SN54H01	SN74H01	J, N, W	62
	16 ns	2 mW	SN54LS01	SN74LS01	J, N, W	62
	16 ns	2 mW	SN54LS03	SN74LS03	J, N, W	63
	22 ns	10 mW	SN5401	SN7401	J, N, W	62
	22 ns	10 mW	SN5403	SN7403	J, N	63
	41 ns	1 mW	SN54L01	SN74L01	T	62
	41 ns	1 mW	SN54L03	SN74L03	J, N	63
TRIPLE 3-INPUT POSITIVE-NAND GATES	22 ns	10 mW	SN5412	SN7412	J, N, W	65
DUAL 4-INPUT POSITIVE-NAND GATES	5 ns	17.5 mW	SN54S22	SN74S22	J, N, W	67
	8 ns	22 mW	SN54H22	SN74H22	J, N, W	
	16 ns	2 mW	SN54LS22	SN74LS22	J, N, W	
	22 ns	10 mW	SN5422	SN7422	J, N, W	

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POSITIVE-NOR GATES WITH TOTEM-POLE OUTPUTS
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DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PIN ASSIGNMENTS PAGE NO.
QUADRUPLE 2-INPUT POSITIVE-NOR GATES	3.5 ns	29 mW	SN54S02	SN74S02	J, N, W	62
	10 ns	2.75 mW	SN54LS02	SN74LS02	J, N, W	
	10 ns	14 mW	SN5402	SN7402	J, N, W	
	33 ns	1.5 mW	SN54L02	SN74L02	J, N, T	
TRIPLE 3-INPUT POSITIVE-NOR GATES	8.5 ns	22 mW	SN5427	SN7427	J, N, W	68
	10 ns	4.5 mW	SN54LS27	SN74LS27	J, N, W	
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE	10.5 ns	23 mW	SN5425	SN7425	J, N, W	67
DUAL 5-INPUT POSITIVE-NOR GATES	3.5 ns	29 mW	SN54S260	SN74S260	J, N, W	84

POSITIVE-AND GATES WITH TOTEM-POLE OUTPUTS
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DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PIN ASSIGNMENTS PAGE NO.
QUADRUPLE 2-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	SN54LS08	SN74LS08	J, N, W	64
	15 ns	19 mW	SN5408	SN7408	J, N, W	
TRIPLE 3-INPUT POSITIVE-AND GATES	4.75 ns	31 mW	SN54S11	SN74S11	J, N, W	65
	8.2 ns	40 mW	SN54H11	SN74H11	J, N, W	
	12 ns	4.25 mW	SN54LS11	SN74LS11	J, N, W	
DUAL 4-INPUT POSITIVE-AND GATES	8.2 ns	40 mW	SN54H21	SN74H21	J, N, W	67
	12 ns	4.25 mW	SN54LS21	SN74LS21	J, N, W	

POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS
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DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PIN ASSIGNMENTS PAGE NO.
QUADRUPLE 2-INPUT POSITIVE-AND GATES	18.5 ns	19.4 mW	SN5409	SN7409	J, N, W	64
	20 ns	4.25 mW	SN54LS09	SN74LS09	J, N, W	
TRIPLE 3-INPUT POSITIVE-AND GATES	6 ns	28 mW	SN54S15	SN74S15	J, N, W	66
	10.5 ns	38 mW	SN54H15	SN74H15	J, N, W	
	20 ns	4.25 mW	SN54LS15	SN74LS15	J, N, W	

SCHMITT-TRIGGER POSITIVE-NAND GATES AND INVERTERS WITH TOTEM-POLE OUTPUTS
ELECTRICAL TABLES—PAGE 98

DESCRIPTION	TYPICAL HYSTERESIS	TYPICAL DELAY TIME	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PIN ASSIGNMENTS PAGE NO.
HEX SCHMITT TRIGGER INVERTERS	0.8 V	15 ns	SN5414	SN7414	J, N, W	65
QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS	0.55 V	8 ns	SN54S132	SN74S132	J, N, W	83
	0.8 V	15 ns	SN54132	SN74132	J, N, W	
DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS	0.8 V	16.5 ns	SN5413	SN7413	J, N, W	65

BUFFERS/CLOCK DRIVERS WITH TOTEM-POLE OUTPUTS

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DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP POWER PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
					−55°C to 125°C	0°C to 70°C		
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	48 mA	−2.4 mA	7 ns	28 mW	SN5428	SN7428	J, N, W	68
	24 mA	−1.2 mA	12 ns	5.5 mW		SN74LS28	J, N, W	
	12 mA	−1.2 mA	12 ns	5.5 mW	SN54LS28		J, N, W	
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	48 mA	−1.2 mA	10.5 ns	27 mW	SN5437	SN7437	J, N, W	69
	24 mA	−1.2 mA	12 ns	4.3 mW		SN74LS37	J, N, W	
	12 mA	−1.2 mA	12 ns	4.3 mW	SN54LS37		J, N, W	
DUAL 4-INPUT POSITIVE-NAND BUFFERS	60 mA	−3 mA	4 ns	21 mW	SN54S40	SN74S40	J, N, W	70
	60 mA	−1.5 mA	7.5 ns	44 mW	SN54H40	SN74H40	J, N, W	
	48 mA	−1.2 mA	10.5 ns	26 mW	SN5440	SN7440	J, N, W	
	24 mA	−1.2 mA	12 ns	4.3 mW		SN74LS40	J, N, W	
	12 mA	−1.2 mA	12 ns	4.3 mW	SN54LS40		J, N, W	

50-OHM/75-OHM LINE DRIVERS

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DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP POWER PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
					−55°C to 125°C	0°C to 70°C		
QUADRUPLE 2-INPUT POSITIVE-NOR LINE DRIVERS	60 mA	−40 mA	4 ns	22 mW	SN54S140	SN74S140	J, N, W	84
DUAL 4-INPUT POSITIVE-NAND LINE DRIVERS	48 mA	−42.4 mA	7 ns	28 mW		SN74128	J, N, W	83
	48 mA	−29 mA	7 ns	28 mW	SN54128		J, N, W	

BUFFER AND INTERFACE GATES WITH OPEN-COLLECTOR OUTPUTS

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DESCRIPTION	HIGH-LEVEL OUTPUT VOLTAGE	LOW-LEVEL OUTPUT CURRENT	TYPICAL DELAY TIME	TYP POWER PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
					−55°C to 125°C	0°C to 70°C		
HEX BUFFERS/DRIVERS	30 V	40 mA	13 ns	21 mW		SN7407	J, N, W	64
	30 V	30 mA	13 ns	21 mW	SN5407		J, N, W	64
	15 V	40 mA	13 ns	21 mW		SN7417	J, N, W	66
	15 V	30 mA	13 ns	21 mW	SN5417		J, N, W	66
HEX INVERTER BUFFERS/DRIVERS	30 V	40 mA	12.5 ns	26 mW		SN7406	J, N, W	63
	30 V	30 mA	12.5 ns	26 mW	SN5406		J, N, W	63
	15 V	40 mA	12.5 ns	26 mW		SN7416	J, N, W	66
	15 V	30 mA	12.5 ns	26 mW	SN5416		J, N, W	66
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	15 V	16 mA	13.5 ns	10 mW	SN5426	SN7426	J, N	68
	5.5 V	48 mA	12.5 ns	24.4 mW	SN5438	SN7438	J, N, W	69
	5.5 V	24 mA	19 ns	4.3 mW		SN74LS38	J, N, W	69
	5.5 V	12 mA	19 ns	4.3 mW	SN54LS38		J, N, W	69
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	5.5 V	48 mA	11 ns	28 mW	SN5433	SN7433	J, N, W	69
	5.5 V	24 mA	19 ns	5.45 mW		SN74LS33	J, N, W	69
	5.5 V	12 mA	19 ns	5.45 mW	SN54LS33		J, N, W	69

B

B

POSITIVE-OR GATES WITH TOTEM-POLE OUTPUTS

ELECTRICAL TABLES—PAGE 108

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
			−55°C to 125°C	0°C to 70°C		
QUADRUPLE 2-INPUT POSITIVE-OR GATES	12 ns	24 mW	SN5432	SN7432	J, N, W	69
	12 ns	5 mW	SN54LS32	SN74LS32	J, N, W	

AND-OR-INVERT GATES WITH TOTEM-POLE OUTPUTS

ELECTRICAL TABLES—PAGE 110

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
			−55°C to 125°C	0°C to 70°C		
2-WIDE 4-INPUT	12.5 ns	2.75 mW	SN54LS55	SN74LS55	J, N, W	73
	43 ns	1.5 mW	SN54L55	SN74L55	J, N, T	
4-WIDE 4-2-3-2-INPUT	3.5 ns	29 mW	SN54S64	SN74S64	J, N, W	74
4-WIDE 2-2-3-2-INPUT	6.6 ns	41 mW	SN54H54	SN74H54	J, N, W	72
4-WIDE 2-INPUT	10.5 ns	23 mW	SN5454	SN7454	J, N, W	72
4-WIDE 2-3-3-2-INPUT	12.5 ns	4.5 mW	SN54LS54	SN74LS54	J, N, W	72
4-WIDE 2-3-3-2-INPUT	43 ns	1.5 mW	SN54L54	SN74L54	J, N, T	72
DUAL 2-WIDE 2-INPUT	3.5 ns	28 mW	SN54S51	SN74S51	J, N, W	70
	6.5 ns	29 mW	SN54H51	SN74H51	J, N, W	
	10.5 ns	14 mW	SN5451	SN7451	J, N, W	
	12.5 ns	2.75 mW	SN54LS51	SN74LS51	J, N, W	
	43 ns	1.5 mW	SN54L51	SN74L51	J, N, T	

AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

ELECTRICAL TABLES—PAGE 112

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
			−55°C to 125°C	0°C to 70°C		
4-WIDE 4-2-3-2-INPUT	5.5 ns	36 mW	SN54S65	SN74S65	J, N, W	74

EXPANDABLE GATES

ELECTRICAL TABLES—PAGE 113

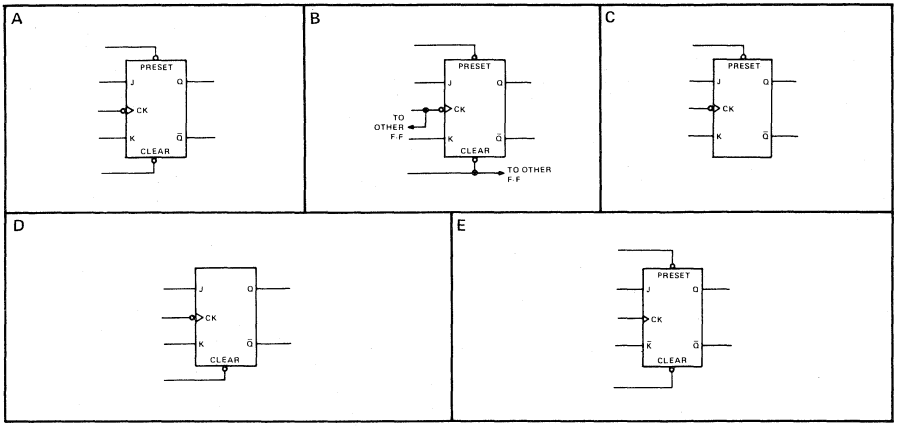
DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
			−55°C to 125°C	0°C to 70°C		
DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE	10.5 ns	23 mW	SN5423	SN7423	J, N, W	67
4-WIDE AND-OR GATES	9.9 ns	88 mW	SN54H52	SN74H52	J, N, W	71
4-WIDE AND-OR-INVERT GATES	6.6 ns	41 mW	SN54H53	SN74H53	J, N, W	71
	10.5 ns	23 mW	SN5453	SN7453	J, N, W	
2-WIDE AND-OR-INVERT GATES	6.8 ns	30 mW	SN54H55	SN74H55	J, N, W	73
DUAL 2-WIDE AND-OR-INVERT GATES	6.5 ns	29 mW	SN54H50	SN74H50	J, N, W	70
	10.5 ns	14 mW	SN5450	SN7450	J, N, W	

EXPANDERS

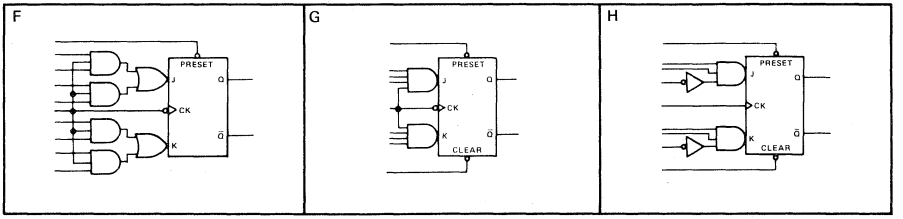
ELECTRICAL TABLES—PAGE 117

DESCRIPTION	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
		−55°C to 125°C	0°C to 70°C		
DUAL 4-INPUT EXPANDERS	4 mW	SN5460	SN7460	J, N, W	73
	6 mW	SN54H60	SN74H60	J, N, W	
TRIPLE 3-INPUT EXPANDERS	13 mW	SN54H61	SN74H61	J, N, W	73
3-2-2-3-INPUT AND-OR EXPANDERS	25 mW	SN54H62	SN74H62	J, N, W	74

DUAL J-K EDGE-TRIGGERED FLIP-FLOPS



SINGLE J-K EDGE-TRIGGERED FLIP-FLOPS



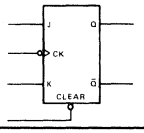
DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		TEMPERATURE RANGE		PACKAGES	PAGE REFERENCES	
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	−55°C to 125°C	0°C to 70°C		PIN ASSIGNMENTS	ELECTRICAL
A	125	75	6↓	0↓	SN54S112	SN74S112	J, N, W	81	132
	50	100	13↓	0↓	SN54H106	SN74H106	J, N, W	79	126
	45	10	20↓	0↓	SN54LS76	SN74LS76	J, N, W	77	130
	45	10	20↓	0↓	SN54LS112	SN74LS112	J, N, W	81	130
B	125	75	6↓	0↓	SN54S114	SN74S114	J, N, W	81	132
	50	100	13↓	0↓	SN54H108	SN74H108	J, N, W	79	126
	45	10	20↓	0↓	SN54LS78	SN74LS78	J, N, W	77	130
	45	10	20↓	0↓	SN54LS114	SN74LS114	J, N, W	81	130
C	125	75	6↓	0↓	SN54S113	SN74S113	J, N, W	81	132
	45	10	20↓	0↓	SN54LS113	SN74LS113	J, N, W	81	130
D	50	100	13↓	0↓	SN54H103	SN74H103	J, N, W	78	126
	45	10	20↓	0↓	SN54LS73	SN74LS73	J, N, W	76	130
E	33	10	20↑	5↑	SN54LS109	SN74LS109	J, N, W	80	130
	33	45	10↑	6↑	SN54109	SN74109	J, N, W	80	120
F	50	100	13↓	0↓	SN54H101	SN74H101	J, N, W	78	126
G	50	100	13↓	0↓	SN54H102	SN74H102	J, N, W	78	126
H	35	65	20↑	0↑	SN5470	SN7470	J, N, W	75	120

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

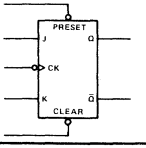
B

DUAL PULSE-TRIGGERED FLIP-FLOPS

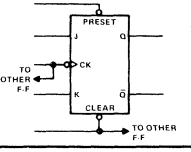
I



J

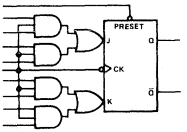


K

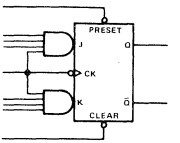


SINGLE PULSE-TRIGGERED FLIP-FLOPS

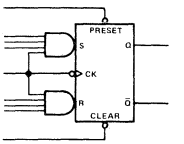
L



M



N

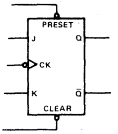


DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		TEMPERATURE RANGE		PACKAGES	PAGE REFERENCES	
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	−55°C to 125°C	0°C to 70°C		PIN ASSIGNMENTS	ELECTRICAL
I	30	80	0↑	0↓	SN54H73	SN74H73	J, N, W	76	124
	20	50	0↑	0↓	SN5473	SN7473	J, N, W	76	120
	20	50	0↑	0↓	SN54107	SN74107	J, N	79	120
	3	3.8	0↑	0↓	SN54L73	SN74L73	J, N, T	76	128
J	30	80	0↑	0↓	SN54H76	SN74H76	J, N, W	77	124
	20	50	0↑	0↓	SN5476	SN7476	J, N, W	77	120
K	30	80	0↑	0↓	SN54H78	SN74H78	J, N, W	77	124
	3	3.8	0↑	0↓	SN54L78	SN74L78	J, N, T	77	128
L	30	80	0↑	0↓	SN54H71	SN74H71	J, N, W	75	124
M	30	80	0↑	0↓	SN54H72	SN74H72	J, N, W	76	124
	20	50	0↑	0↓	SN5472	SN7472	J, N, W	76	120
	3	3.8	0↑	0↓	SN54L72	SN74L72	J, N, T	76	128
N	3	3.8	0↑	0↓	SN54L71	SN74L71	J, N, T	75	128

J-K FLIP-FLOPS WITH DATA LOCKOUT

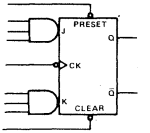
DUAL

O



SINGLE

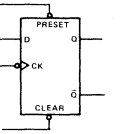
P



D-TYPE FLIP-FLOPS

DUAL

Q



DWG. REF.	TYPICAL CHARACTERISTICS		DATA TIMES		TEMPERATURE RANGE		PACKAGES	PAGE REFERENCES	
	f_{max} (MHz)	Pwr/F-F (mW)	SETUP (ns)	HOLD (ns)	−55°C to 125°C	0°C to 70°C		PIN ASSIGNMENTS	ELECTRICAL
O	25	70	0↑	30	SN54111	SN74111	J, N, W	80	120
P	25	100	20↑	5↑	SN54110	SN74110	J, N, W	80	120
Q	110	75	3↑	2↑	SN54S74	SN74S74	J, N, W	76	132
	43	75	15↑	5↑	SN54H74	SN74H74	J, N, W	76	124
	33	10	25↑	5↑	SN54LS74	SN74LS74	J, N, W	76	130
	25	43	20↑	5↑	SN5474	SN7474	J, N, W	76	120
	3	4	50↑	0↑	SN54L74	SN74L74	J, N, T	76	128

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

MONOSTABLE MULTIVIBRATORS WITH SCHMITT-TRIGGER INPUTS
ELECTRICAL TABLES–PAGE 134

DESCRIPTION	NO. OF INPUTS		OUTPUT PULSE RANGE	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
	POSITIVE	NEGATIVE			–55°C to 125°C	0°C to 70°C		
SINGLE	1	2	40 ns–28 s	90 mW	SN54121	SN74121	J, N, W	82
	1	2	40 ns–28 s	40 mW	SN54L121	SN74L121	J, N, T	

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS
ELECTRICAL TABLES–PAGE 138

DESCRIPTION	NO. OF INPUTS		DIRECT CLEAR	OUTPUT PULSE RANGE	TYP TOTAL POWER	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
	POSITIVE	NEGATIVE				–55°C to 125°C	0°C to 70°C		
SINGLE	2	2	Yes	45 ns–∞	115 mW	SN54122	SN74122	J, N, W	82
	2	2	Yes	90 ns–∞	55 mW	SN54L122	SN74L122	J, N, T	
DUAL	1	1	Yes	45 ns–∞	230 mW	SN54123	SN74123	J, N, W	82
	1	1	Yes	90 ns–∞	115 mW	SN54L123	SN74L123	J, N	

$\overline{S}$-$\overline{R}$ LATCHES
ELECTRICAL TABLES–PAGE 141

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
			–55°C to 125°C	0°C to 70°C		
QUADRUPLE $\overline{S}$-$\overline{R}$ LATCHES	12 ns	90 mW	SN54279	SN74279	J, N, W	85

GATES WITH 3-STATE TOTEM-POLE OUTPUTS
ELECTRICAL TABLES–PAGE 142

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PACKAGES	PIN ASSIGNMENTS PAGE NO.
			–55°C to 125°C	0°C to 70°C		
QUADRUPLE BUS BUFFERS	10 ns	40 mW	SN54125	SN74125	J, N, W	83
	10 ns	45 mW	SN54126	SN74126	J, N, W	
12-INPUT POSITIVE-NAND GATES	4.5 ns	45 mW	SN54S134	SN74S134	J, N, W	84

B

ADDERS

DESCRIPTION	TYPICAL CARRY TIME	TYPICAL ADD TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
SINGLE 1-BIT GATED FULL ADDERS	10.5 ns	52 ns	105 mW	SN5480	SN7480	J, N, W	187
SINGLE 2-BIT FULL ADDERS	14.5 ns	25 ns	87 mW	SN5482	SN7482	J, N, W	195
SINGLE 4-BIT FULL ADDERS	10 ns	16 ns	76 mW	SN5483A	SN7483A	J, N, W	198
	10 ns	16 ns	76 mW	SN54283	SN74283	J, N, W	494
	50 ns	33 ns	19 mW	SN54LS83	SN74LS83	J, N, W	198
DUAL 1-BIT CARRY-SAVE FULL ADDERS	11 ns	11 ns	110 mW	SN54H183	SN74H183	J, N, W	396
4-BIT ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS	7 ns	11 ns	600 mW	SN54S181	SN74S181	J, N†, W	381
	12.5 ns	24 ns	455 mW	SN54181	SN74181	J, N, W	
	16 ns	24 ns	102 mW	SN54LS181	SN74LS181	J, N, W	
LOOK-AHEAD CARRY GENERATORS	7 ns		260 mW	SN54S182	SN74S182	J, N, W	392
	13 ns		180 mW	SN54182	SN74182	J, N, W	

MULTIPLIERS

DESCRIPTION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS (8-BIT PRODUCT IN 40 ns TYPICAL)	SN54284, SN54285	SN74284, SN74285	J, N, W	496
25-MHz 6-BIT-BINARY RATE MULTIPLIERS	SN5497	SN7497	J, N†, W	248
25-MHz DECADE RATE MULTIPLIERS	SN54167	SN74167	J, N, W	347

COMPARATORS

DESCRIPTION	TYPICAL COMPARE TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
4-BIT MAGNITUDE COMPARATORS	11.5 ns	365 mW	SN54S85	SN74S85	J, N, W	202
	21 ns	275 mW	SN5485	SN7485	J, N, W	
	82 ns	20 mW	SN54L85	SN74L85	J, N	

PARITY GENERATORS/CHECKERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	13 ns	335 mW	SN54S280	SN74S280	J, N, W	491
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	35 ns	170 mW	SN54180	SN74180	J, N, W	379

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH TOTEM-POLE OUTPUTS	7 ns	250 mW	SN54S86	SN74S86	J, N, W	209
	10 ns	30 mW	SN54LS86	SN74LS86	J, N, W	
	14 ns	150 mW	SN5486	SN7486	J, N, W	
	55 ns	15 mW	SN54L86	SN74L86	J, N, T	
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS	18 ns	30 mW	SN54LS136	SN74LS136	J, N, W	271
	27 ns	150 mW	SN54136	SN74136	J, N, W	
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES	18 ns	40 mW	SN54LS266	SN74LS266	J, N, W	486
QUADRUPLE EXCLUSIVE OR/NOR GATES	8 ns	325 mW	SN54S135	SN74S135	J, N, W	269
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT	14 ns	270 mW	SN54H87	SN74H87	J, N, W	214

†SN54S181, SN5497 not available in the N package.

SHIFT REGISTERS

DESCRIPTION	NO OF BITS	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	MODES S-R‡	MODES S-L‡	MODES LOAD	MODES HOLD	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
PARALLEL-IN, PARALLEL-OUT (BIDIRECTIONAL)	8	25 MHz	D	Low	X	X	X	X	360 mW	SN54198	SN74198	J, N, W	456
	4	70 MHz	D	Low	X	X	X	X	450 mW	SN54S194	SN74S194	J, N, W	437
		25 MHz	D	Low	X	X	X	X	195 mW	SN54194	SN74194	J, N, W	437
		20 MHz	D	Low	X	X	X	X	60 mW	SN54LS194	SN74LS194	J, N, W	437
PARALLEL-IN, PARALLEL-OUT	8	25 MHz	J-$\overline{K}$	Low	X		X	X	360 mW	SN54199	SN74199	J, N, W	456
	5	10 MHz	D	Low	X		X		240 mW	SN5496	SN7496	J, N, W	243
		5 MHz	D	Low	X		X		120 mW	SN54L96	SN74L96	J, N	243
	4	70 MHz	J-$\overline{K}$	Low	X		X		375 mW	SN54S195	SN74S195	J, N, W	444
		30 MHz	J-$\overline{K}$	Low	X		X		195 mW	SN54195	SN74195	J, N, W	444
		25 MHz	D	None	X		X		195 mW	SN5495A	SN7495A	J, N, W	237
		25 MHz	D	Low	X		X	X	230 mW	SN54179	SN74179	J, N, W	375
		25 MHz	D	None	X		X	X	230 mW	SN54178	SN74178	J, N, W	375
		20 MHz	J-$\overline{K}$	Low	X		X		50 mW	SN54LS195	SN74LS195	J, N, W	444
		20 MHz	D	None	X		X		50 mW	SN54LS95A	SN74LS95A	J, N, W	237
		20 MHz	D	None	X		X		62 mW	SN54LS295	SN74LS295	J, N, W	502
		3 MHz	J-$\overline{K}$	None	X		X		19 mW	SN54L99	SN74L99	J, N	255
		3 MHz	D	None	X		X		19 mW	SN54L95	SN74L95	J, N, T	237
SERIAL-IN, PARALLEL-OUT	8	25 MHz	Gated D	Low	X				167 mW	SN54164	SN74164	J, N, W	334
		12 MHz	Gated D	Low	X				84 mW	SN54L164	SN74L164	J, N, T	334
PARALLEL-IN, SERIAL-OUT	8	25 MHz	D	None	X		X	X	210 mW	SN54165	SN74165	J, N, W	339
		20 MHz	D	Low	X		X	X	360 mW	SN54166	SN74166	J, N, W	343
	4	10 MHz	D	High	X		X		175 mW	SN5494	SN7494	J, N, W	234
SERIAL-IN, SERIAL-OUT	8	10 MHz	Gated D	None	X				175 mW	SN5491A	SN7491A	J, N, W	230
		3 MHz	Gated D	None	X				17.5 mW	SN54L91	SN74L91	J, N, T	230

‡S-R ≡ shift right, S-L ≡ shift left

REGISTER FILES

DESCRIPTION	TYPICAL ADDRESS TIME	TYP READ ENABLE TIME	DATA INPUT RATE	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
EIGHT WORDS OF TWO BITS	33 ns	15 ns	20 MHz	560 mW		SN74172	J, N	356
FOUR WORDS OF FOUR BITS	30 ns	15 ns	20 MHz	635 mW	SN54170	SN74170	J, N†, W	351

OTHER REGISTERS

DESCRIPTION	FREQ	ASYNC CLEAR	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
HEX D-TYPE REGISTERS	75 MHz	Low	450 mW	SN54S174	SN74S174	J, N†, W	363
	30 MHz	Low	65 mW	SN54LS174	SN74LS174	J, N, W	363
	25 MHz	Low	225 mW	SN54174	SN74174	J, N, W	363
QUADRUPLE D-TYPE REGISTERS	75 MHz	Low	300 mW	SN54S175	SN74S175	J, N, W	363
	30 MHz	Low	45 mW	SN54LS175	SN74LS175	J, N, W	363
	25 MHz	Low	150 mW	SN54175	SN74175	J, N, W	363
QUADRUPLE MULTIPLEXERS WITH STORAGE	25 MHz	None	195 mW	SN54298	SN74298	J, N, W	505
	3 MHz	None	25 mW	SN54L98	SN74L98	J, N	253
QUADRUPLE BUS-BUFFER REGISTERS	25 MHz	High	250 mW	SN54173	SN74173	J, N, W	360

PULSE SYNCHRONIZERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE −55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
DUAL 30-MHz PULSE SYNCHRONIZERS/DRIVERS	16 ns	255 mW	SN54120	SN74120	J, N, W	264

†SN54170, SN54S174 not available in the N package.

B

LATCHES

DESCRIPTION	NO. OF BITS	CLEAR	OUTPUTS	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
D_G (CLOCKED) LATCHES	8	Low	Q	11 ns	250 mW	SN54116	SN74116	J, N, W	261
		None	Q	15 ns	320 mW	SN54100	SN74100	J, N, W	259
	4	None	Q, $\overline{Q}$	15 ns	160 mW	SN5475	SN7475	J, N, W	182
		None	Q	15 ns	160 mW	SN5477	SN7477	W	182
		None	Q, $\overline{Q}$	30 ns	80 mW	SN54L75	SN74L75	J, N	182
		None	Q	30 ns	80 mW	SN54L77	SN74L77	T	182
$\overline{S}$-$\overline{R}$ Latches (SSI)	4	None	Q	12 ns	90 mW	SN54279	SN74279	J, N, W	85

READ-ONLY MEMORIES (ROM's, PROM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPICAL ADDRESS TIME	TYPICAL ENABLE TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
1024-BIT ROM	256 X 4	O-C	40 ns	20 ns	0.46 mW	SN54187	SN74187	J, N†, W	410
512-BIT PROM	64 X 8	O-C	50 ns	47 ns	0.6 mW	SN54186	SN74186	J, N, W	404
256-BIT PROM	32 X 8	O-C	29 ns	28 ns	1.3 mW		SN74188A	J, N	414
256-BIT ROM	32 X 8	O-C	26 ns	22 ns	1.1 mW	SN5488A	SN7488A	J, N, W	216

READ/WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPICAL ADDRESS TIME	TYPICAL ENABLE TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
256-BIT	256 X 1	3-State	30 ns	9 ns	1.7 mW	SN54S200	SN74S200	J, N, W	466
READ/WRITE	256 X 1	3-State	42 ns	17 ns	1.8 mW		SN74200	J, N	463
MEMORY	256 X 1	O-C	32 ns	17 ns	1.7 mW	SN54S206	SN74S206	J, N, W	470
64-BIT READ/WIRTE MEMORY	16 X 4	O-C	32 ns	30 ns	5.9 mW		SN7489	J, N, W	220
16-BIT READ/WRITE	16 X 1	O-C	15 ns	15 ns	14 mW	SN5481A	SN7481A	J, N, W	190
MEMORY	16 X 1	O-C	15 ns	15 ns	14 mW	SN5484A	SN7484A	J, N, W	190
16-BIT MULTIPLE-PORT REGISTER FILE	8 X 2	3-State	33 ns	15 ns	35 mW		SN74172	J, N	356
16-BIT REGISTER FILE	4 X 4	O-C	30 ns	15 ns	40 mW	SN54170	SN74170	J, N†, W	351

CODE CONVERTERS

DESCRIPTION	TYPICAL DELAY TIME PER PACKAGE LEVEL	TYPICAL TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
6-LINE-BCD TO 6-LINE BINARY, OR 4-LINE TO 4-LINE BCD 9's/BCD 10's CONVERTERS	25 ns	280 mW	SN54184	SN74184	J, N, W	398
6-BIT-BINARY TO 6-BIT-BCD CONVERTERS	25 ns	280 mW	SN54185A	SN74185A	J, N, W	398

†SN54187, SN54170 not available in the N package.

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL DELAY TIMES: DATA TO INV OUTPUT	TYPICAL DELAY TIMES: DATA TO NON-INV OUTPUT	TYPICAL DELAY TIMES: FROM ENABLE	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE: −55°C to 125°C	TEMPERATURE RANGE: 0°C to 70°C	PACKAGES	PAGE NO.
16-LINE-TO-1-LINE	2-state	11 ns		18 ns	200 mW	SN54150	SN74150	J, N, W	294
8-LINE-TO-1-LINE	3-state	4.5 ns	8 ns	14 ns	275 mW	SN54S251	SN74S251	J, N, W	473
	3-state	17 ns	21 ns	21 ns	250 mW	SN54251	SN74251	J, N, W	473
	3-state	17 ns	21 ns	21 ns	35 mW	SN54LS251	SN74LS251	J, N, W	473
	2-state	4.5 ns	8 ns	9 ns	225 mW	SN54S151	SN74S151	J, N, W	294
	2-state	8 ns	16 ns	22 ns	145 mW	SN54151A	SN74151A	J, N, W	294
	2-state	8 ns			130 mW	SN54152A	SN74152A	W	294
	2-state	11 ns	18 ns	27 ns	30 mW	SN54LS151	SN74LS151	J, N, W	294
	2-state	11 ns		18 ns	28 mW	SN54LS152	SN74LS152	W	294
DUAL 4-LINE-TO-1-LINE	3-state		12 ns	16 ns	35 mW	SN54LS253	SN74LS253	J, N, W	480
	2-state		6 ns	9.5 ns	225 mW	SN54S153	SN74S153	J, N, W	302
	2-state		14 ns	17 ns	180 mW	SN54153	SN74153	J, N, W	302
	2-state		14 ns	17 ns	31 mW	SN54LS153	SN74LS153	J, N, W	302
	2-state		27 ns	34 ns	90 mW	SN54L153	SN74L153	J, N	302
QUADRUPLE 2-LINE-TO-1-LINE WITH STORAGE	2-state		20 ns from clock		195 mW	SN54298	SN74298	J, N, W	505
QUADRUPLE 2-LINE-TO-1-LINE	3-state	4 ns		14 ns	280 mW	SN54S258	SN74S258	J, N, W	483
	3-state		5 ns	14 ns	320 mW	SN54S257	SN74S257	J, N, W	483
	2-state	4 ns		7 ns	195 mW	SN54S158	SN74S158	J, N, W	317
	2-state		5 ns	8 ns	250 mW	SN54S157	SN74S157	J, N, W	317
	2-state		9 ns	14 ns	150 mW	SN54157	SN74157	J, N, W	317
	2-state		18 ns	27 ns	75 mW	SN54L157	SN74L157	J, N	317

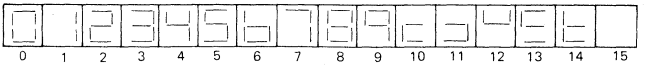
DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL SELECT TIME	TYPICAL ENABLE TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE: −55°C to 125°C	TEMPERATURE RANGE: 0°C to 70°C	PACKAGES	PAGE NO.
4-LINE-TO-16-LINE	Totem-Pole	23 ns	19 ns	170 mW	SN54154	SN74154	J, N, W	308
	Totem-Pole	46 ns	38 ns	85 mW	SN54L154	SN74L154	J, N	308
	Open-Collector	24 ns	19 ns	170 mW	SN54159	SN74159	J, N, W	323
4-LINE-TO-10-LINE, BCD-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5442A	SN7442A	J, N, W	167
	Totem-Pole	34 ns		70 mW	SN54L42	SN74L42	J, N	167
4-LINE-TO-10-LINE, EXCESS-3-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5443A	SN7443A	J, N, W	167
	Totem-Pole	34 ns		70 mW	SN54L43	SN74L43	J, N	167
4-LINE-TO-10-LINE EXCESS-3-GRAY-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5444A	SN7444A	J, N, W	167
	Totem-Pole	34 ns		70 mW	SN54L44	SN74L44	J, N	167
3-LINE-TO-8-LINE	Totem-Pole	8 ns	7 ns	225 mW	SN54S138	SN74S138	J, N, W	274
	Totem-Pole	22 ns	21 ns	31 mW	SN54LS138	SN74LS138	J, N, W	274
DUAL 2-LINE-TO-4-LINE	Totem-Pole	7.5 ns	6 ns	300 mW	SN54S139	SN74S139	J, N, W	274
	Totem-Pole	22 ns	19 ns	34 mW	SN54LS139	SN74LS139	J, N, W	274
	Totem-Pole	18 ns	15 ns	30 mW	SN54LS155	SN74LS155	J, N, W	312
	Totem-Pole	21 ns	16 ns	250 mW	SN54155	SN74155	J, N, W	312
	Open-Collector	23 ns	18 ns	250 mW	SN54156	SN74156	J, N, W	312

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
BCD-TO-DECIMAL DECODERS/DRIVERS	80 mA	30 V	215 mW	Invalid Codes	SN5445	SN7445	J, N, W	171
	80 mA	15 V	215 mW	Invalid Codes	SN54145	SN74145	J, N, W	288
	7 mA	60 V	80 mW	Invalid Codes		SN74141	J, N, W	278
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS	40 mA	30 V	320 mW	Ripple	SN5446A	SN7446A	J, N, W	173
	40 mA	15 V	320 mW	Ripple	SN5447A	SN7447A	J, N, W	173
	20 mA	30 V	133 mW	Ripple	SN54L46	SN74L46	J, N	173
	20 mA	15 V	133 mW	Ripple	SN54L47	SN74L47	J, N	173
	10 mA	5.5 V	265 mW	Ripple	SN5448	SN7448	J, N, W	173
	6.4 mA	5.5 V	165 mW	Direct	SN5449	SN7449	W	173

RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47



OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTER/LATCH

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-DECIMAL DECODER/DRIVER	7 mA	55 V	340 mW			SN74142	J, N	280
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN SEGMENT DECODER/ LED DRIVER	Constant Current 15 mA	7 V	280 mW	Ripple	SN54143	SN74143	J, N, W	283
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN-SEGMENT DECODER/ LAMP DRIVER	20 mA	15 V	280 mW	Ripple	SN54144		J, N, W	283
	25 mA	15 V	280 mW	Ripple		SN74144	J, N, W	283

RESULTANT DISPLAYS USING '143, '144

ASYNCHRONOUS COUNTERS (RIPPLE CLOCK)—NEGATIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ	PARALLEL LOAD	CLEAR	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
DECADE	50 MHz	Yes	Low	240 mW	SN54196	SN74196	J, N, W	451
	35 MHz	Yes	Low	150 mW	SN54176	SN74176	J, N, W	369
	32 MHz	Set-to-9	High	160 mW	SN5490A	SN7490A	J, N, W	224
	32 MHz	Set-to-9	High	160 mW	SN54290	SN74290	J, N, W	499
	30 MHz	Yes	Low	60 mW	SN54LS196	SN74LS196	J, N, W	451
	3 MHz	Set-to-9	High	20 mW	SN54L90	SN74L90	J, N, T	224
4-BIT BINARY	50 MHz	Yes	Low	240 mW	SN54197	SN74197	J, N, W	451
	35 MHz	Yes	Low	150 mW	SN54177	SN74177	J, N, W	369
	32 MHz	None	High	160 mW	SN5493A	SN7493A	J, N, W	224
	32 MHz	None	High	160 mW	SN54293	SN74293	J, N, W	499
	30 MHz	Yes	Low	60 mW	SN54LS197	SN74LS197	J, N, W	451
	3 MHz	None	High	20 mW	SN54L93	SN74L93	J, N, T	224
DIVIDE-BY-12	32 MHz	None	High	160 mW	SN5492A	SN7492A	J, N, W	224

SYNCHRONOUS COUNTERS—POSITIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ	PARALLEL LOAD	CLEAR	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
DECADE	25 MHz	Sync	Sync-L	305 mW	SN54162	SN74162	J, N, W	325
	25 MHz	Sync	Async-L	305 mW	SN54160	SN74160	J, N, W	325
DECADE UP/DOWN	25 MHz	Async	Async-H	85 mW	SN54LS192	SN74LS192	J, N, W	427
	25 MHz	Async	Async-H	325 mW	SN54192	SN74192	J, N, W	427
	20 MHz	Async	None	90 mW	SN54LS190	SN74LS190	J, N, W	417
	20 MHz	Async	None	325 mW	SN54190	SN74190	J, N, W	417
	3 MHz	Async	Async-H	42 mW	SN54L192	SN74L192	J, N	427
DECADE RATE MULTIPLIER, $\frac{1}{N_{10}}$	25 MHz	Set-to-9	Async-H	270 mW	SN54167	SN74167	J, N, W	347
4-BIT BINARY	25 MHz	Sync	Sync-L	305 mW	SN54163	SN74163	J, N, W	325
	25 MHz	Sync	Async-L	305 mW	SN54161	SN74161	J, N, W	325
4-BIT BINARY	25 MHz	Async	Async-H	85 mW	SN54LS193	SN74LS193	J, N, W	427
	25 MHz	Async	Async-H	325 mW	SN54193	SN74193	J, N, W	427
	20 MHz	Async	None	90 mW	SN54LS191	SN74LS191	J, N, W	417
	20 MHz	Async	None	325 mW	SN54191	SN74191	J, N, W	417
	3 MHz	Async	Async-H	42 mW	SN54L193	SN74L193	J, N	427
6-BIT BINARY RATE MULTIPLIER, $\frac{1}{N_2}$	25 MHz		Async-H	345 mW	SN5497	SN7497	J, N†, W	248

†SN5497 not available in N package

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
			−55°C to 125°C	0°C to 70°C		
FULL BCD PRIORITY ENCODERS	10 ns	225 mW	SN54147	SN74147	J, N, W	290
CASCADABLE OCTAL PRIORITY ENCODERS	10 ns	190 mW	SN54148	SN74148	J, N, W	290
4-BIT CASCADABLE PRIORITY REGISTERS	35 ns	275 mW	SN54278	SN74278	J, N, W	488

B

INVERTERS/NAND/NOR/AND/OR GATES WITH TOTEM-POLE OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.
			−55°C to 125°C	0°C to 70°C	
HEX INVERTERS	9.5 ns	2 mW	BL54LS04Y	BL74LS04Y	568
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	9.5 ns	2 mW	BL54LS00Y	BL74LS00Y	568
	10 ns	10 mW	BL5400Y	BL7400Y	543
	33 ns	1 mW	BL54L00Y	BL74L00Y	545
TRIPLE 3-INPUT POSITIVE-NAND GATES	9.5 ns	2 mW	BL54LS10Y	BL74LS10Y	568
	10 ns	10 mW	BL5410Y	BL7410Y	543
DUAL-4-INPUT POSITIVE-NAND GATES	9.5 ns	2 mW	BL54LS20Y	BL74LS20Y	568
	33 ns	1 mW	BL54L20Y	BL74L20Y	545
8-INPUT POSITIVE-NAND GATES	17 ns	2 mW	BL54LS30Y	BL74LS30Y	568
	33 ns	1 mW	BL54L30Y	BL74L30Y	549
QUADRUPLE 2-INPUT POSITIVE-NOR GATES	10 ns	2.75 mW	BL54LS02Y	BL74LS02Y	568
QUADRUPLE 2-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	BL54LS08Y	BL74LS08Y	568
TRIPLE 3-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	BL54LS11Y	BL74LS11Y	568
DUAL 4-INPUT POSITIVE-AND GATES	12 ns	4.25 mW	BL54LS21Y	BL74LS21Y	568
QUADRUPLE 2-INPUT POSITIVE-OR GATES	12 ns	5 mW	BL54LS32Y	BL74LS32Y	568

INVERTERS/NAND/AND GATES WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.
			−55°C to 125°C	0°C to 70°C	
HEX INVERTERS	16 ns	2 mW	BL54LS05Y	BL74LS05Y	568
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	16 ns	2 mW	BL54LS01Y	BL74LS01Y	568
	16 ns	2 mW	BL54LS03Y	BL74LS03Y	568
	22 ns	10 mW	BL5401Y	BL7401Y	547
DUAL 4-INPUT POSITIVE-NAND GATES	16 ns	2 mW	BL54LS22Y	BL74LS22Y	568
QUADRUPLE 2-INPUT POSITIVE-AND GATES	20 ns	4.25 mW	BL54LS09Y	BL74LS09Y	568
TRIPLE 3-INPUT POSITIVE-AND GATES	20 ns	4.25 mW	BL54LS15Y	BL74LS15Y	568

BUFFERS WITH TOTEM-POLE OUTPUTS

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT VOLTAGE	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.
				−55°C to 125°C	0°C to 70°C	
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	24 mA	−1.2 mA	4.3 mW		BL74LS37Y	568
	12 mA	−1.2 mA	4.3 mW	BL54LS37Y		
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	24 mA	−1.2 mA	5.5 mW		BL74LS28Y	568
	12 mA	−1.2 mA	5.5 mW	BL54LS28Y		

BUFFERS WITH OPEN-COLLECTOR OUTPUTS

DESCRIPTION	LOW-LEVEL OUTPUT CURRENT	HIGH-LEVEL OUTPUT VOLTAGE	TYP POWER DISSIPATION PER GATE	TEMPERATURE RANGE		PAGE NO.
				−55°C to 125°C	0°C to 70°C	
QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS	24 mA	5.5 V	4.3 mW		BL74LS38Y	568
	12 mA	5.5 V	4.3 mW	BL54LS38Y		
QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS	24 mA	5.5 V	5.45 mW		BL74LS33Y	568
	12 mA	5.5 V	5.45 mW	BL54LS33Y		

AND-OR-INVERT GATES

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE		PAGE NO.
			−55°C to 125°C	0°C to 70°C	
4-WIDE 2-3-3-2-INPUT AND-OR-INVERT GATES	12.5 ns	4.5 mW	BL54LS54Y	BL74LS54Y	568
2-WIDE 4-INPUT AND-OR-INVERT GATES	12.5 ns	2.75 mW	BL54LS55Y	BL74LS55Y	568
	43 ns	1.5 mW	BL54L55Y	BL74L55Y	551
DUAL 2-WIDE AND-OR-INVERT GATES	12.5 ns	2.75 mW	BL54LS51Y	BL74LS51Y	568

FLIP-FLOPS

DESCRIPTION	TEMPERATURE RANGE		PAGE NO.
	−55°C to 125°C	0°C to 70°C	
J-K EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET	BL54L67Y	BL74L67Y	553
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR	BL54L68Y	BL74L68Y	556
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK	BL54L69Y	BL74L69Y	559
DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH CLEAR	BL5473Y	BL7473Y	562
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR AND PRESET	BL5474Y	BL7474Y	565

MSI FUNCTIONS

DESCRIPTION/FEATURES		TEMPERATURE RANGE		PAGE NO.
		−55°C to 125°C	0°C to 70°C	
PARALLEL-IN, PARALLEL-OUT, 4-BIT SHIFT REGISTERS	BIDIRECTIONAL	BL54LS194Y	BL74LS194Y	568
	D-TYPE SERIAL INPUT	BL54LS95AY	BL74LS95AY	
	J-$\overline{K}$ SERIAL INPUTS	BL54LS195Y	SN74LS195Y	
	THREE-STATE OUTPUTS	BL54LS295Y	BL74LS295Y	
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS	TWO-STATE OUTPUTS	BL54LS153Y	BL74LS153Y	
	THREE-STATE OUTPUTS	BL54LS253Y	BL74LS253Y	
DECODERS/DEMULTIPLEXERS	3-LINE-TO-8-LINE	BL54S138Y	BL74LS138Y	
	DUAL 2-LINE-TO-4-LINE	BL54LS139Y	BL74LS139Y	
		BL54LS155Y	BL74LS155Y	
30-MHz COUNTERS/LATCHES	DECADE	BL54LS196Y	BL74LS196Y	
	4-BIT BINARY	BL54LS197Y	BL74LS197Y	
4-BIT ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR		BL54LS181Y	BL74LS181Y	

RADIATION-HARDENED TTL
FUNCTIONAL INDEX/SELECTION GUIDE

B

INVERTERS AND POSITIVE-NAND GATES

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO.
HEX INVERTERS	RSN5404	H	585
	RSN54H04	H	585
QUADRUPLE 2-INPUT POSITIVE-NAND GATES	RSN5400	H	581
	RSN54H00	H	581
	RSN54L00	H	583
TRIPLE 3-INPUT POSITIVE-NAND GATES	RSN5410	H	581
	RSN54H10	H	581
	RSN54L10	H	583
DUAL 3-INPUT POSITIVE-NAND GATE	RSN54L130	H	583
DUAL EXPANDABLE 3-INPUT POSITIVE-NAND GATE	RSN54L131	H	583
DUAL 4-INPUT POSITIVE-NAND GATES	RSN5420	H	581
	RSN54H20	H	581
	RSN54L20	H	583
DUAL 4-INPUT POSITIVE-NAND BUFFERS	RSN5440	H	586
	RSN54H40	H	586
11-INPUT POSITIVE-NAND GATES	RSN5431	H	581
	RSN54H31	H	581

AND-OR INVERT GATES

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO.
4-WIDE 3-3-2-3-INPUT AND-OR-INVERT GATES	RSN5457	H	587
	RSN54H57	H	587
	RSN54L57	H	589
2-WIDE 4-INPUT AND-OR-INVERT GATES	RSN5458	H	587
	RSN54H58	H	587
2-WIDE 3-INPUT, 2-WIDE 2-INPUT	RSN5456	H	587
DUAL AND-OR-INVERT GATES	RSN54H56	H	587
DUAL 2-WIDE 3-2-INPUT AND-OR-INVERT GATE	RSN54H66	H	587

FLIP-FLOPS

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO.
S-R MASTER-SLAVE FLIP-FLOP	RSN54L71	H	590
J-K MASTER-SLAVE FLIP-FLOP	RSN54L72	H	593
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS	RSN5474	H	596
	RSN54H74	H	596
	RSN54L74	H	596
DUAL J-K EDGE-TRIGGERED FLIP-FLOP	RSN54H103	H	600

DECODER/DEMULTIPLEXER

DESCRIPTION	TYPE NO.	PACKAGE	PAGE NO.
3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER	RSN54H149	H	603

TTL CROSS-REFERENCE GUIDE

Direct Replacements were selected as pin-for-pin equivalent circuits based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangability in any particular application is not necessarily guaranteed. Before using a substitute, the user should compare the specifications of the substitute device with the detailed specifications of the original device.

TI makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

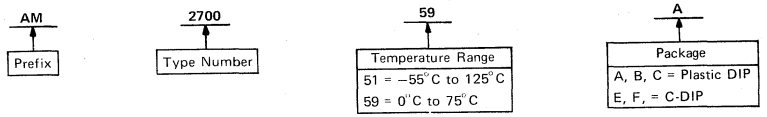
Recommendation for New Designs lists devices performing a similar (sometimes identical) function. Most are pin-for-pin equivalents for the competitor's part. However, the recommended part may have different pin-outs or organizations, as later technologies are listed in some cases to ensure that current high-performance components are recommended.

Only the basic circuit numbers are cross referenced. As the pin-out sometimes varies between a flat-package part and the equivalent DIP part, it is recommended that the manufacturer's specifications be consulted prior to specifying a direct replacement. Other than parts offered only in a flat package, the dual-in-line pin-outs were used as a guide in preparing the following cross references.

This list is intended to give TI replacements for competitors' parts not using the 54/74 numbering system. For a complete listing of parts in the 54 and 74 families, see the functional index, pages 20 through 36.

AMD TTL CROSS-REFERENCE

Example of AMD ordering code:

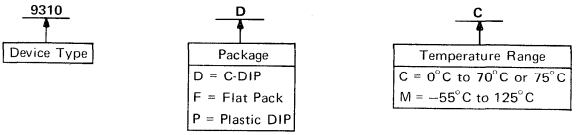


AMD TYPE	RECOMMENDED FOR NEW DESIGNS
2501	SN54191/SN74191
2505	SN54284, SN54285/SN74284, SN74285
2506	SN54S181/SN74S181
2600	SN54121/SN74121
2602	SN54123/SN74123
2700	SN54S200/SN74S200
2701	SN54S206/SN74S206

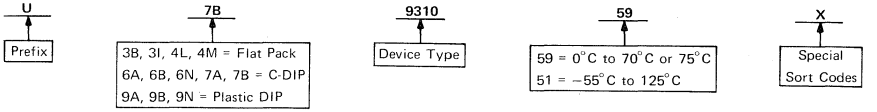
FAIRCHILD TTL CROSS-REFERENCE

Fairchild announced a new method for ordering digital integrated circuits in 1972. Here is a breakdown of the new method:

Example of new order code:



Example of previous order code:



FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
9000	SN29000	SN5472/SN7472
9H00	SN54H00/SN74H00	SN54S00/SN74S00
9L00	SN54LS00/SN74LS00	SN54LS00/SN74LS00
9N00	SN5400/SN7400	SN5400/SN7400
9S00	SN54S00/SN74S00	SN54S00/SN74S00
9001	SN29001	SN5470/SN7470
9H01	SN54H01/SN74H01	SN54S03/SN74S03
9N01	SN5401/SN7401	SN5403/SN7403
9002	SN29002/SN7400, SN5400	SN5400/SN7400
9N02	SN5402/SN7402	SN5402/SN7402
9003	SN29003/SN7410, SN5410	SN5410/SN7410
9N03	SN5403/SN7403	SN5403/SN7403
9S03	SN54S03/SN74S03	SN54S03/SN74S03
9004	SN29004/SN7420, SN5420	SN5420/SN7420
9H04	SN54H04/SN74H04	SN54S04/SN74S04
9L04	SN54LS04/SN74LS04	SN54LS04/SN74LS04
9N04	SN5404/SN7404	SN5404/SN7404
9S04	SN54S04/SN74S04	SN54S04/SN74S04
9005	SN29005/SN7450, SN5450	SN5450/SN7450
9H05	SN54H05/SN74H05	SN54S05/SN74S05
9N05	SN5405/SN7405	SN5405/SN7405
9S05	SN54S05/SN74S05	SN54S05/SN74S05
9006	SN5460/SN7460	SN5460/SN7460
9N06	SN5406/SN7406	SN5406/SN7406
9007	SN29007	SN5430/SN7430
9N07	SN5407/SN7407	SN5407/SN7407
9008	SN29008	SN54S65/SN74S65
9N08	SN5408/SN7408	SN5408/SN7408

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
9009	SN29009/SN7440, SN5440	SN5440/SN7440
9N09	SN5409/SN7409	SN5409/SN7409
9H10	SN54H10/SN74H10	SN54S10/SN74S10
9N10	SN5410/SN7410	SN5410/SN7410
9H11	SN54H11/SN74H11	SN54S11/SN74S11
9012	SN29012/SN7403, SN5403	SN5403/SN7403
9N13	SN5413/SN7413	SN5413/SN7413
9014		SN54S135/SN74S135
9015		SN5402/SN7402
9016	SN29016/SN7404, SN5404	SN5404/SN7404
9N16	SN5416/SN7416	SN5416/SN7416
9017	SN5405/SN7405	SN5405/SN7405
9N17	SN5417/SN7417	SN5417/SN7417
9H20	SN54H20/SN74H20	SN54S20/SN74S20
9N20	SN5420/SN7420	SN5420/SN7420
9S20	SN54S20/SN74S20	SN54S20/SN74S20
9H21	SN54H21/SN74H21	SN54S15/SN74S15
9H22	SN54H22/SN74H22	SN54S22/SN74S22
9S22	SN54S22/SN74S22	SN54S22/SN74S22
9024	SN29024/SN74109, SN54109	SN54109/SN74109
9L24	SN54LS109/SN74LS109	SN54LS109/SN74LS109
9N26	SN5426/SN7426	SN5426/SN7426
9H30	SN54H30/SN74H30	SN54S30/SN74S30
9N30	SN5430/SN7430	SN5430/SN7430
9033	SN83433, SN93433	SN5481A/SN7481A
9034	SN5488A/SN7488A	SN5488A/SN7488A
9N37	SN5437/SN7437	SN5437/SN7437
9N38	SN5438/SN7438	SN5438/SN7438

FAIRCHILD TTL CROSS-REFERENCE

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
9H40	SN54H40/SN74H40	SN54S40/SN74S40
9S40	SN54S40/SN74S40	SN54S40/SN74S40
9H50	SN54H50/SN74H50	SN54S51/SN74S51
9N50	SN5450/SN7450	SN5450/SN7450
9H51	SN54H51/SN74H51	SN54S51/SN74S51
9N51	SN5451/SN7451	SN5451/SN7451
9H52	SN54H52/SN74H52	SN54S51/SN74S51
9N53	SN5453/SN7453	SN5453/SN7453
9L54	SN54L54/SN74L54	SN54LS54/SN74LS54
9N54	SN5454/SN7454	SN5454/SN7454
9H55	SN54H55/SN74H55	SN54S65/SN74S65
9H60	SN54H60/SN74H60	SN54S11/SN74S11
9N60	SN5460/SN7460	SN5460/SN7460
9H61	SN54H61/SN74H61	SN54S11/SN74S11
9S64	SN54S64/SN74S64	SN54S64/SN74S64
9S65	SN54S65/SN74S65	SN54S65/SN74S65
9N70	SN5470/SN7470	SN5470/SN7470
9H71	SN54H71/SN74H71	SN54S112/SN74S112
9H72	SN54H72/SN74H72	SN54S112/SN74S112
9N72	SN5472/SN7472	SN5472/SN7472
9H73	SN54H73/SN74H73	SN54S113/SN74S113
9N73	SN5473/SN7473	SN5473/SN7473
9H74	SN54H74/SN74H74	SN54S74/SN74S74
9N74	SN5474/SN7474	SN5474/SN7474
9S74	SN54S74/SN74S74	SN54S74/SN74S74
9H76	SN54H76/SN74H76	SN54S112/SN74S112
9N76	SN5476/SN7476	SN5476/SN7476
9H78	SN54H78/SN74H78	SN54S114/SN74S114
9L86	SN54L86/SN74L86	SN54LS86/SN74LS86
9N86	SN5486/SN7486	SN5486/SN7486
9H101	SN54H101/SN74H101	SN54S112/SN74S112
9H102	SN54H102/SN74H102	SN54S112/SN74S112
9H103	SN54H103/SN74H103	SN54S113/SN74S113
9H106	SN54H106/SN74H106	SN54S112/SN74S112
9H107	SN54107/SN74107	SN54107/SN74107
9H108	SN54H108/SN74H108	SN54S114/SN74S114
9S140	SN54S140/SN74S140	SN54S140/SN74S140
9300	SN39300/SN54195 SN29300/SN74195	SN54195/SN74195
93H00	SN54S195/SN74S195	SN54S195/SN74S195
93L00	SN54LS195/SN74LS195	SN54LS195/SN74LS195
9301	SN39301/SN29301	SN5442A/SN7442A
93L01		SN54L42/SN74L42
9304		SN54H183/SN74H183
9307	SN5448A/SN7448A	SN5448A/SN7448A
9308	SN39308/SN54116 SN29308/SN74116	SN54116/SN74116
9309	SN39309/SN29309	SN54153/SN74153
93L09		SN54L153/SN74L153
9310	SN39310/SN54160 SN29310/SN74160	SN54162/SN74162

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
9311	SN39311/SN54154 SN29311/SN74154	SN54154/SN74154
93L11	SN54L154/SN74L154	SN54L154/SN74L154
9312	SN39312/SN29312	SN54151A/SN74151A
9313		SN54251/SN74251
9314		SN54175/SN74175
93L14		SN54L75/SN74L75
9315	SN54141	SN74141
9316	SN39316/SN54161 SN29316/SN74161	SN54163/SN74163
9317B	SN5446A/SN7446A	SN5446A/SN7446A
9317C	SN5446A/SN7446A	SN5446A/SN7446A
9318	SN39318/SN54148 SN29318/SN74148	SN54148/SN74148
93L21	SN54LS139/SN74LS139	SN54LS139/SN74LS139
9321	SN54S139/SN74S139	SN54S139/SN74S139
9322	SN39322/SN54157 SN29322/SN74157	SN54157/SN74157
93L22	SN54L157/SN74L157	SN54L157/SN74L157
9324		SN54S85/SN74S85
93L24		SN54L85/SN74L85
9328		SN5491A/SN7491A
93L28		SN54L91/SN74L91
9338		SN74172
9340		SN54181/SN74181
93L40		SN54LS181/SN74LS181
9341	SN54181/SN74181	SN54S181/SN74S181
9342	SN54182/SN74182	SN54S182/SN74S182
9344		SN54284/SN74284 SN54285/SN74285
9345	SN5445/SN7445	SN5445/SN7445
9348		SN54S280/SN74S280
9350	SN54290/SN74290	SN54290/SN74290
9352	SN5442A/SN7442A	SN5442A/SN7442A
9353	SN5443A/SN7443A	SN5443A/SN7443A
9354	SN5444A/SN7444A	SN5444A/SN7444A
9356	SN54293/SN74293	SN54293/SN74293
9357A	SN5446A/SN7446A	SN5446A/SN7446A
9357B	SN5447A/SN7447A	SN5447A/SN7447A
9358	SN5448/SN7448	SN5448/SN7448
9359	SN5449/SN7449	SN5449/SN7449
9360	SN54192/SN74192	SN54192/SN74192
9366	SN54193/SN74193	SN54193/SN74193
93H72		SN54S194/SN74S194
9375	SN5475/SN7475	SN54175/SN74175
9377	SN5477/SN7477	SN54175/SN74175
9380	SN5480/SN7480	SN5480/SN7480
9382	SN5482/SN7482	SN5482/SN7482
9383	SN5483A/SN7483A	SN54283/SN74283

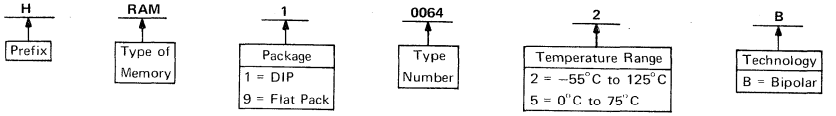
FAIRCHILD TTL CROSS-REFERENCE

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
9386	SN54LS266/SN74LS266	SN54LS266/SN74LS266
93H87	SN54H87/SN74H87	SN54H87/SN74H87
9390	SN5490A/SN7490A	SN54290/SN74290
9391	SN5491A/SN7491A	SN5491A/SN7491A
9392	SN5492A/SN7492A	SN5492A/SN7492A
9393	SN5493A/SN7493A	SN54293/SN74293
9394	SN5494/SN7494	SN5494/SN7494
9395	SN5495A/SN7495A	SN5495A/SN7495A
9396	SN5496/SN7496	SN5496/SN7496
93145	SN54145/SN74145	SN54145/SN74145
93150	SN54150/SN74150	SN54150/SN74150
93151	SN54151/SN74151	SN54151A/SN74151A
93152	SN54152/SN74152	SN54151A/SN74151A
93153	SN54153/SN74153	SN54153/SN74153
93165	SN54165/SN74165	SN54165/SN74165

FSC TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGN
93180	SN54180/SN74180	SN54180/SN74180
93H183	SN54H183/SN74H183	SN54H183/SN74H183
93400		SN54S200/SN74S200
93403	SN7489	SN7489
93406	SN54187/SN74187	SN54187/SN74187
93407	SN5481A/SN7481A	SN5481A/SN7481A
93410		SN54S200/SN74S200
93433	SN83433, SN93433	SN5481A/SN7481A
93434	SN5488A/SN7488A	SN5488A/SN7488A
9600		SN54121/SN74121
9601	SN29601	SN54122/SN74122
9602		SN54123/SN74123
9603	SN54121/SN74121	SN54121/SN74121

HARRIS (MEMORY CIRCUITS) CROSS-REFERENCE

Example of Harris order code:



HARRIS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
RAM 1-0064	SN7489	SN7489
PROM 1-0512	SN74186	SN74186
PROM 1-1024		*SN74S287
PROM 1-1024A		*SN74S287
ROM 1-1024	SN54187/SN74187	SN54187/SN74187
PROM 1-8256	SN74188	SN74188

*To be announced.

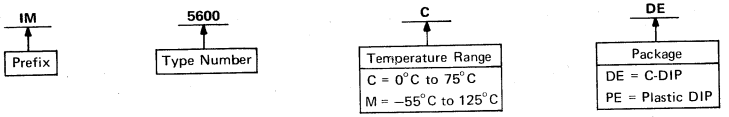
INTEL TTL CROSS-REFERENCE

Example of Intel order code:

INTEL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
3101	SN7489	SN7489
3102		SN54S200/SN74S200
3106A	SN54S200/SN74S200	SN54S200/SN74S200
3107A	SN54S206/SN74S206	SN54S206/SN74S206
3205		SN54S138/SN74S138
3404		SN54S174/SN74S174
3301A	SN54187/SN74187	SN54187/SN74187
3301A/0141	SN54285/SN74285	SN54285/SN74285
3301A/0142	SN54284/SN74284	SN54284/SN74284

INTERSIL TTL CROSS-REFERENCE

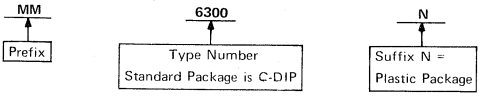
Example of Intersil ordering code:



INTERSIL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
5501	SN7489	SN7489
5502	SN5481A/SN7481A	SN5481A/SN7481A
5503		SN54S206/SN74S206
5512	SN5481A/SN7481A	SN5481A/SN7481A
5523	SN54S200/SN74S200	SN54S200/SN74S200
5533	SN54S206/SN74S206	SN54S206/SN74S206
5600	SN5488A/SN7488A	SN5488A/SN7488A
5610	SN5488A/SN7488A	SN5488A/SN7488A
5543	SN54S200/SN74S200	SN54S200/SN74S200
5553	SN54S206/SN74S206	SN54S206/SN74S206
5563		SN54S206/SN74S206

MONOLITHIC MEMORIES TTL CROSS-REFERENCE

Example of Monolithic Memories ordering code:

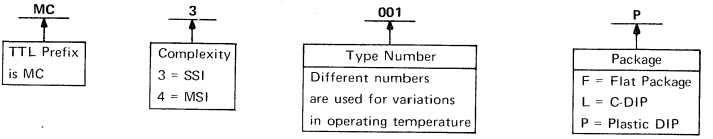


B

MONOLITHIC MEMORIES TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
6205	*SN74S270	*SN74S270
6240		*SN74S270
6300	*SN74S287	*SN74S287
6330	SN74188	SN74188
6331		SN74188

MOTOROLA TTL CROSS-REFERENCE

Example of Motorola order code:



MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC3000	SN74H00	SN74S00
MC3001	SN7408	SN74S11
MC3002		SN74S02
MC3003	SN7432	
MC3004	SN74H01	SN74S03
MC3005	SN74H10	SN74S10
MC3006	SN74H11	SN74S11
MC3008	SN74H04	SN74S04
MC3009	SN74H05	SN74S05
MC3010	SN74H20	SN74S20
MC3011	SN74H21	SN74S11
MC3012	SN74H22	SN74S22
MC3015		SN74S133
MC3016	SN74H30	SN74S133
MC3018	SN74H62	SN74S11
MC3019	SN74H61	SN74S11
MC3020	SN74H50	SN74S51
MC3021	SN74S86	SN74S86
MC3022		SN74S135

MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC3023	SN74H51	SN74S51
MC3024	SN74H40	SN74S40
MC3025	SN74H40	SN74S40
MC3030	SN74H60	SN74S11
MC3031	SN74H52	SN74S64
MC3032	SN74H53	SN74S64
MC3033	SN74H54	SN74S64
MC3034	SN74H55	SN74S64
MC3050		SN74S112
MC3051		SN74S113
MC3052		SN74S114
MC3054	SN74H71	SN74S112
MC3055	SN74H72	SN74S112
MC3060	SN74H74	SN74S74
MC3061	SN74S114	SN74S114
MC3062	SN74S113	SN74S113
MC3063	SN74H73	SN74S112
MC3100	SN54H00	SN54S00
MC3101	SN5408	SN54S11

*To be announced.

MOTOROLA TTL CROSS-REFERENCE

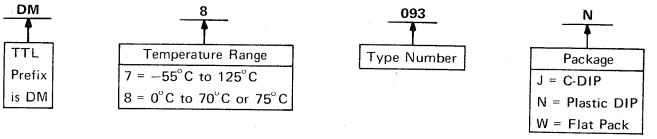
MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC3102		SN54S02
MC3103	SN5432	
MC3104	SN54H01	SN54S03
MC3105	SN54H10	SN54S10
MC3106	SN54H11	SN54S11
MC3108	SN54H04	SN54S04
MC3109	SN54H05	SN54S05
MC3110	SN54H20	SN54S20
MC3111	SN54H21	SN54S11
MC3112	SN54H22	SN54S22
MC3115		SN54S133
MC3116	SN54H30	SN54S133
MC3118	SN54H62	SN54S11
MC3119	SN54H61	SN54S11
MC3120	SN54H50	SN54S51
MC3121	SN54S86	SN54S86
MC3122		SN54S135
MC3123	SN54H51	SN54S51
MC3124	SN54H40	SN54S40
MC3125	SN54H40	SN54S40
MC3130	SN54H60	SN54S11
MC3131	SN54H52	SN54S64
MC3132	SN54H53	SN54S64
MC3133	SN54H54	SN54S64
MC3134	SN54H55	SN54S64
MC3150		SN54S112
MC3151		SN54S113
MC3152		SN54S114
MC3154	SN54H71	SN54S112
MC3155	SN54H72	SN54S112
MC3160	SN54H74	SN54S74
MC3161	SN54S114	SN54S114
MC3162	SN54S113	SN54S113
MC3163	SN54H73	SN54S112
MC4000		SN74S139
MC4001		SN74184/SN74185A
MC4002		SN74S139
MC4004	SN7481A	SN7481A
MC4005	SN7481A	SN7481A
MC4006		SN74S138
MC4007		SN74S139
MC4008		SN74S280

MOTOROLA TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
MC4010		SN74S135
MC4012		SN74S194
MC4015		SN74S195
MC4016		SN74190
MC4018		SN74191
MC4021		SN74S85
MC4022		SN74S85
MC4023		SN7492A
MC4024		*SN74S124
MC4026		SN74283
MC4027		SN74283
MC4028		SN74S181
MC4029		SN74S181
MC4030		SN74S181
MC4031		SN74S181
MC4032		SN74S182
MC4035		SN74S174
MC4037		SN74S174
MC4038		SN74S138
MC4039		SN7448
MC4040		SN74S139
MC4042		SN74128
MC4043		SN74128
MC4048		SN74S138
MC4050		SN74143
MC4051		SN74144
MC4062		SN74S64
MC4300		SN54S139
MC4304	SN5481A	SN5481A
MC4305	SN5481A	SN5481A
MC4306		SN54S138
MC4308		SN54S280
MC4316		SN54190
MC4318		SN54191
MC4326		SN54283
MC4327		SN54283
MC4328		SN54S181
MC4331		SN54S181
MC4332		SN54S182
MC4335		SN54S174
MC4337		SN54S174
MC4350		SN54143

*To be announced.

NATIONAL TTL CROSS-REFERENCE

Example of National order code:



B

NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
7093	SN54125	SN54125
7094	SN54126	SN54126
7095		SN5407
7096		SN5406
7121	SN54251	SN54251
71L22	SN54L157	SN54L157
7123	SN54S257	SN54S257
7130		SN54S85
7131		SN54S85
7160		SN54S85
7200		SN54S85
7210		SN54151A
7211		SN54151A
7213	SN54154	SN54154
7214	SN54LS253	SN54LS253
7219		SN54150
7220		SN54S280
7223		SN54S139
7230		SN54S257
7520		SN5497
7551	SN54173	SN54173
7552		SN54176
7553		SN54177
7554		SN54116
7555		SN54196
7556		SN54197
7560	SN54192	SN54192
75L60	SN54L192	SN54L192
7563	SN54193	SN54193
75L63	SN54L193	SN54L193
7570	SN54164	SN54164
7582	SN54S206	SN54S206
7588	SN5488A	SN5488A
7590	SN54165	SN54165

NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
7594		SN54S200
7595		SN5488A
7596		SN5488A
7597		SN54187
7598		SN5488A
76L70	SN54L164	SN54L164
7810	5426	5426
7811		SN5426
7812	SN5416	SN5416
7819		SN5417
8093	SN74125	SN74125
8094	SN74126	SN74126
8095		SN7407
8096		SN7406
8121	SN74251	SN74251
81L22	SN74L157	SN74L157
8123	SN74S257	SN74S257
8130		SN74S85
8131		SN74S85
8160		SN74S85
8200		SN74S85
8210		SN74151A
8211		SN74151A
8213	SN74154	SN74154
8214	SN74LS253	SN74LS253
8219		SN74150
8220		SN74S280
8223		SN74S139
8230		SN74S257
8520		SN7497
8551	SN74173	SN74173
8552		SN74176

NATIONAL TTL CROSS-REFERENCE

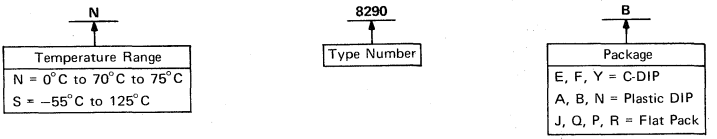
NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8553		SN74177
8554		SN74116
8555		SN74196
8556		SN74197
8560	SN74192	SN74192
85L60	SN74L192	SN74LS192
8563	SN74193	SN74193
85L63	SN74L193	SN74LS193

NATIONAL TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8579	SN74164	SN74164
8588	SN7488A	SN7488A
8590	SN74165	SN74165
8598		SN7488A
8599	*SN74S189	*SN74S189
86L70	SN74L164	SN74L164
8810	SN7426	SN7426

B

SIGNETICS TTL CROSS-REFERENCE

Example of Signetics order code:



SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8H16		SN54S20/SN74S20
8H20		SN54S112/SN74S112
8H21		SN54S112/SN74S112
8H22		SN54S112/SN74S112
8H70	SN54H11/SN74H11	SN54S11/SN74S11
8H80	SN54H00/SN74H00	SN54S00/SN74S00
8H90	SN54H04/SN74H04	SN54S04/SN74S04
8T01		SN74141
8T04		SN5447A/SN7447A
8T05		SN5448/SN7448
8T06		SN54143/SN74143
8T09		SN54128/SN74128
8T10	SN54173/SN74173	SN74173
8T13		SN54128/SN74128
8T18		SN5426/SN7426
8T20		SN54121/SN74121
8T22	SN54122/SN74122	SN54122/SN74122
8T23		SN54128/SN74128
8T26		SN54125/SN74125
8T80		SN5426/SN7426
8T90		SN5406/SN7406
8162		SN54121/SN74121
8200		SN54174/SN74174
8201		SN54174/SN74174
8202		SN54174/SN74174
8203		SN54174/SN74174
8204		*SN74S270

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8205		*SN74S270
8206	SN74200	SN74200
82S06	SN54S200/SN74S200	SN54S200/SN74S200
8207	SN54S206/SN74S206	SN54S206/SN74S206
82S07	SN54S206/SN74S206	SN54S206/SN74S206
8223	SN74188	SN74188
8224	SN5488A/SN7488A	SN5488A/SN7488A
8225	SN7489	SN7489
82S26	*SN74S287	*SN74S287
8228		*SN74S270
82S29	*SN74S287	*SN74S287
8230	SN39312/SN29312	SN54151A/SN74151A
82S30		SN54S151A/SN74S151A
8231		SN54151A/SN74151A
82S31		SN54S151/SN74S151
8232		SN54151A/SN74151A
82S32		SN54S151/SN74S151
8233		SN54153/SN74153
82S33		SN54S153/SN74S153
8234		SN54153/SN74153
82S34		SN54S153/SN74S153
8235		SN54153/SN74153
8241		SN5486/SN7486
82S41		SN54S86/SN74S86
8242	SN54LS266/SN74LS266	SN54LS266/SN74LS266
82S42		SN54S135/SN74S135
8243		SN54198/SN74198

*To be announced.

SIGNETICS TTL CROSS-REFERENCE

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8250		SN5442A/SN7442A
82S50		SN54138/SN74138
8252	SN39301/SN29301	SN5442A/SN7442A
82S52		SN54S138/SN74S138
8260		SN54S181/SN74S181
8261		SN54S182/SN74S182
8262		SN54180/SN74180
82S63		SN54S280/SN74S280
8263		SN54153/SN74153
8264		SN54153/SN74153
8266		SN54157/SN74157
82S66		SN54S157/SN74S157
8267		SN54157/SN74157
82S67		SN54S157/SN74S157
8268	SN5480/SN7480	SN54181/SN74181
8269		SN5485/SN7485
8270	SN54178/SN74178	SN54194/SN74194
8271	SN54179/SN74179	SN54194/SN74194
8273		SN54198/SN74198
8274		SN54198/SN74198
8275		SN54174/SN74174
8276		SN5491A/SN7491A
8277		SN5491A/SN7491A
8280	SN54176/SN74176	SN54176/SN74176
8281	SN54177/SN74177	SN54177/SN74177
8283		SN54191/SN74191
8285		SN54190/SN74190
8288		SN54163/SN74163
8290	SN54196/SN74196	SN54196/SN74196
8291	SN54197/SN74197	SN54197/SN74197
8292	SN54LS196/SN74LS196	SN54LS196/SN74LS196
8293	SN54LS197/SN74LS197	SN54LS197/SN74LS197
8415		SN5420/SN7420
8416		SN5420/SN7420

SIGNETICS TYPE	TI DIRECT REPLACEMENT	RECOMMENDED FOR NEW DESIGNS
8417		SN5410/SN7410
8424		SN54111/SN74111
8425		SN54111/SN74111
8440		SN5450/SN7450
8455	SN5440/SN7440	SN5440/SN7440
8470	SN5410/SN7410	SN5410/SN7410
8471	SN5412/SN7412	SN5412/SN7412
8480	SN5400/SN7400	SN5400/SN7400
8481	SN5403/SN7403	SN5403/SN7403
8490	SN5404/SN7404	SN5404/SN7404
8706		SN5460/SN7460
8731		SN5460/SN7460
8806	SN5460/SN7460	SN5460/SN7460
8808	SN5430/SN7430	SN5430/SN7430
8815	SN5425/SN7425	SN5425/SN7425
8816		SN5420/SN7420
8821		SN5476/SN7476
8822		SN54107/SN74107
8824		SN5476/SN7476
8825		SN5470/SN7470
8826		SN54107/SN74107
8827		SN5476/SN7476
8828	SN5474/SN7474	SN5474/SN7474
8829	SN54110/SN74110	SN54110/SN74110
8840	SN5450/SN7450	SN5450/SN7450
8848	SN54H54/SN74H74	SN54S64/SN74S64
8855		SN5440/SN7440
8870		SN5410/SN7410
8875	SN5427/SN7427	SN5427/SN7427
8880		SN5400/SN7400
8881	SN5401/SN7401	SN5401/SN7401
8885		SN5402/SN7402
8890	SN5404/SN7404	SN5404/SN7404
8891	SN5405/SN7405	SN5405/SN7405

Ordering Instructions and Mechanical Data

ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book, unless otherwise noted, apply for circuit type(s) listed in the page heading regardless of package. Except for the beam-lead chips, the availability of a circuit function in a particular package is denoted by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section. Beam-lead chip designations and outlines are shown on individual data sheets.

Factory orders for circuits described in this catalog should include a four-part type number as explained in the following example.

EXAMPLE: SN 54H72 N –00

1. Prefix

MUST CONTAIN TWO OR THREE LETTERS
(From Individual Data Sheet)

RSN	Radiation-Hardened Circuit
SN	Standard Prefix
SNM	Mach IV, Level I
SNA	Mach IV, Level II
SNC	Mach IV, Level III
SNH	Mach IV, Level IV

2. Unique Circuit Description

MUST CONTAIN FOUR TO SEVEN CHARACTERS
(From Individual Data Sheet)

Examples: 5410
74H10
54S112
54L78
74LS153
74188A

3. Package

MUST CONTAIN A SINGLE LETTER
H, J, N, T, W
(From Pin-Connection Diagram on Individual Data Sheet)

4. Instructions (Dash No.)

MUST CONTAIN TWO NUMBERS
(From Dash No. Column of Following Table)

PACKAGES	FORMED LEADS	SOLDER-DIPPED LEADS	INSULATOR	CARRIER	ORDER DASH NO.
METAL FLAT PACKAGES					
T	No	No	No	†	00
T	Yes	No	Yes	†	01
T	No	No	No	Mech-Pak	02
T	No	No	Yes	Mech-Pak	03
T	Yes	No	No	Mech-Pak	04
T	Yes	No	Yes	Mech-Pak	05
T	No	No	Yes	†	06
T	Yes	No	No	†	07
T	No	Yes	No	†	10
T	Yes	Yes	Yes	†	11
T	No	Yes	No	Mech-Pak	12
T	No	Yes	Yes	Mech-Pak	13
T	Yes	Yes	No	Mech-Pak	14
T	Yes	Yes	Yes	Mech-Pak	15
T	No	Yes	Yes	†	16
T	Yes	Yes	No	†	17
CERAMIC FLAT PACKAGES					
H, W	No	No	N/A	†	00
H	No	No	N/A	Mech-Pak	02
H, W	No	Yes	N/A	†	10
DUAL-IN-LINE PACKAGES					
J, N	No	No	N/A	†	00
N	No	Yes	N/A	†	10

†These circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier. Please contact your TI sales representative for the method which will best suit your particular needs.

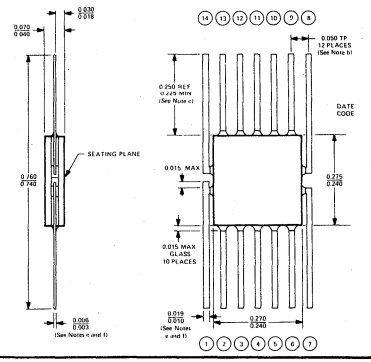
Flat (H, T, W)
–Mech-Pakette
–Barnes Carrier
–Milton Ross Carrier

Dual-in-line (J, N)
–Slide Magazines
–A-Channel Plastic Tubing
–Barnes Carrier (N only)
–Sectioned Cardboard Box
–Individual Plastic Box

H flat package (inch dimensions, see page 53 for metric dimensions)

This package consists of a ceramic base, ceramic cap, and a 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (–00) require no additional cleaning or processing when used in welded or soldered assembly.

14-PIN H CERAMIC FLAT PACKAGE OUTLINE

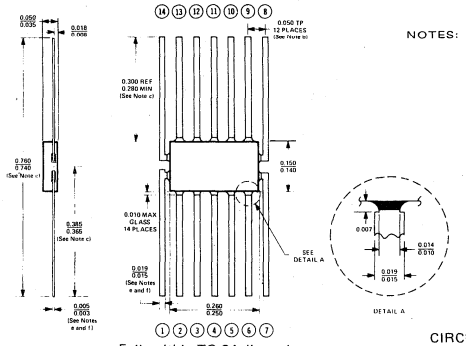


NOTES:
a. All dimensions are in inches.
b. Lead centerlines are located within 0.005 of true position (TP) relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Index tab on pin 1 denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.

T flat package (inch dimensions, see page 53 for metric dimensions)

This hermetic package features glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram.

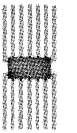
14-PIN T FLAT PACKAGE OUTLINE



Falls within TO-84 dimensions.

NOTES:
a. All dimensions are in inches.
b. Lead centerlines are located within 0.005 of true position (TP) relative to body centerlines. This is measured along lines located within 0.030 from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Index tab on pin 1 denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 0.050 of the package body.

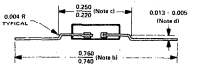
CIRCUIT SUBSTRATE IS IN ELECTRICAL CONTACT WITH THE BODY OF THE PACKAGE.



T package leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Circuits can be removed from Mech-Pak carriers with lead lengths up to 0.300 inch.

FORMED LEADS



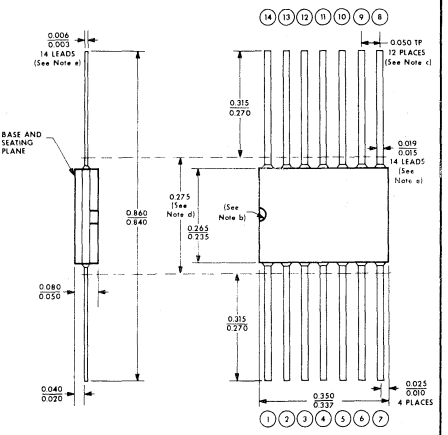
NOTES:
a. All dimensions are in inches.
b. Not applicable in Mech-Pak carrier.
c. Measured from centerline of outside bends.
d. Measured from center of lead to bottom of package where lead emerges from body.
e. When solder-dipped leads are specified, dipped area of lead extends from lead tip to outside bend (minimum).

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

W ceramic flat packages (inch dimensions, see page 54 for metric dimensions)

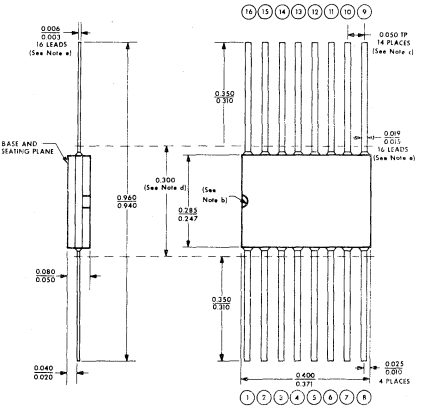
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16-, or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC FLAT PACKAGE OUTLINE



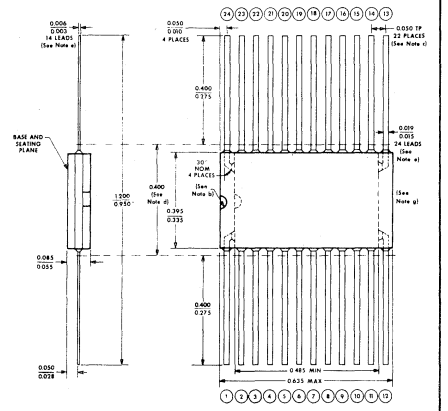
Falls Within
JEDEC MO-004AA Dimensions

16-PIN W CERAMIC FLAT PACKAGE OUTLINE



Falls Within
JEDEC MO-004AG Dimensions

24-PIN W CERAMIC FLAT PACKAGE OUTLINE



Falls Within
JEDEC MO-019AA Dimensions

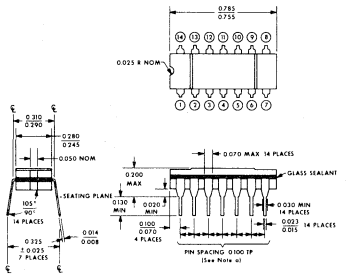
NOTES:

a. All dimensions are in inches.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.005 radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 0.050 of package body.
g. End configuration of 24-pin package is at the option of TI.

J ceramic dual-in-line packages (inch dimensions, see page 55 for metric dimensions)

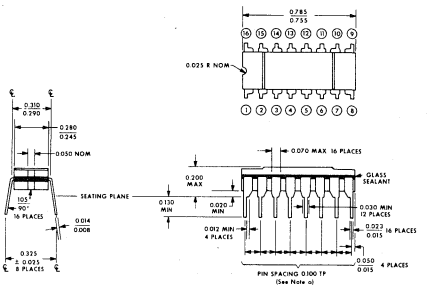
These hermetically sealed, dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300-inch or (0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE

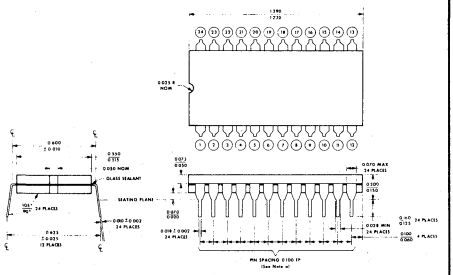


Falls Within JEDEC TO-116 and
MO-001AA Dimensions

16-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE

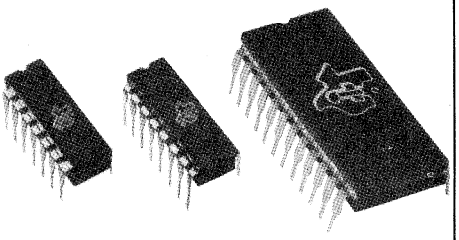


24-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE



Falls Within
JEDEC MO-015AA Dimensions

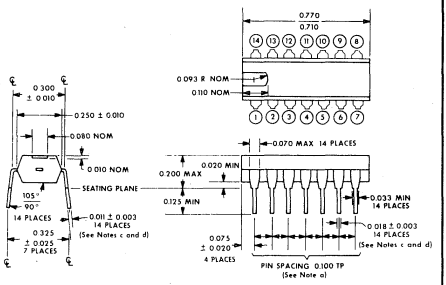
NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.



N plastic dual-in-line packages (inch dimensions, see page 56 for metric dimensions)

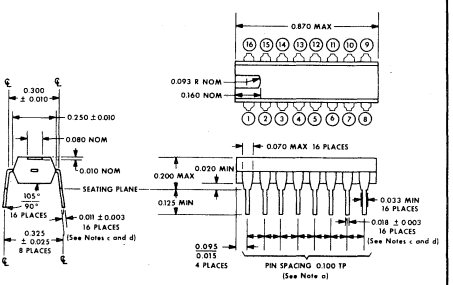
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 0.300-inch (or 0.600-inch) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE

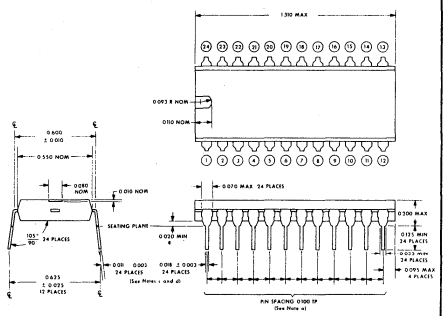


Falls Within JEDEC TO-116 and MO-001AA Dimensions

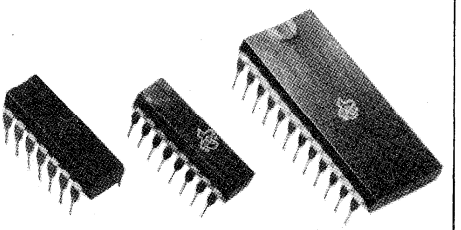
16-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE



24-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE



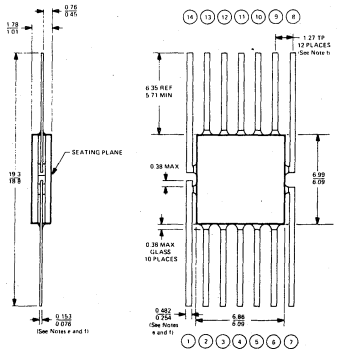
NOTES: a. Each pin centerline is located within 0.010 of its true longitudinal position.
b. All dimensions are in inches unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.020 above the seating plane.



H flat package (metric dimensions, see page 49 for inch dimensions)

This package consists of a ceramic base, ceramic cap, and a 14-lead frame. Hermetic sealing is accomplished with glass. Gold-plated leads (–00) require no additional cleaning or processing when used in welded or soldered assembly.

14-PIN H CERAMIC FLAT PACKAGE OUTLINE

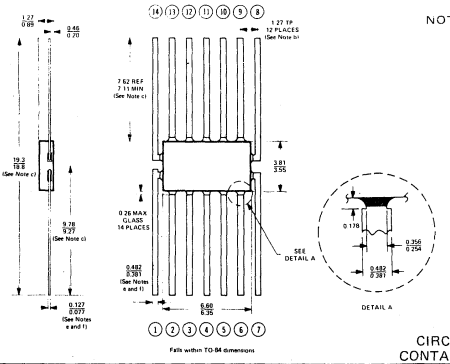


NOTES:
a. All dimensions are in millimeters.
b. Lead centerlines are located within 0.13 mm of true position (TP) relative to body centerlines. This is measured along lines located within 0.76 mm from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Index tab on pin 1 denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 1.27 mm of the package body.

T flat package (metric dimensions, see page 49 for inch dimensions)

This hermetic package features glass-to-metal seals and welded construction. Package body and leads are gold-plated F-15‡ glass-sealing alloy. Approximate weight is 0.1 gram.

14-PIN T FLAT PACKAGE OUTLINE



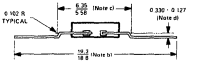
NOTES:
a. All dimensions are in millimeters.
b. Lead centerlines are located within 0.13 mm of true position (TP) relative to body centerlines. This is measured along lines located within 0.76 mm from (and parallel to) the sides of the package.
c. Not applicable in Mech-Pak carrier.
d. Index tab on pin 1 denotes orientation of package.
e. This dimension does not apply for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to within 1.27 mm of the package body.

CIRCUIT SUBSTRATE IS IN ELECTRICAL CONTACT WITH THE BODY OF THE PACKAGE.

T package leads

Gold-plated F-15‡ leads require no additional cleaning or processing when used in soldered or welded assembly. Solder-dipped leads are also available. Formed leads are available to facilitate planar mounting of networks on flat circuit boards. Circuits can be removed from Mech-Pak carriers with lead lengths up to 7.62 mm.

FORMED LEADS



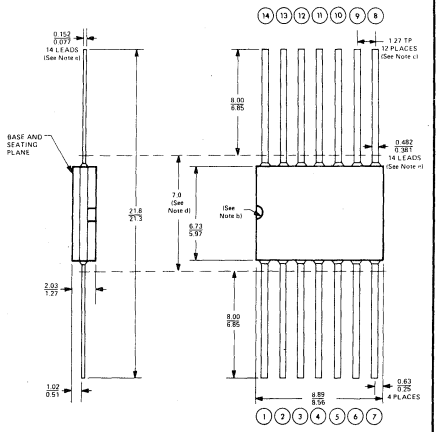
NOTES:
a. All dimensions are in millimeters.
b. Not applicable in Mech-Pak carrier.
c. Measured from centerline of outside bends.
d. Measured from center of lead to bottom of package where lead emerges from body.
e. When solder-dipped leads are specified, dipped area of lead extends from lead tip to outside bend (minimum).

‡F-15 is the ASTM designation for an iron-nickel-cobalt alloy containing nominally 53% iron, 29% nickel, and 17% cobalt.

W ceramic flat packages (metric dimensions, see page 50 for inch dimensions)

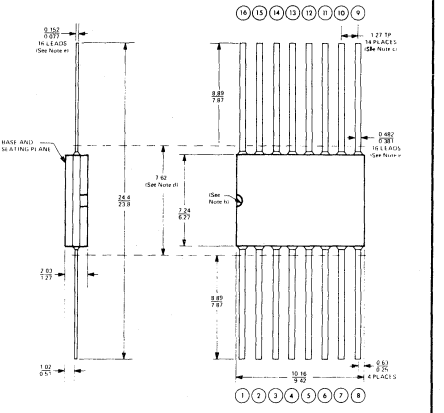
These hermetically sealed flat packages consist of an electrically nonconductive ceramic base and cap, and a 14-, 16-, or 24-lead frame. Hermetic sealing is accomplished with glass. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN W CERAMIC FLAT PACKAGE OUTLINE



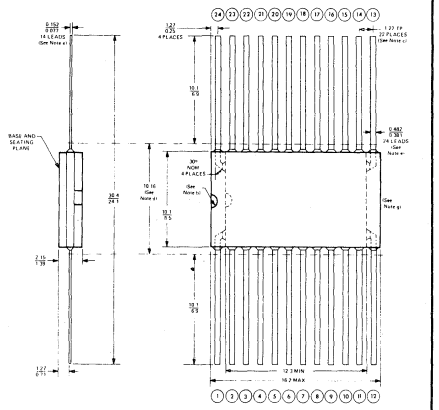
Falls Within
JEDEC MO-004AA Dimensions

16-PIN W CERAMIC FLAT PACKAGE OUTLINE



Falls Within
JEDEC MO-004AG Dimensions

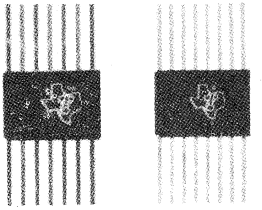
24-PIN W CERAMIC FLAT PACKAGE OUTLINE

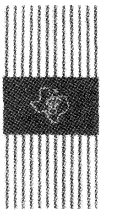


Falls Within
JEDEC MO-019AA Dimensions

NOTES:

a. All dimensions are in millimeters.
b. Index point is provided on cap for terminal identification only.
c. Leads are within 0.13 mm radius of true position (TP) at maximum material condition.
d. This dimension determines a zone within which all body and lead irregularities lie.
e. Not applicable for solder-dipped leads.
f. When solder-dipped leads are specified, dipped area extends from lead tip to within 1.27 mm of package body.
g. End configuration of 24-pin package is at the option of TI.

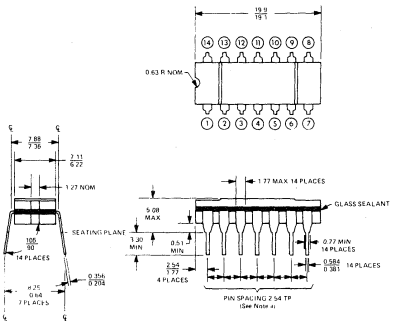




J ceramic dual-in-line packages (metric dimensions, see page 51 for inch dimensions)

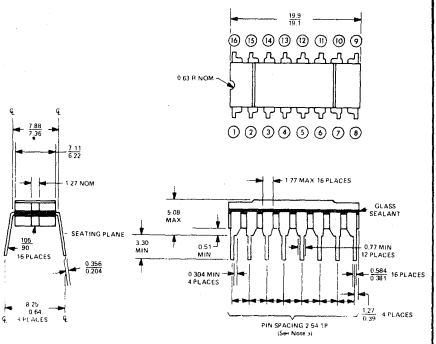
These hermetically sealed, dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 24-lead frame. The circuit bar is alloy-mounted to the base and hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 7.62-mm (or 15.24-mm) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE

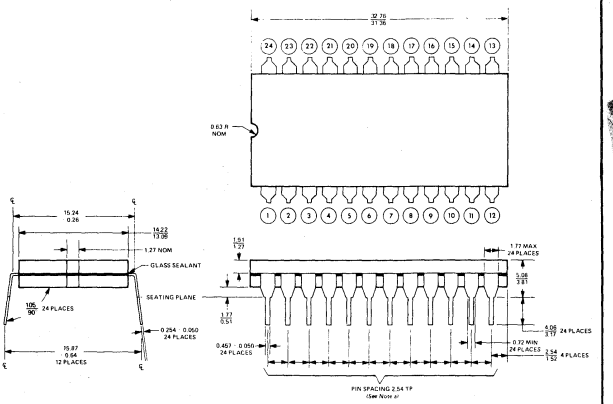


Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE

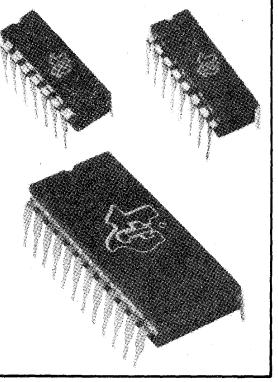


24-PIN J CERAMIC
DUAL-IN-LINE PACKAGE OUTLINE



Falls Within JEDEC MO-015AA Dimensions

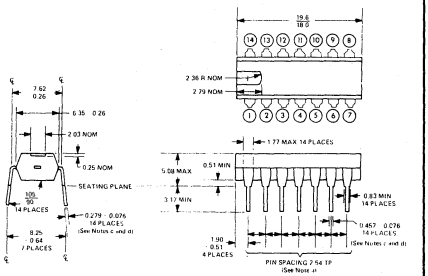
NOTES:
a. Each pin centerline is located within 0.26 mm of its true longitudinal position.
b. All dimensions are in millimeters unless otherwise noted.



N plastic dual-in-line packages (metric dimensions, see page 52 for inch dimensions)

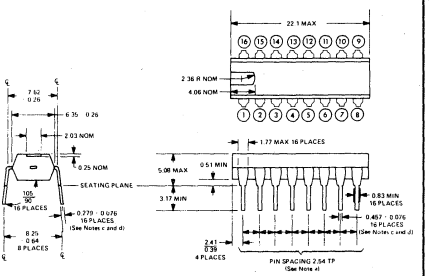
These dual-in-line packages consist of a circuit mounted on a 14-, 16-, or 24-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7.62-mm (or 15.24-mm) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads (–00) require no additional cleaning or processing when used in soldered assembly.

14-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE

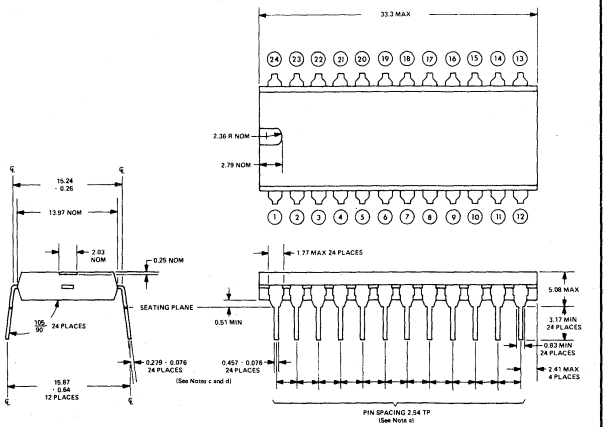


Falls Within JEDEC TO-116 and
MO 001AA Dimensions

16-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE

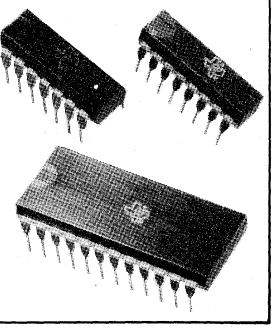


24-PIN N PLASTIC
DUAL-IN-LINE PACKAGE OUTLINE



NOTES:

a. Each pin centerline is located within 0.26 mm of its true longitudinal position.
b. All dimensions are in millimeters unless otherwise noted.
c. This dimension does not apply for solder-dipped leads.
d. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0.5 mm above the seating plane.



54/74 Family SSI Circuits

2

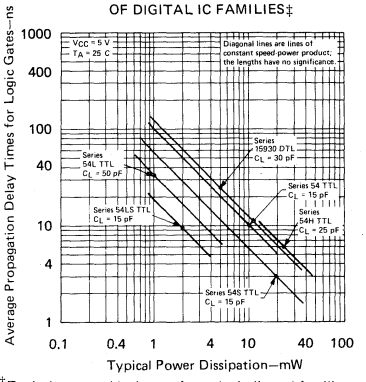
54/74 FAMILIES OF COMPATIBLE TTL CIRCUITS

description

Texas Instruments transistor-transistor-logic (TTL) family of high-performance bipolar digital integrated circuits comprises five distinct series of compatible product lines. These product lines offer the digital systems designer a full spectrum of performance ranges in order to optimize system cost and performance. The available choices range from the very high performance of the Schottky-clamped† functions for systems operating typically up to 125 megahertz to low-power functions with power consumption of only one milliwatt per gate.

Typical characteristics of the five TTL series offered are shown in Table I and their respective speed/power relationships are illustrated in Figure A.

SPEED-POWER RELATIONSHIPS
OF DIGITAL IC FAMILIES‡



‡Typical saturated logic gate from the indicated families.

FIGURE A

TABLE I—54/74 FAMILY TYPICAL PERFORMANCE CHARACTERISTICS

SERIES	GATES			FLIP-FLOPS
	Speed-Power Product	Propagation Delay Time	Power Dissipation	Clock Input Frequency Range
54LS/74LS	19 pJ	9.5 ns	2 mW	dc to 45 MHz
54L/74L	33 pJ	33 ns	1 mW	dc to 3 MHz
54S/74S	57 pJ	3 ns	19 mW	dc to 125 MHz
54/74	100 pJ	10 ns	10 mW	dc to 35 MHz
54H/74H	132 pJ	6 ns	22 mW	dc to 50 MHz

features

EASE OF SYSTEM DESIGN

- Full compatibility provides choice from five distinct performance ranges
- Broad range of functions are offered in each series
- Diode-clamped inputs are provided on all high-performance functions
- Terminated, controlled-impedance lines not normally required with TTL
- Low output impedance:
  Provides low a-c noise susceptibility
  Drives high-capacity loads
- Output-drive capability (fan-out):
  Comprehends driving mixed loads
  Most are rated for double fan-out to high-level loads for driving unused inputs

FULL COMPATIBILITY IS DESIGNED INTO TI TTL

- All series are designed for single 5-volt power supply
- All series provide one-volt or greater typical d-c noise margins
- Power dissipation relatively insensitive to operating frequency
- Switching times are guaranteed at full d-c loading
- Compatible with most logic families such as DTL, MOS, CMOS

†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	54 FAMILY / 74 FAMILY	SERIES 54 SERIES 54H / SERIES 74 SERIES 74H	SERIES 54L / SERIES 74L	SERIES 54LS / SERIES 74LS WITH DIODE INPUTS	SERIES 54LS / SERIES 74LS WITH EMITTER INPUTS	SERIES 54S / SERIES 74S	UNIT
Supply voltage, V_{CC} (see Note 1)		7	8	7	7	7	V
Input voltage		5.5	5.5	7	5.5	5.5	V
Interemitter voltage (see Note 2)		5.5	5.5		5.5	5.5	V
Off-state (high-level) voltage applied to open-collector outputs	'06, '07	30					V
	'16, '17, '26	15					
	Others		8	7	7	7	
Operating free-air temperature range	54 Family	−55 to 125					°C
	74 Family	0 to 70					
Storage temperature range		−65 to 150					°C

NOTES: 1. Voltage values, unless otherwise noted, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these SSI circuits, this rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.

unused inputs of positive-AND/NAND gates

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a voltage greater than V_{OH} min (see tables of electrical characteristics), but not to exceed the absolute maximum rating. This eliminates the distributed capacitance associated with the floating input, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling unused inputs are:

a. Connect unused inputs to an independent supply voltage. Preferably, this voltage should be between V_{OH} min and 4.5 V. Series 54LS/74LS devices with diode inputs may be connected directly to V_{CC}.

b. Connect unused inputs to a used input if maximum drive capability of the driving output will not be exceeded. Each additional input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the input maximum rating should occur, the impedance will be high enough to protect the input. One to 25 unused inputs may be connected to each 1-kΩ resistor. Series 54LS/74LS devices with diode inputs may be connected directly to V_{CC}.

d. Connect unused inputs to any fixed-high-level compatible output such as the output of an inverter or NAND gate that has its input(s) grounded. Maximum high-level drive capability of the output should not be exceeded.

input-current requirements

Input-current requirements reflect worst-case conditions over the specified recommended operating free-air temperature and V_{CC} ranges. The table below shows maximum input current requirements and nominal base resistor values for standard loads in each TTL series. A standard load is defined as an input connected to a single emitter or diode that is associated with a pull-up resistor having the value indicated in the table. However, some inputs are tied to more than one input transistor (or diode), or the base-resistor values of some inputs have been changed either to reduce input-current requirements or to improve performance. Therefore, the input-current requirements may vary. Consult the electrical characteristics table for the particular device type to determine the input-current requirements of each input.

STANDARD INPUTS (ONE LOAD)

SERIES	NOMINAL VALUE OF INPUT PULL-UP RESISTOR	MAXIMUM HIGH-LEVEL INPUT CURRENT	MAXIMUM LOW-LEVEL INPUT CURRENT
54/74	4 kΩ	40 μA	−1.6 mA
54H/74H	2.8 kΩ	50 μA	−2 mA
54L/74L‡	40 kΩ	10 μA	−0.18 mA
	8 kΩ	20 μA	−0.8 mA
54LS/74LS	25 kΩ	20 μA	−0.36 mA
54S/74S	2.8 kΩ	50 μA	−2 mA

‡Series 54L/74L has two different types of standard inputs as shown.

Since low-level input current is primarily a function of the input base resistor, two or more inputs of the same NAND or AND gate may be tied together and still be considered one load at a low logic level, but at a high logic level, each input is an additional load.

Currents into input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

drive capability

The maximum value of I_{OL} given under "recommended operating conditions" reflects the ability of an output to sink current from a number of loads at a low voltage level and maximum I_{OH} reflects the ability to supply current at a high voltage level. Each standard output at a low level is capable of sinking current from 10 standard loads of its own series, and at a high level is capable of supplying current to either 10 or 20 loads of its own series. The fan-out of 20 at a high logic level makes it possible to tie as many as 10 unused inputs of NAND or AND gates to used inputs of the same gates (as mentioned under input-current requirements) without exceeding the fan-out capability of the output driving 10 used inputs. Certain outputs are designed for special applications and have greater or lesser drive capability. See the recommended operating conditions for each type.

The loads may be intermixed in any desired combination so long as the load totals for I_{IH} and I_{IL} are less than the maximum recommended values of I_{OH} and I_{OL}, respectively, for the driving circuit.

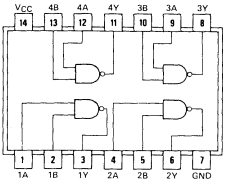
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

00

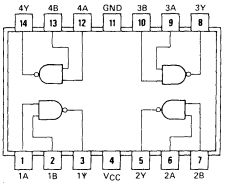
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 86



SN5400/SN7400(J, N)
SN54H00/SN74H00(J, N)
SN54L00/SN74L00(J, N)
SN54LS00/SN74LS00(J, N, W)
SN54S00/SN74S00(J, N, W)



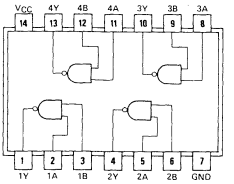
SN5400/SN7400(W)
SN54H00/SN74H00(W)
SN54L00/SN74L00(T)

01

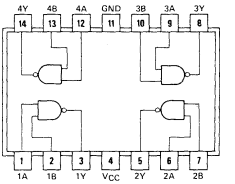
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

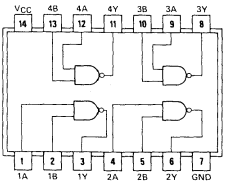
See page 88



SN5401/SN7401(J, N)
SN54LS01/SN74LS01(J, N, W)



SN5401/SN7401(W)
SN54H01/SN74H01(W)
SN54L01/SN74L01(T)



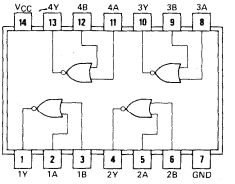
SN54H01/SN74H01(J, N)

02

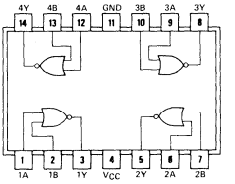
QUADRUPLE 2-INPUT
POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B}$

See page 92



SN5402/SN7402(J, N)
SN54L02/SN74L02(J, N)
SN54LS02/SN74LS02(J, N, W)
SN54S02/SN74S02(J, N, W)



SN5402/SN7402(W)
SN54L02/SN74L02(T)

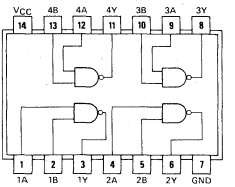
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

03

QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

See page 88



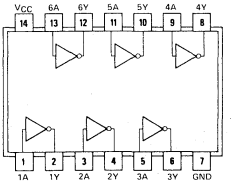
SN5403/SN7403(J, N)
SN54L03/SN74L03(J, N)
SN54LS03/SN74LS03(J, N, W)
SN54S03/SN74S03(J, N, W)

04

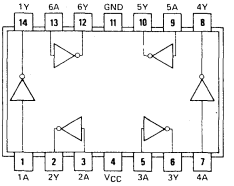
HEX INVERTERS

positive logic:
$Y = \overline{A}$

See page 86



SN5404/SN7404(J, N)
SN54H04/SN74H04(J, N)
SN54L04/SN74L04(J, N)
SN54LS04/SN74LS04(J, N, W)
SN54S04/SN74S04(J, N, W)



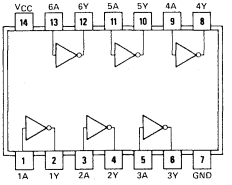
SN5404/SN7404(W)
SN54H04/SN74H04(W)
SN54L04/SN74L04(T)

05

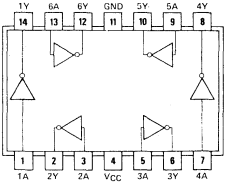
HEX INVERTERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A}$

See page 88



SN5405/SN7405(J, N)
SN54H05/SN74H05(J, N)
SN54LS05/SN74LS05(J, N, W)
SN54S05/SN74S05(J, N, W)



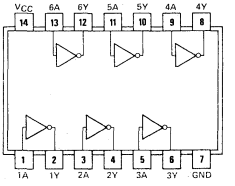
SN5405/SN7405(W)
SN54H05/SN74H05(W)

06

HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106



SN5406/SN7406(J, N, W)

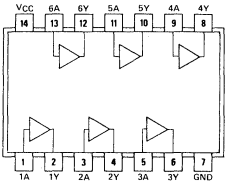
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

07

HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
Y = A

See page 106



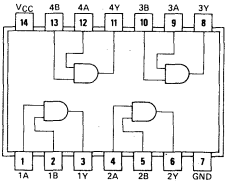
SN5407/SN7407(J, N, W)

08

QUADRUPLE 2-INPUT
POSITIVE-AND GATES

positive logic:
Y = AB

See page 94



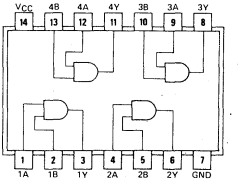
SN5408/SN7408(J, N, W)
SN54LS08/SN74LS08(J, N, W)

09

QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
Y = AB

See page 96



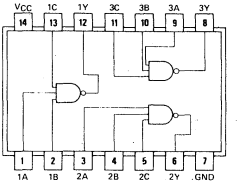
SN5409/SN7409(J, N, W)
SN54LS09/SN74LS09(J, N, W)

10

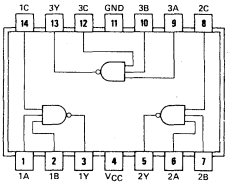
TRIPLE 3-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABC}$

See page 86



SN5410/SN7410(J, N)
SN54H10/SN74H10(J, N)
SN54L10/SN74L10(J, N)
SN54LS10/SN74LS10(J, N, W)
SN54S10/SN74S10(J, N, W)



SN5410/SN7410(W)
SN54H10/SN74H10(W)
SN54L10/SN74L10(T)

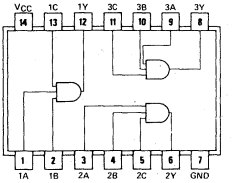
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

11

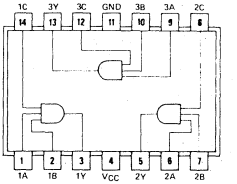
TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:
$Y = ABC$

See page 94



SN54H11/SN74H11(J, N)
SN54LS11/SN74LS11(J, N, W)
SN54S11/SN74S11(J, N, W)



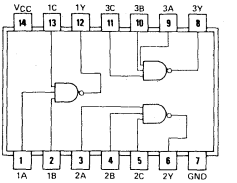
SN54H11/SN74H11(W)

12

TRIPLE 3-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{ABC}$

See page 88



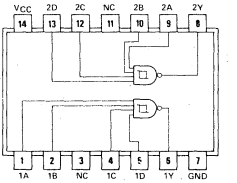
SN5412/SN7412(J, N, W)

13

DUAL 4-INPUT POSITIVE-NAND SCHMITT TRIGGERS

positive logic:
$Y = \overline{ABCD}$

See page 98



SN5413/SN7413(J, N, W)

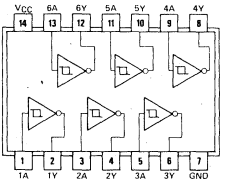
NC—No internal connection

14

HEX SCHMITT-TRIGGER INVERTERS

positive logic:
$Y = \overline{A}$

See page 98



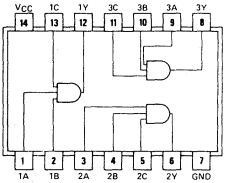
SN5414/SN7414(J, N, W)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

15
TRIPLE 3-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = ABC$

See page 96

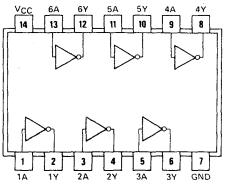


SN54H15/SN74H15(J, N, W)
SN54LS15/SN74LS15(J, N, W)
SN54S15/SN74S15(J, N, W)

16
HEX INVERTER BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = \overline{A}$

See page 106

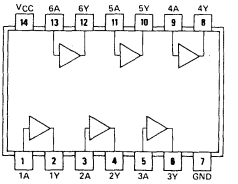


SN5416/SN7416(J, N, W)

17
HEX BUFFERS/DRIVERS
WITH OPEN-COLLECTOR
HIGH-VOLTAGE OUTPUTS

positive logic:
$Y = A$

See page 106

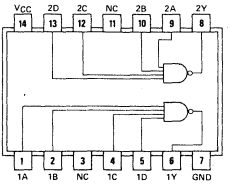


SN5417/SN7417(J, N, W)

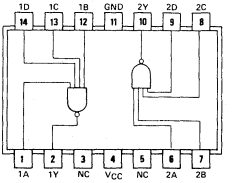
20
DUAL 4-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCD}$

See page 86



SN5420/SN7420(J, N)
SN54H20/SN74H20(J, N)
SN54L20/SN74L20(J, N)
SN54LS20/SN74LS20(J, N, W)
SN54S20/SN74S20(J, N, W)



SN5420/SN7420(W)
SN54H20/SN74H20(W)
SN54L20/SN74L20(T)

NC—No internal connection

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

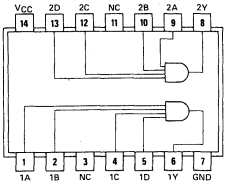
21

DUAL 4-INPUT POSITIVE-AND GATES

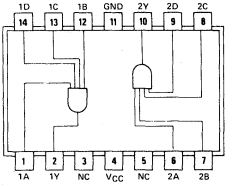
positive logic:

$Y = ABCD$

See page 94



SN54H21/SN74H21(J, N)
SN54LS21/SN74LS21(J, N, W)



SN54H21/SN74H21 (W)

NC—No internal connection

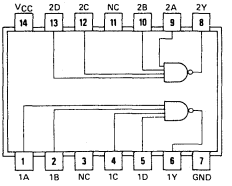
22

DUAL 4-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

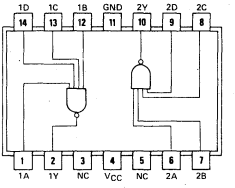
positive logic:

$Y = \overline{ABCD}$

See page 88



SN5422/SN7422(J, N, W)
SN54H22/SN74H22(J, N)
SN54LS22/SN74LS22(J, N, W)
SN54S22/SN74S22(J, N, W)



SN54H22/SN74H22(W)

NC—No internal connection

23

EXPANDABLE DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

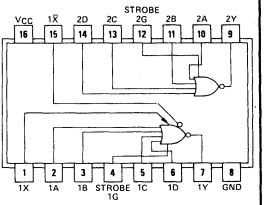
positive logic:

$1Y = \overline{1G(1A+1B+1C+1D)+X}$

$2Y = \overline{2G(2A+2B+2C+2D)}$

X = output of SN5460/SN7460

See page 113



SN5423/SN7423 (J, N, W)

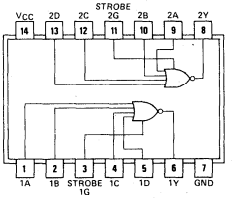
25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

$Y = \overline{G(A+B+C+D)}$

See page 92



SN5425/SN7425 (J, N, W)

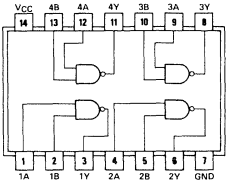
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

26

QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES

positive logic:
$Y = \overline{AB}$

See page 106



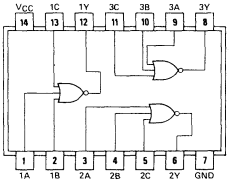
SN5426/SN7426(J, N)

27

TRIPLE 3-INPUT
POSITIVE-NOR GATES

positive logic:
$Y = \overline{A+B+C}$

See page 92



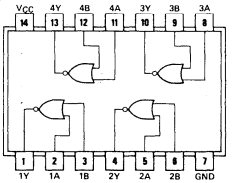
SN5427/SN7427(J, N, W)
SN54LS27/SN74LS27(J, N, W)

28

QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS

positive logic:
$Y = \overline{A+B}$

See page 102



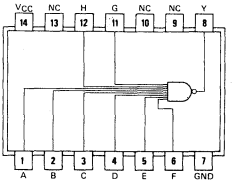
SN5428/SN7428(J, N, W)
SN54LS28/SN74LS28(J, N, W)

30

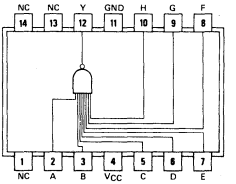
8-INPUT
POSITIVE-NAND GATES

positive logic:
$Y = \overline{ABCDEFGH}$

See page 86



SN5430/SN7430(J, N)
SN54H30/SN74H30(J, N)
SN54L30/SN74L30(J, N)
SN54LS30/SN74LS30(J, N, W)
SN54S30/SN74S30(J, N, W)



SN5430/SN7430(W)
SN54H30/SN74H30(W)
SN54L30/SN74L30(T)

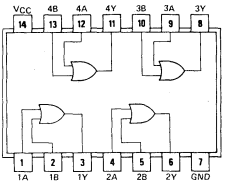
NC—No internal connection

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

32
QUADRUPLE 2-INPUT
POSITIVE-OR GATES

positive logic:
$Y = A+B$

See page 108

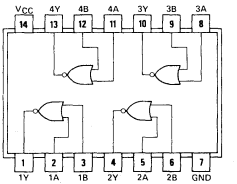


SN5432/SN7432(J, N, W)
SN54LS32/SN74LS32(J, N, W)

33
QUADRUPLE 2-INPUT
POSITIVE-NOR BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{A+B}$

See page 106

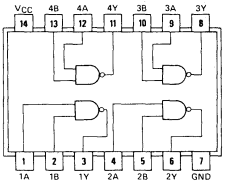


SN5433/SN7433(J, N, W)
SN54LS33/SN74LS33(J, N, W)

37
QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS

positive logic:
$Y = \overline{AB}$

See page 102

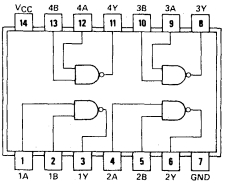


SN5437/SN7437(J, N, W)
SN54LS37/SN74LS37(J, N, W)

38
QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS

positive logic:
$Y = \overline{AB}$

See page 106



SN5438/SN7438(J, N, W)
SN54LS38/SN74LS38(J, N, W)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

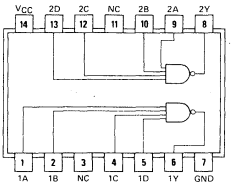
40

DUAL 4-INPUT POSITIVE-NAND BUFFERS

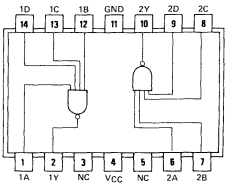
positive logic:

$Y = \overline{ABCD}$

See page 102



SN5440/SN7440(J, N)
SN54H40/SN74H40(J, N)
SN54LS40/SN74LS40(J, N, W)
SN54S40/SN74S40(J, N, W)



SN5440/SN7440(W)
SN54H40/SN74H40(W)

NC—No internal connection

50

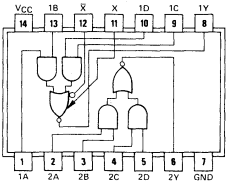
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

positive logic:

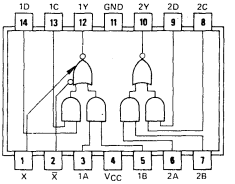
$Y = \overline{AB+CD+X}$

'50: X = output of SN5460/SN7460
'H50: X = output of SN54H60/SN74H60 or SN54H62/SN74H62

See page 113



SN5450/SN7450(J, N)
SN54H50/SN74H50(J, N)



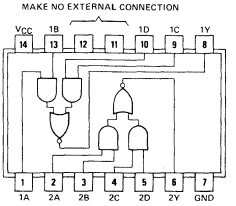
SN5450/SN7450(W)
SN54H50/SN74H50(W)

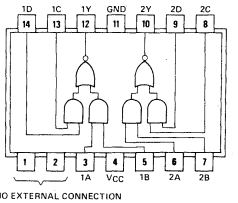
51

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES

'51, 'H51, 'S51
positive logic:

$Y = \overline{AB+CD}$





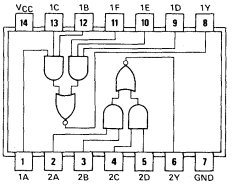
SN5451/SN7451(J, N)
SN54H51/SN74H51(J, N)
SN54S51/SN74S51(J, N, W)

SN5451/SN7451(W)
SN54H51/SN74H51(W)

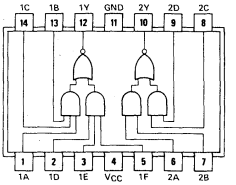
'L51, 'LS51
positive logic:

$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$
$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$

See page 110



SN54L51/SN74L51(J, N)
SN54LS51/SN74LS51(J, N, W)



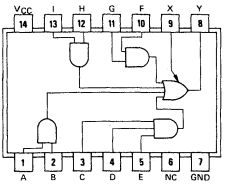
SN54L51/SN74L51(T)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

52

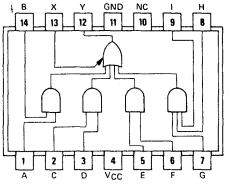
EXPANDABLE 4-WIDE AND-OR GATES

'H52(J, N)
positive logic:
Y = AB+CDE+FG+HI+X
X = output of SN54H61/SN74H61



SN54H52/SN74H52(J, N)

'H52(W)
positive logic:
Y = AB+CD+EF+GHI+X
X = output of SN54H61/SN74H61



SN54H52/SN74H52(W)

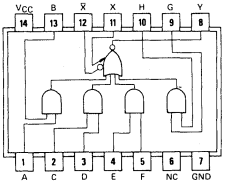
See page 113

NC—No internal connection

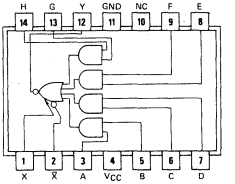
53

EXPANDABLE 4-WIDE AND-OR-INVERT GATES

'53
positive logic:
$Y = \overline{AB+CD+EF+GH+X}$
X = output of SN5460/SN7460

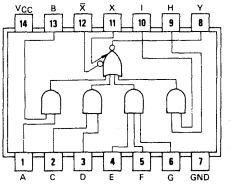


SN5453/SN7453(J, N)

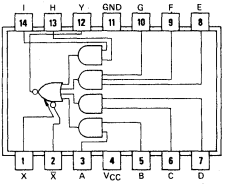


SN5453/SN7453(W)

'H53
positive logic:
Y = AB+CD+EFG+HI+X
X = output of SN54H60/SN74H60
or SN54H62/SN74H62



SN54H53/SN74H53(J, N)



SN54H53/SN74H53(W)

See page 113

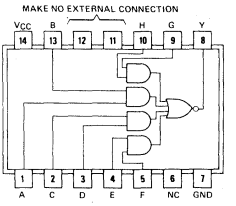
NC—No internal connection

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

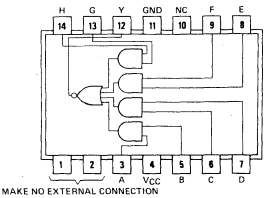
54

4-WIDE AND-OR-INVERT GATES

'54
positive logic:
$Y = \overline{AB+CD+EF+GH}$

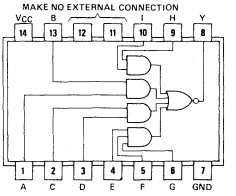


SN5454/SN7454(J, N)

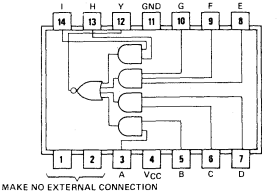


SN5454/SN7454(W)

'H54
positive logic:
$Y = \overline{AB+CD+EFG+HI}$

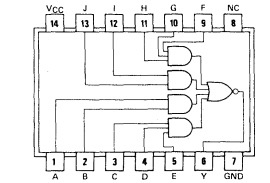


SN54H54/SN74H54(J, N)



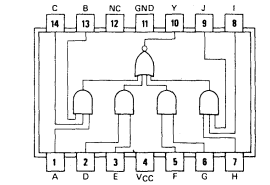
SN54H54/SN74H54(W)

'L54(J, N), 'LS54
positive logic:
$Y = \overline{AB+CDE+FGH+IJ}$



SN54L54/SN74L54(J, N)
SN54LS54/SN74LS54(J, N, W)

'L54(T)
positive logic:
$Y = \overline{ABC+DE+FG+HIJ}$



SN54L54/SN74L54(T)

See page 110

NC—No internal connection

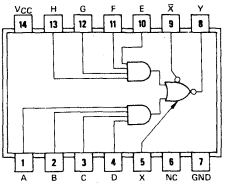
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

55

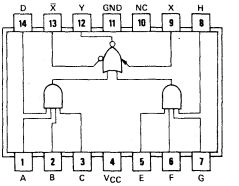
2-WIDE 4-INPUT AND-OR-INVERT GATES

'H55 (EXPANDABLE)
positive logic:
$Y = \overline{ABCD+EFGH+X}$
X = output of SN54H60/SN74H60 or SN54H62/SN74H62

See page 113



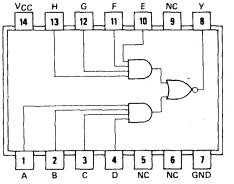
SN54H55/SN74H55(J, N)



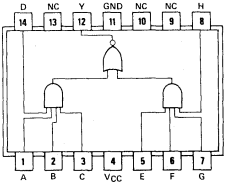
SN54H55/SN74H55(W)

'L55, 'LS55
positive logic:
$Y = \overline{ABCD+EFGH}$

See page 110



SN54L55/SN74L55(J, N)
SN54LS55/SN74LS55(J, N, W)

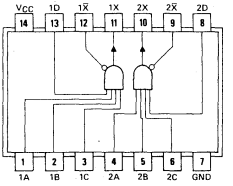


SN54L55/SN74L55(T)
NC—No internal connection

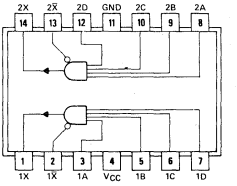
60

DUAL 4-INPUT EXPANDERS
'60
positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN5423/SN7423, SN5450/SN7450, or SN5453/SN7453
'H60
positive logic:
X = ABCD when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55

See pages 117 and 118



SN5460/SN7460(J, N)
SN54H60/SN74H60(J, N)



SN5460/SN7460(W)
SN54H60/SN74H60(W)

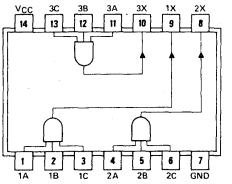
NC—No internal connection

61

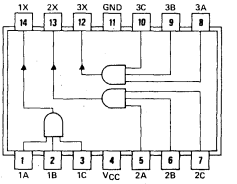
TRIPLE 3-INPUT EXPANDERS

positive logic:
X = ABC when connected to X input of SN54H52/SN74H52

See page 119



SN54H61/SN74H61(J, N)



SN54H61/SN74H61(W)

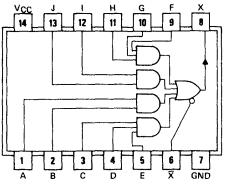
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

62

4-WIDE AND-OR EXPANDER

'H62(J, N) (2-3-3-2 INPUT)
positive logic:

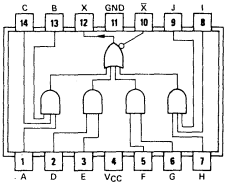
X = AB+CDE+FGH+IJ when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55



SN54H62/SN74H62(J, N)

'H62(W) (3-2-2-3 INPUT)
positive logic:

X = ABC+DE+FG+HIJ when connected to X and $\overline{X}$ inputs of SN54H50/SN74H50, SN54H53/SN74H53, or SN54H55/SN74H55



SN54H62/SN74H62(W)

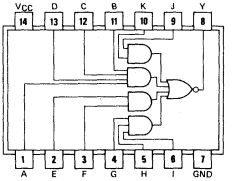
See page 118

64

4-2-3-2-INPUT AND-OR-INVERT GATES

positive logic:

$Y = \overline{ABCD+EF+GHI+JK}$



SN54S64/SN74S64(J, N, W)

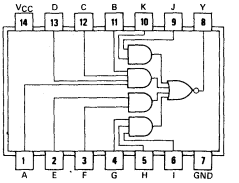
See page 110

65

4-2-3-2-INPUT AND-OR-INVERT GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

$Y = \overline{ABCD+EF+GHI+JK}$



SN54S65/SN74S65(J, N, W)

See page 112

FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

70

AND-GATED J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

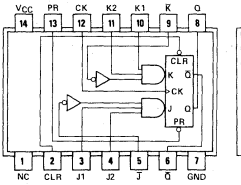
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	Q_0	$\bar{Q}_0$
H	H	↑	H	L	H	L
H	H	↑	L	H	L	H
H	H	↑	H	H	TOGGLE	
H	H	L	X	X	Q_0	$\bar{Q}_0$

positive logic: $J = J1 \cdot J2 \cdot \bar{J}$

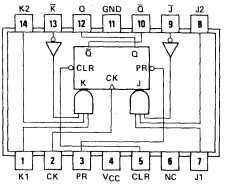
$K = K1 \cdot K2 \cdot \bar{K}$

If inputs $\bar{J}$ and $\bar{K}$ are not used, they must be grounded.

See page 120



SN5470/SN7470(J, N)



SN5470/SN7470(W)

NC—No internal connection

H71

AND-OR-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET

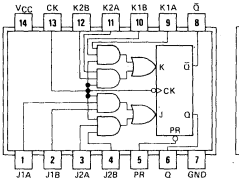
FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

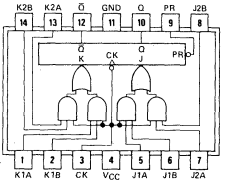
positive logic: $J = (J1A \cdot J1B) + (J2A \cdot J2B)$

$K = (K1A \cdot K1B) + (K2A \cdot K2B)$

See page 124



SN54H71/SN74H71(J, N)



SN54H71/SN74H71(W)

L71

AND-GATED R-S MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

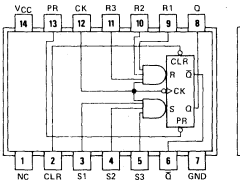
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	INDETERMINATE	

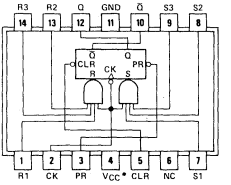
positive logic: $R = R1 \cdot R2 \cdot R3$

$S = S1 \cdot S2 \cdot S3$

See page 128



SN54L71/SN74L71(J, N)



SN54L71/SN74L71(T)

NC—No internal connection

H = high level (steady state), L = low level (steady state), X = irrelevant

↑ = transition from low to high level.

⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

72

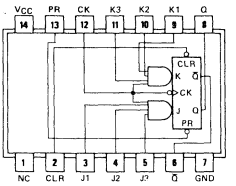
AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

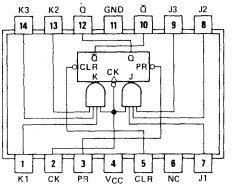
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⊓	L	L	Q_0	$\bar{Q}_0$
H	H	⊓	H	L	H	L
H	H	⊓	L	H	L	H
H	H	⊓	H	H	TOGGLE	

positive logic: $J = J1 \cdot J2 \cdot J3$; $K1 \cdot K2 \cdot K3$

See pages 120, 124, and 128



SN5472/SN7472(J, N)
SN54H72/SN74H72(J, N)
SN54L72/SN74L72(J, N)



SN5472/SN7472(W)
SN54H72/SN74H72(W)
SN54L72/SN74L72(T)

NC—No internal connection

73

DUAL J-K FLIP-FLOPS WITH CLEAR

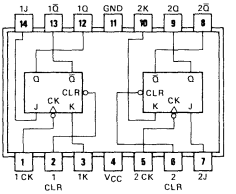
'73, 'H73, 'L73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⊓	L	L	Q_0	$\bar{Q}_0$
H	⊓	H	L	H	L
H	⊓	L	H	L	H
H	⊓	H	H	TOGGLE	

'LS73
FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

See pages 120, 124, 128, and 130



SN5473/SN7473(J, N, W)
SN54H73/SN74H73(J, N, W)
SN54L73/SN74L73(J, N, T)
SN54LS73/SN74LS73(J, N, W)

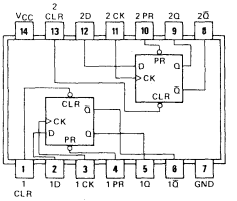
74

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

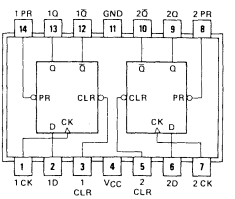
FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

See pages 120, 124, 128, 130, and 132



SN5474/SN7474(J, N)
SN54H74/SN74H74(J, N)
SN54L74/SN74L74(J, N)
SN54LS74/SN74LS74(J, N, W)
SN54S74/SN74S74(J, N, W)



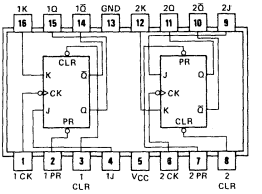
SN5474/SN7474(W)
SN54H74/SN74H74(W)
SN54L74/SN74L74(T)

H = high level (steady state), L = low level (steady state), X = irrelevant
⊓ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
↑ = transition from low to high level, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

76

DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR



SN5476/SN7476(J, N, W)
SN54H76/SN74H76(J, N, W)
SN54LS76/SN74LS76(J, N, W)

'76, 'H76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

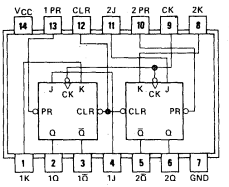
'LS76
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

See pages 120, 124, and 130

78

DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

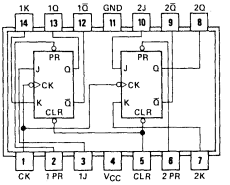


SN54H78/SN74H78(J, N, W)

'H78, 'L78
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

See pages 124 and 128



SN54L78/SN74L78(J, N, T)
SN54LS78/SN74LS78(J, N, W)

'LS78
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

See page 130

H = high level (steady state), L = low level (steady state), X = irrelevant
⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) state.

FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

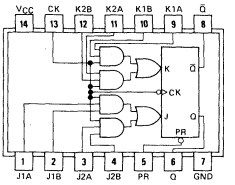
101

AND-OR-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

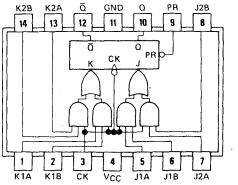
FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

positive logic: J = (J1A•J1B)+(J2A•J2B)
K = (K1A•K1B)+(K2A•K2B)



SN54H101/SN74H101(J, N)



SN54H101/SN74H101(W)

See page 126

2

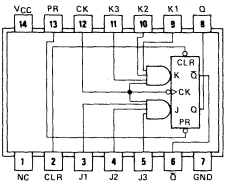
102

AND-GATED J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

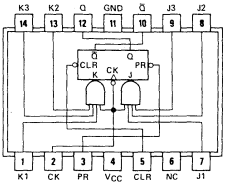
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

positive logic: J = J1•J2•J3
K = K1•K2•K3



SN54H102/SN74H102(J, N)



SN54H102/SN74H102(W)

See page 126

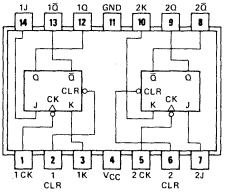
NC—No internal connection

103

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54H103/SN74H103(J, N, W)

See page 126

H = high level (steady state), L = low level (steady state), X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

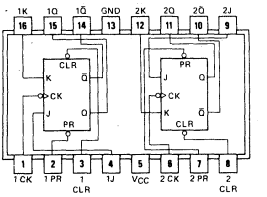
FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

106

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54H106/SN74H106(J, N, W)

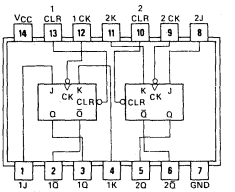
See page 126

107

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH CLEAR

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	



SN54107/SN74107(J, N)

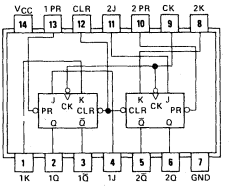
See page 120

108

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54H108/SN74H108(J, N, W)

See page 126

H = high level (steady state), L = low level (steady state), X = irrelevant
↓ = transition from high to low level
⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

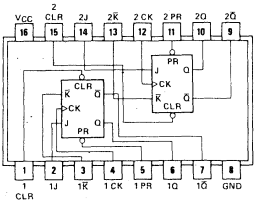
FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

109

DUAL J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$



SN54109/SN74109(J, N, W)
SN54LS109/SN74LS109(J, N, W)

See pages 120 and 130

2

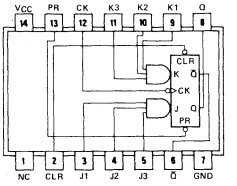
110

AND-GATED J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

positive logic: J = J1•J2•J3
K = K1•K2•K3



SN54110/SN74110(J, N, W)

See page 120

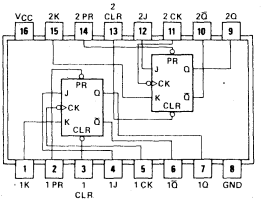
NC—No internal connection

111

DUAL J-K MASTER-SLAVE FLIP-FLOPS WITH DATA LOCKOUT

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	



SN54111/SN74111(J, N, W)

See page 120

H = high level (steady state), L = low level (steady state), X = irrelevant, ↑ = transition from low to high level
⎍ = high-level pulse; while the clock is high, changes at the J and K inputs after the specified hold time have no effect. Data is transferred to output on the falling edge of the pulse.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

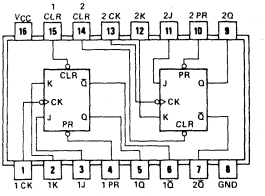
FLIP-FLOPS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

112

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS112/SN74LS112(J, N, W)
SN54S112/SN74S112(J, N, W)

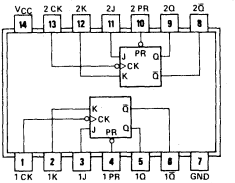
See pages 130 and 132

113

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS113/SN74LS113(J, N, W)
SN54S113/SN74S113(J, N, W)

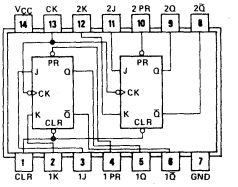
See pages 130 and 132

114

DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$



SN54LS114/SN74LS114(J, N, W)
SN54S114/SN74S114(J, N, W)

See pages 130 and 132

H = high level (steady state), L = low level (steady state), X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

MONOSTABLE MULTIVIBRATORS . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

MONOSTABLE MULTIVIBRATORS

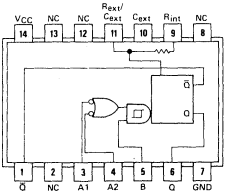
121

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	$\bar{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

See page 134

See Notes



SN54121/SN74121(J, N, W)
SN54L121/SN74L121(J, N, T)
'121 . . . R_{int} = 2 kΩ NOM
'L121 . . . R_{int} = 4 kΩ NOM

NC—No internal connection

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

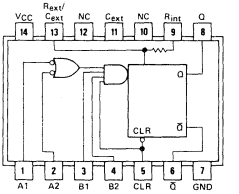
122

FUNCTION TABLE

INPUTS					OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

See page 138

See Notes



SN54122/SN74122(J, N, W)
SN54L122/SN74L122(J, N, T)
'122 . . . R_{int} = 10 kΩ NOM
'L122 . . . R_{int} = 20 kΩ NOM

NC—No internal connection

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

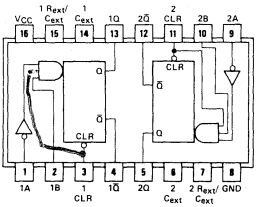
123

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

See page 138

See Notes



SN54123/SN74123(J, N, W)
SN54L123/SN74L123(J, N)

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low-level pulse, X = irrelevant (any input, including transitions).
B. To use the internal timing resistor of '121, 'L121, '122, or 'L122, connect R_{int} to V_{CC}.
C. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).
D. For accurate repeatable pulse widths, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.
E. To obtain variable pulse widths, connect external variable resistance between R_{int} or R_{ext}/C_{ext} and V_{CC}.

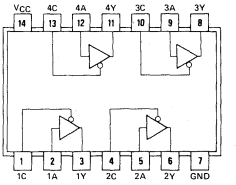
SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

125

QUADRUPLE BUS BUFFER GATES
WITH THREE-STATE OUTPUTS

positive logic:
Y = A
Output is off (disabled) when C is high.

See page 142



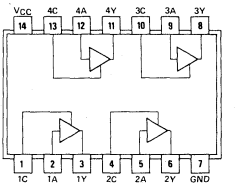
SN54125/SN74125(J, N, W)

126

QUADRUPLE BUS BUFFER GATES
WITH THREE-STATE OUTPUTS

positive logic:
Y = A
Output is off (disabled) when C is low.

See page 142



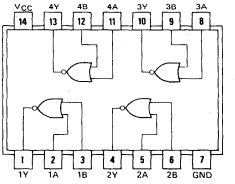
SN54126/SN74126(J, N, W)

128

SN54128 . . . 75-OHM LINE DRIVER
SN74128 . . . 50-OHM LINE DRIVER

positive logic:
$Y = \overline{A+B}$

See page 104



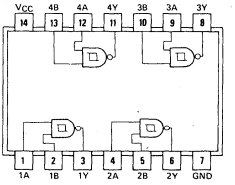
SN54128/SN74128(J, N, W)

132

QUADRUPLE 2-INPUT
POSITIVE-NAND
SCHMITT TRIGGERS

positive logic:
$Y = \overline{AB}$

See page 98



SN54132/SN74132(J, N, W)
SN54S132/SN74S132(J, N, W)

SSI GATES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEWS)

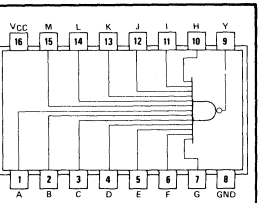
133

13-INPUT POSITIVE-NAND GATES

positive logic:

$Y = \overline{ABCDEFGHIJKLM}$

See page 86



SN54S133/SN74S133(J, N, W)

134

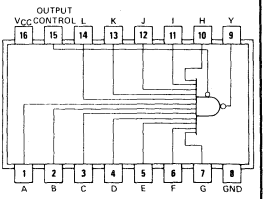
12-INPUT POSITIVE-NAND GATES
WITH THREE-STATE OUTPUTS

positive logic:

$Y = \overline{ABCDEFGHIJKL}$

Output is off (disabled) when output control is high.

See page 142



SN54S134/SN74S134(J, N, W)

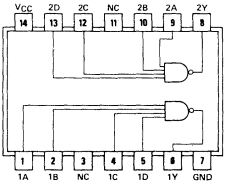
140

DUAL 4-INPUT
POSITIVE-NAND 50-OHM LINE DRIVERS

positive logic:

$Y = \overline{ABCD}$

See page 104



SN54S140/SN74S140(J, N, W)

NC—No internal connection

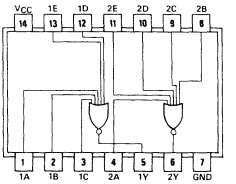
260

DUAL 5-INPUT
POSITIVE-NOR GATES

positive logic:

$Y = \overline{A+B+C+D+E}$

See page 92



SN54S260/SN74S260(J, N, W)

LATCHES . . . LOGIC AND PIN ASSIGNMENTS (TOP VIEW)

279

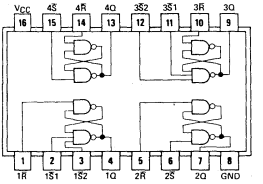
QUADRUPLE $\overline{S}$-$\overline{R}$ LATCHES

FUNCTION TABLE

INPUTS $\overline{S}$†	INPUTS $\overline{R}$	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level
L = low level
Q_0 = the level of Q before the indicated input conditions were established.
*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.
†For latches with double $\overline{S}$ inputs:
H = both $\overline{S}$ inputs high
L = one or both $\overline{S}$ inputs low

See page 141



SN54279/SN74279(J, N, W)

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−500			−100			−400			−1000	μA
	74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			20			2			4			20	mA
	74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '00, '04, '10, '20, '30			SERIES 54H SERIES 74H 'H00, 'H04, 'H10, 'H20, 'H30			SERIES 54L SERIES 74L 'L00, 'L04, 'L10, 'L20, 'L30			SERIES 54LS SERIES 74LS 'LS00, 'LS04, 'LS10, 'LS20, 'LS30			SERIES 54S SERIES 74S 'S00, 'S04, 'S10, 'S20, 'S30, 'S133			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.7			0.8	V
				74 Family			0.8			0.8			0.7			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §			*−1.5			*−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.5		2.4	3.3		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.5		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			0.1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50			10							μA
				V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V									−0.18							mA
				V_{IL} = 0.4 V, 'LS30												−0.4				
				V_{IL} = 0.4 V, Others			−1.6			−2						−0.36				
				V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−3		−15	−6		−40	−40		−100	mA
				74 Family	−18		−55	−40		−100	−3		−15	−5		−42	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of short-circuit should not exceed 1 second.
*The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts date-coded 7332 or higher.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'00	4	8	12	22	2
'04	6	12	18	33	2
'10	3	6	9	16.5	2
'20	2	4	6	11	2
'30	1	2	3	6	2
'H00	10	16.8	26	40	4.5
'H04	16	26	40	58	4.5
'H10	7.5	12.6	19.5	30	4.5
'H20	5	8.4	13	20	4.5
'H30	2.5	4.2	6.5	10	4.5
'L00	0.44	0.8	1.16	2.04	0.20
'L04	0.66	1.2	1.74	3.06	0.20
'L10	0.33	0.6	0.87	1.53	0.20
'L20	0.22	0.4	0.58	1.02	0.20
SN54L30	0.11	0.33	0.29	0.51	0.20
SN74L30	0.11	0.2	0.29	0.51	0.20
'LS00	0.8	1.6	2.4	4.4	0.4
'LS04	1.2	2.4	3.6	6.6	0.4
'LS10	0.6	1.2	1.8	3.3	0.4
'LS20	0.4	0.8	1.2	2.2	0.4
'LS30	0.35	0.5	0.6	1.1	0.48
'S00	10	16	20	36	3.75
'S04	15	24	30	54	3.75
'S10	7.5	12	15	27	3.75
'S20	5	8	10	18	3.75
'S30	3	5	5.5	10	4.25
'S133	3	5	5.5	10	4.25

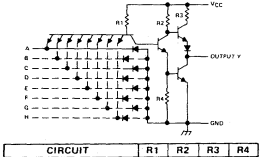
switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'00, '10	C_L = 15 pF, R_L = 400 Ω		11	22		7	15
'04, '20			12	22		8	15
'30			13	22		8	15
'H00	C_L = 25 pF, R_L = 280 Ω		5.9	10		6.2	10
'H04			6	10		6.5	10
'H10			5.9	10		6.3	10
'H20			6	10		7	10
'H30			6.8	10		8.9	12
'L00, 'L04, 'L10, L20	C_L = 50 pF, R_L = 4 kΩ		35	60		31	60
'L30			35	60		70	100
'LS00, 'LS04 'LS10, 'LS20	C_L = 15 pF, R_L = 2 kΩ		9	20		10	20
'LS30			9	20		25	35
'S00, 'S04	C_L = 15 pF, R_L = 280 Ω	2	3	4.5	2	3	5
'S10, 'S20	C_L = 50 pF, R_L = 280 Ω		4.5			5	
'S30, 'S133	C_L = 15 pF, R_L = 280 Ω	2	4	6	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω		5.5			6.5	

#Load circuits and voltage waveforms are shown on pages 148 and 149.

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

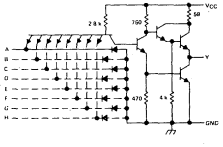
schematics (each gate)



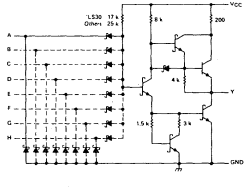
CIRCUIT	R1	R2	R3	R4
'00, '04, '10, '20, '30	4 k	1.6 k	130	1 k
'L00, 'L04, 'L10, 'L20, 'L30	40 k	20 k	500	12 k

'00, '04, '10, '20, '30
'L00, 'L04, 'L10, 'L20, 'L30, CIRCUITS

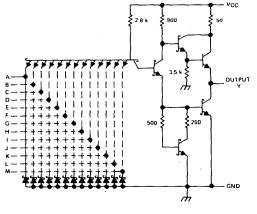
Input clamp diodes not on SN54L'/SN74L' circuits.



'H00, 'H04, 'H10, 'H20, 'H30 CIRCUITS



'LS00, 'LS04, 'LS10, 'LS20, 'LS30 CIRCUITS



S00, 'S04, 'S10, 'S20, 'S30, 'S133 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '01, '03, '05, '12, '22			SERIES 54H SERIES 74H 'H01, 'H05, 'H22			SERIES 54L SERIES 74L 'L01, 'L03			SERIES 54LS SERIES 74LS 'LS01, 'LS03, 'LS05, 'LS22			SERIES 54S SERIES 74S 'S03, 'S05, 'S22			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}					5.5			5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}		54 Family			16			20			2			4			20	mA
		74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '01, '03, '05, '12, '22			SERIES 54H SERIES 74H 'H01, 'H05, 'H22			SERIES 54L SERIES 74L 'L01, 'L03			SERIES 54LS SERIES 74LS 'LS01, 'LS03, 'LS05, 'LS22			SERIES 54S SERIES 74S 'S03, 'S05, 'S22			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.6			0.7			0.8	V
				74 Family			0.8			0.8			0.6			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §				*−1.5			*−1.5						−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				250			250			50			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4		0.5		V
				74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5		0.5		
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			0.1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50			10							μA
				V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V									−0.18							mA
				V_{IL} = 0.4 V			−1.6			−2						−0.36				
				V_{IL} = 0.5 V															−2	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
* The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts shipped after 31 July 1973.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per Gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'01	4	8	12	22	2
'03	4	8	12	22	2
'05	6	12	18	33	2
'12	3	6	9	16.5	2
'22	2	4	6	11	2
'H01	6.8	10	26	40	4.1
'H05	16	26	40	58	4.67
'H22	3.4	5	13	20	4.1
'L01	0.44	0.8	1.16	2.04	0.20
'L03	0.44	0.8	1.16	2.04	0.20
'LS01	0.8	1.6	2.4	4.4	0.4
'LS03	0.8	1.6	2.4	4.4	0.4
'LS05	1.2	2.4	3.6	6.6	0.4
'LS22	0.4	0.8	1.2	2.2	0.4
'S03	6	13.2	20	36	3.25
'S05	9	19.8	30	54	3.25
'S22	3	6.6	10	18	3.25

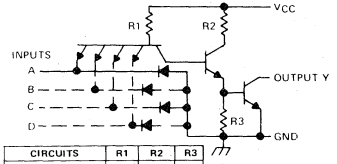
¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'01, '03	C_L = 15 pF, R_L = 4 kΩ for t_{PLH}, 400 Ω for t_{PHL}		35	45		8	15
'05			40	55		8	15
'12, '22			35	45		8	15
'H01, 'H05, 'H22	C_L = 25 pF, R_L = 280 Ω		10	15		7.5	12
'L01, 'L03	C_L = 50 pF, R_L = 4 kΩ		60	90		33	60
'LS01, 'LS03, 'LS05, 'LS22	C_L = 15 pF, R_L = 2 kΩ		17	32		15	28
'S03, 'S05, 'S22	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	2	4.5	7
	C_L = 50 pF, R_L = 280 Ω		7.5			7	

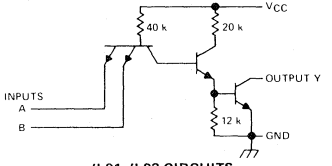
Load circuits and voltage waveforms are shown on pages 148 and 149.

schematics (each gate)

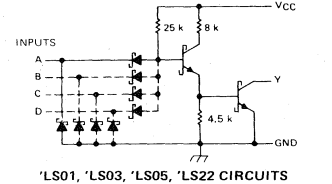


CIRCUITS	R1	R2	R3
'01, '03, '05, '12, '22	4 k	1.6 k	1 k
'H01, 'H05, 'H22	2.8 k	760	470

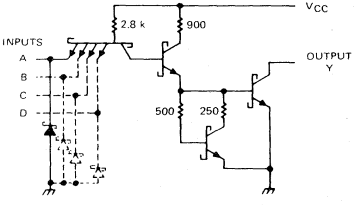
'01, '03, '05, '12, '22, 'H01, 'H05, 'H22 CIRCUITS



'L01, 'L03 CIRCUITS



'LS01, 'LS03, 'LS05, 'LS22 CIRCUITS



'S03, 'S05, 'S22 CIRCUITS

Resistor values shown are nominal and in ohms.

APPLICATION DATA

combined fan-out and wire-AND capabilities

The open-collector TTL gate, when supplied with a proper load resistor (R_L), may be paralleled with other similar TTL gates to perform the wire-AND function, and simultaneously, will drive from one to nine standard loads of its own series. When no other open-collector gates are paralleled, this gate may be used to drive ten loads. For any of these conditions an appropriate load resistor value must be determined for the desired circuit configuration. A maximum resistor value must be determined which will ensure that sufficient load current (to TTL loads) and off current (through paralleled outputs) will be available while the output is high. A minimum resistor value must be determined which will ensure that current through this resistor and sink current from the TTL loads will not cause the output voltage to rise above the low level even if only one of the paralleled outputs is sinking all the currents.

In both conditions (low and high level) the value of R_L is determined by:

$$R_L = \frac{V_{RL}}{I_{RL}}$$

where V_{RL} is the voltage drop in volts, and I_{RL} is the current in amperes.

high-level (off-state) circuit calculations (see figure A)

The allowable voltage drop across the load resistor (V_{RL}) is the difference between V_{CC} applied and the V_{OH} level required at the load:

$$V_{RL} = V_{CC} - V_{OH\ min}$$

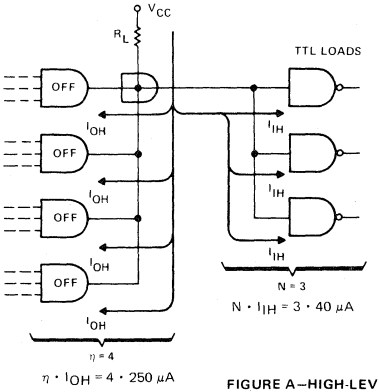
The total current through the load resistor (I_{RL}) is the sum of the load currents (I_{IH}) and off-state reverse currents (I_{OH}) through each of the wire-AND-connected outputs:

$$I_{RL} = \eta \cdot I_{OH} + N \cdot I_{IH} \text{ to TTL loads}$$

Therefore, calculations for the maximum value of R_L would be:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

where η = number of gates wire-AND-connected, and N = number of standard loads.



Calculation:

$$R_{L(max)} = \frac{V_{CC} - V_{OH\ min}}{\eta \cdot I_{OH} + N \cdot I_{IH}}$$

$$R_{L(max)} = \frac{5 - 2.4}{0.001 + 0.00012}\ \Omega = \frac{2.6}{0.00112}\ \Omega = 2321\ \Omega$$

Values shown are for Series 54/74 standard inputs and outputs. For other devices, substitute appropriate values.

FIGURE A—HIGH-LEVEL CIRCUIT CONDITIONS

APPLICATION DATA

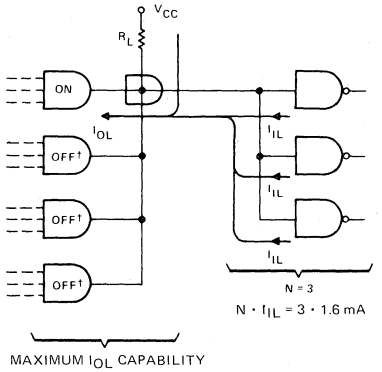
low-level (on-state) circuit calculations (see figure B)

The current through the resistor must be limited to the maximum sink current of one output transistor. Note that if several output transistors are wire-AND connected, the current through R_L may be shared by those paralleled transistors. However, unless it can be absolutely guaranteed that more than one transistor will be on during low-level periods, the current must be limited to the recommended maximum I_{OL}, the maximum current which will ensure that the low-level output voltage, V_{OL}, will be below V_{OL} max.

Also, fan-out must be considered. Part of I_{OL} will be supplied from the inputs which are being driven. This reduces the amount of current which can be allowed through R_L.

Therefore, the equation used to determine the minimum value of R_L would be:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$



Calculation:

$$R_{L(min)} = \frac{V_{CC} - V_{OL\ max}}{I_{OL\ capability} - N \cdot I_{IL}}$$

$$R_{L(min)} = \frac{5 - 0.4}{0.016 - 0.0048}\ \Omega = \frac{4.6}{0.0112}\ \Omega = 410\ \Omega$$

Values shown are for Series 54/74 standard inputs and outputs. For other devices, substitute the appropriate values.

†Current into OFF outputs is negligible at the low logic level.

FIGURE B–LOW-LEVEL CIRCUIT CONDITIONS

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '02			SERIES 54 / SERIES 74 '25, '27			SERIES 54L / SERIES 74L 'L02			SERIES 54LS / SERIES 74LS 'LS02, 'LS27			SERIES 54S / SERIES 74S 'S02, 'S260			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−400			−800			−100			−400			−1000	μA
	74 Family			−400			−800			−200			−400			−1000	
Low-level output current, I_{OL}	54 Family			16			16			2			4			20	mA
	74 Family			16			16			3.6			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '02, '25, '27			SERIES 54L / SERIES 74L 'L02			SERIES 54LS / SERIES 74LS 'LS02, 'LS27			SERIES 54S / SERIES 74S 'S02, 'S260			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		1, 2			2			2			2			2			V
V_{IL}	Low-level input voltage		1, 2		54 Family			0.8			0.7			0.7			0.8	V
					74 Family			0.8			0.7			0.8			0.8	
V_I	Input clamp voltage		3	V_{CC} = MIN, I_I = §				*−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
					74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage		4	V_{CC} = MAX, V_I = 5.5 V				1			0.1			0.1			1	mA
I_{IH}	High-level input current	Data inputs	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			10							μA
		Strobe of '25						160										
		All inputs			V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	All inputs	5	V_{CC} = MAX	V_{IL} = 0.3 V						−0.18							mA
		Data inputs			V_{IL} = 0.4 V			−1.6						−0.36				
		Strobe of '25						−6.4										
		All inputs			V_{IL} = 0.5 V												−2	
I_{OS}	Short-circuit output current♦		6	V_{CC} = MAX	54 Family	−20		−55	−3		−15	−6		−40	−40		−100	mA
					74 Family	−18		−55	−3		−15	−5		−42	−40		−100	
I_{CC}	Supply current		7	V_{CC} = MAX		See table on next page												mA

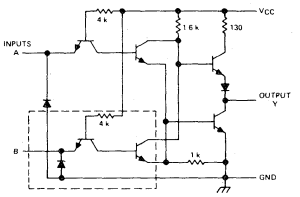
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS', SN54S/SN74S'.
♦Not more than one output should be shorted at a time, and for SN54S'/SN74S', duration of output short-circuit should not exceed one second.
*The input clamp voltage specification is effective for SN5402/SN7402 parts date-coded 7332 or higher.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'02	8	16	14	27	2.75
'25	8	16	10	19	2.25
'27	10	16	16	26	4.34
'L02	0.8	1.6	1.4	2.6	0.275
'LS02	1.6	3.2	2.8	5.4	0.55
'LS27	2.0	4	3.4	6.8	0.9
'S02	17	29	26	45	5.38
'S260	17	29	20	35	9.25

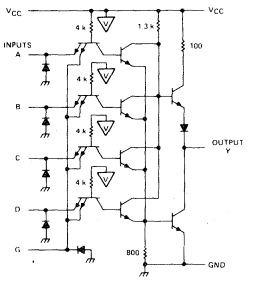
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

schematics (each gate)



The portion of the schematic within the dashed lines is repeated for the C input of the '27.

'02, '27 CIRCUITS



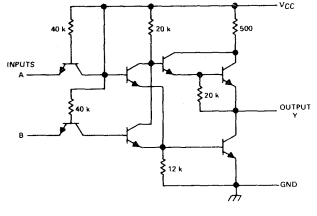
'25 CIRCUITS

switching characteristics at V_{CC} = 5 V, T_A = 25°C

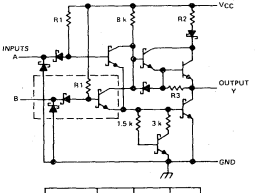
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'02	C_L = 15 pF, R_L = 400 Ω		12	22		8	15
'25			13	22		8	15
'27			7	11		10	15
'L02	C_L = 50 pF, R_L = 4 kΩ		31	60		35	60
'LS02, 'LS27	C_L = 15 pF, R_L = 2 kΩ		10	20		10	20
'S02	C_L = 15 pF, R_L = 280 Ω		3.5	5.5		3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5	
'S260	C_L = 15 pF, R_L = 280 Ω		3.5★			3.5★	

#Load circuit and voltage waveforms are shown on pages 148 and 149.
★Tentative data.

Resistor values are nominal and in ohms.



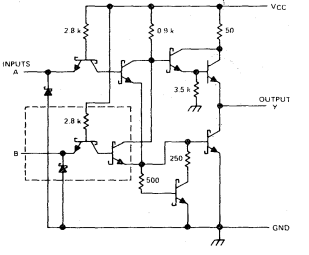
'L02 CIRCUITS



TYPE	R1	R2	R3
'LS02	25 k	200	4 k
'LS27	20 k	100	5 k

The portion of the schematic within the dashed lines is repeated for the C input of the 'LS27.

'LS02, 'LS27 CIRCUITS



The portion of the schematic within the dashed lines is repeated for each additional input of the 'S260, and the 0.9-kΩ resistor is changed to 0.6 kΩ.

'S02, 'S260 CIRCUITS

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 SERIES 74 '08,			SERIES 54H SERIES 74H 'H11, 'H21			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S11			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−500			−400			−1000	μA
Low-level output current, I_{OL}	54 Family			16			20			4			20	mA
	74 Family			16			20			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '08			SERIES 54H SERIES 74H 'H11, 'H21			SERIES 54LS SERIES 74LS 'LS08, 'LS11, 'LS21			SERIES 54S SERIES 74S 'S11			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.8	V
				74 Family			0.8			0.8			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §			*−1.5			*−1.5			−1.5			−1.2		V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.4		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50							μA
				V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6			−2			−0.36				mA
				V_{IL} = 0.5 V												−2	
I_{OS}	Short circuit output current◆	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−6		−40	−40		−100	mA
				74 Family	−18		−55	−40		−100	−5		−42	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
◆Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of output short circuit should not exceed one second.
*The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts shipped after 31 July 1973.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'08	11	21	20	33	3.88
'H11	18	30	30	48	8
'H21	12	20	20	32	8
'LS08	2.4	4.4	6.8	8.8	0.85
'LS11	1.8	3.6	3.3	6.6	0.85
'LS21	1.2	2.4	2.2	4.4	0.85
'S11	13.5	24	24	42	6.25

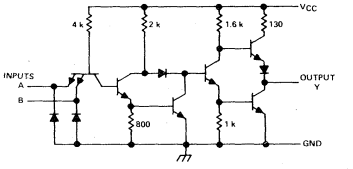
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

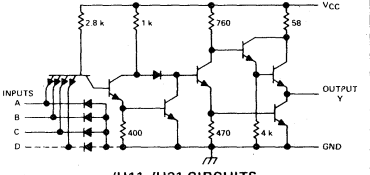
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'08	C_L = 15 pF, R_L = 400 Ω		17.5	27		12	19
'H11, 'H21	C_L = 25 pF, R_L = 280 Ω		7.6	12		8.8	12
'LS08, 'LS11 'LS21	C_L = 15 pF, R_L = 2 kΩ		12	24		12	24
'S11	C_L = 15 pF, R_L = 280 Ω	2.5	4.5	7	2.5	5	7.5
	C_L = 50 pF, R_L = 280 Ω		6			7.5	

#Load circuit and voltage waveforms are shown on pages 148 and 149.

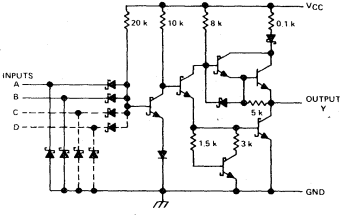
schematics (each gate)



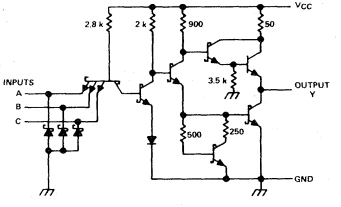
'08 CIRCUITS



'H11, 'H21 CIRCUITS



'LS08, 'LS11, 'LS21 CIRCUITS



'S11 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '09			SERIES 54H SERIES 74H 'H15			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S15			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			16			20			4			20	mA
	74 Family			16			20			8			20	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '09			SERIES 54H SERIES 74H 'H15			SERIES 54LS SERIES 74LS 'LS09, 'LS15			SERIES 54S SERIES 74S 'S15			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.8	V
				74 Family			0.8			0.8			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §				*−1.5			*−1.5			−1.5			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 2 V, V_{OH} = 5.5 V,				250			250			100			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50							μA
				V_{IH} = 2.7 V									20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6			−2			−0.36				mA
				V_{IL} = 0.5 V												−2	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page												mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = − 12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS'.
*The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts shipped after 31 July 1973.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'09	11	21	20	33	3.88
'H15	15	25	30	48	7.5
'LS09	2.4	4.8	4.4	8.8	0.85
'LS15	1.8	3.6	3.3	6.6	0.85
'S15	10.5	19.5	24	42	5.75

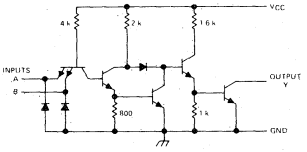
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

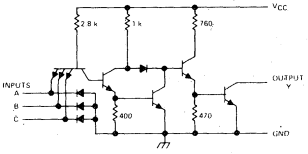
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'09	C_L = 15 pF, R_L = 400 Ω		21	32		16	24
'H15	C_L = 25 pF, R_L = 280 Ω		12	18		9	13
'LS09, 'LS15	C_L = 15 pF, R_L = 2 kΩ		20	35		20	35
'S15	C_L = 15 pF, R_L = 280 Ω	2.5	5.5	8.5	2.5	6	9
	C_L = 50 pF, R_L = 280 Ω		8.5			8	

#Load circuit and voltage waveforms are shown on pages 148 and 149.

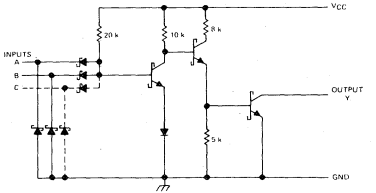
schematics (each gate)



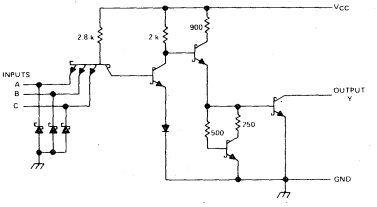
'09 CIRCUITS



'H15 CIRCUITS



'LS09, 'LS15 CIRCUITS



'S15 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '13			SERIES 54 / SERIES 74 '14			SERIES 54 / SERIES 74 '132			SERIES 54S / SERIES 74S 'S132			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−800			−800			−1000	μA
Low-level output current, I_{OL}				16			16			16			20	mA
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

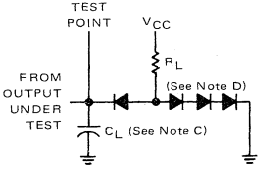
PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '13			SERIES 54 / SERIES 74 '14			SERIES 54 / SERIES 74 '132			SERIES 54S / SERIES 74S 'S132			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage	8	V_{CC} = 5 V		1.5	1.7	2	1.5	1.7	2	1.5	1.7	2	1.6	1.77	1.9	V
V_{T-}	Negative-going threshold voltage	9	V_{CC} = 5 V		0.6	0.9	1.1	0.6	0.9	1.1	0.6	0.9	1.1	1.1	1.22	1.4	V
	Hysteresis ($V_{T+}-V_{T-}$)	8, 9	V_{CC} = 5 V		0.4	0.8		0.4	0.8		0.4	0.8		0.2	0.55		V
V_I	Input clamp voltage	3	V_{CC} = MIN,	I_I = §			−1.5			−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	9	V_{CC} = MIN, V_I = V_{T-}min, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.4		2.4	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.4		2.4	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	8	V_{CC} = MIN, I_{OL} = MAX	V_I = V_{T+}max,		0.2	0.4		0.2	0.4		0.2	0.4			0.5	V
I_{T+}	Input current at positive-going threshold	8	V_{CC} = 5 V,	V_I = V_{T+}		−0.65			−0.43			−0.43			−0.9		mA
I_{T-}	Input current at negative-going threshold	9	V_{CC} = 5 V,	V_I = V_{T-}		−0.85			−0.56			−0.56			−1.1		mA
I_I	Input current at maximum input voltage	4	V_{CC} = MAX,	V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX,	V_I = 2.4 V			40			40			40				μA
				V_I = 2.7 V												50	
I_{IL}	Low-level input current	5	V_{CC} = MAX,	V_{IL} = 0.4 V		−1	−1.6		−0.8	−1.2		−0.8	−1.2				mA
				V_{IL} = 0.5 V												−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−18		−55	−18		−55	−18		−55	−40		−100	mA
I_{CC}	Supply current, Total, output high	7	V_{CC} = MAX			14	23		22	36		15	24		28	44	mA
	Supply current, Total, output low					20	32		39	60		26	40		44	68	
	Supply current, Average per gate		V_{CC} = 5 V,	50% duty cycle		8.5			5.1			5.1			9		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ I_I = −12 mA for SN54'/SN74' and −18 mA for 'S132.
♦Not more than one output should be shorted at a time, and for 'S132, duration of output short-circuit should not exceed one second.

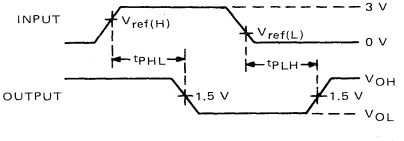
switching characteristics, V_{CC} = 5 V, T_A = 25°C

TYPE	TEST CONDITIONS	t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'13	C_L = 15 pF, R_L = 400 Ω	18	27	15	22
'14, '132		15	22	15	22
'S132	C_L = 15 pF, R_L = 280 Ω	7	10.5	8.5	13

PARAMETER MEASUREMENT INFORMATION



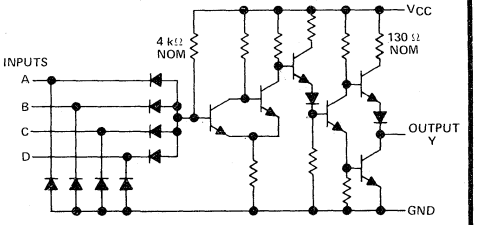
LOAD CIRCUIT



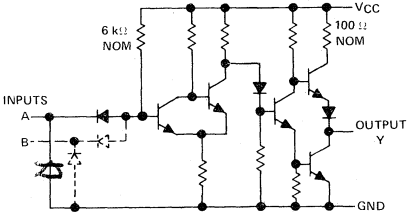
VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator with the following characteristics: Z_{out} = 50 Ω and PRR ≤ 1 MHz. Rise and fall times between 10 and 90 percent points are 10 ns for SN54'/SN74' circuits and 2.5 ns for 'S132.
B. Reference voltages for SN54'/SN74' circuits are: $V_{ref(H)}$ = 1.7 V, $V_{ref(L)}$ = 0.9 V. Reference voltages for 'S132 are: $V_{ref(H)}$ = 1.8 V, $V_{ref(L)}$ = 1.2 V.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

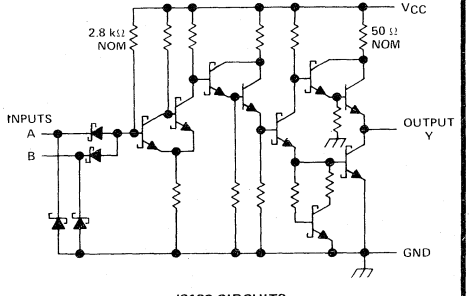
schematics (each gate)



'13 CIRCUITS



'14, '132 CIRCUITS



'S132 CIRCUITS

TYPICAL CHARACTERISTICS†

POSITIVE-GOING THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

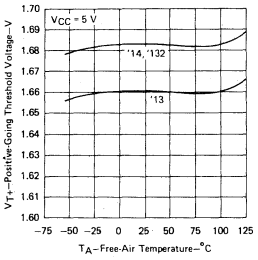


FIGURE 1

NEGATIVE-GOING THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE

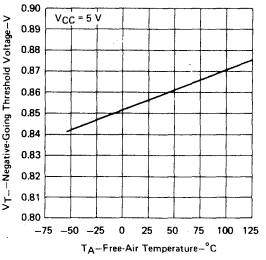


FIGURE 2

HYSTERESIS vs FREE-AIR TEMPERATURE

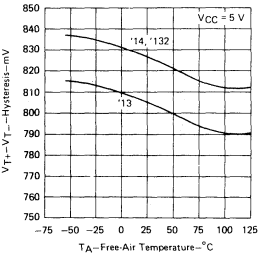


FIGURE 3

2

'13 DISTRIBUTION OF UNITS FOR HYSTERESIS

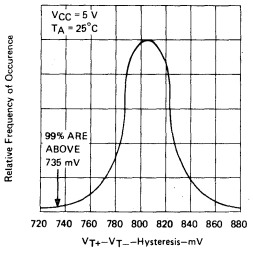


FIGURE 4

'14, '132 DISTRIBUTION OF UNITS FOR HYSTERESIS

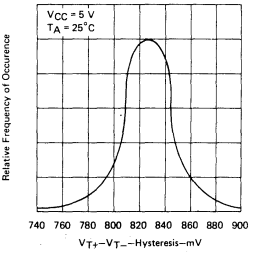


FIGURE 5

THRESHOLD VOLTAGES vs SUPPLY VOLTAGE

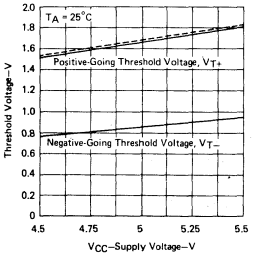


FIGURE 6

HYSTERESIS vs SUPPLY VOLTAGE

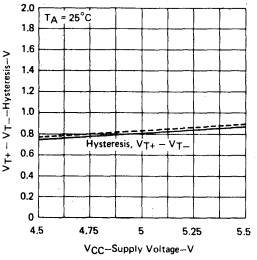


FIGURE 7

OUTPUT VOLTAGE vs INPUT VOLTAGE

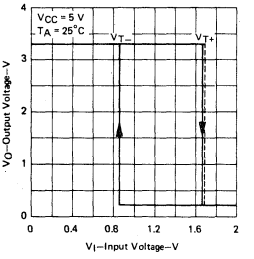
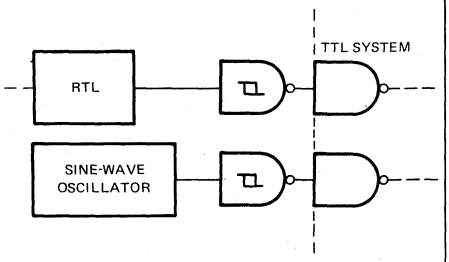


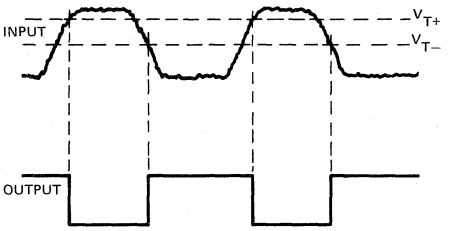
FIGURE 8

†Typical values of '13, '14, and '132 circuit types. Dashed lines in Figures 6, 7, and 8 are applicable for the '14 and '132 circuit types.

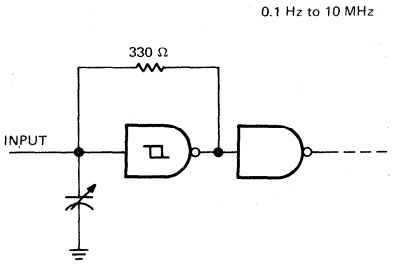
TYPICAL APPLICATION DATA



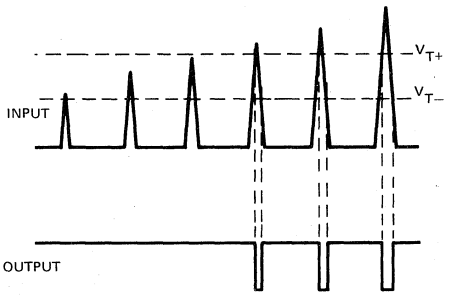
TTL SYSTEM INTERFACE
FOR SLOW INPUT WAVEFORMS



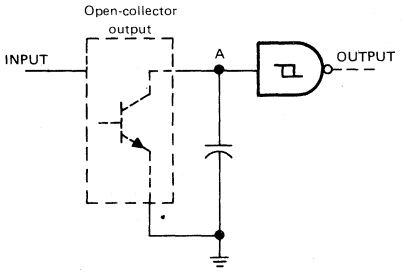
PULSE SHAPER

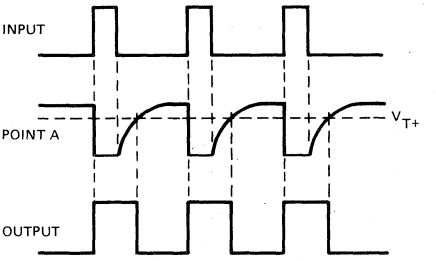


MULTIVIBRATOR



THRESHOLD DETECTOR





PULSE STRETCHER

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			'28			'37, '40			'H40			'LS28, 'LS37 'LS40			'S40			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family		4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−2.4			−1.2			−1.5			−1.2			−3	mA
Low-level output current, I_{OL}	54 Family				48			48			60			12			60	mA
	74 Family				48			48			60			24			60	
Operating free-air temperature, T_A	54 Family		−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family		0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74						SERIES 54H SERIES 74H			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
					'28			'37, '40			'H40			'LS28, 'LS37, 'LS40			'S40			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.8			0.7			0.8	V
				74 Family			0.8			0.8			0.8			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			•−1.5			•−1.5			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.3		2.4	3.4		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.3		2.4	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.26	0.4		0.2	0.4		0.2	0.4		0.25	0.4			0.5	V
				74 Family		0.26	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1			1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			40			100							μA
				V_{IH} = 2.7 V												20			100	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6			−1.6			−4			−0.36				mA
				V_{IL} = 0.5 V															−4	
I_{OS}	Short-circuit output current♦	6		54 Family	−70		−180	−20		−70	−40		−125	−6		−40	−50		−225	mA
				74 Family	−70		−180	−18		−70	−40		−125	−5		−42	−50		−225	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
♦Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second for '28, '37, '40, or 'H40; or 100 milliseconds for 'S40.
•The input clamp voltage specification is effective for '40 and 'H40 parts date-coded 7332 or higher.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'28	12	21	33	57	5.63
'37	9	15.5	34	54	5.38
'40	4	8	17	27	5.25
'H40	10.4	16	25	40	8.85
'LS28	1.8	3.6	6.9	13.8	1.09
'LS37	0.9	2	6	12	0.86
'LS40	0.45	1	3	6	0.86
'S40	5	9	12.5	22	4.38

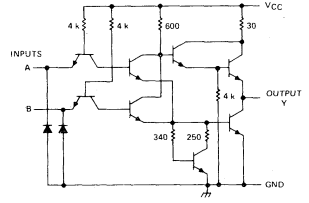
¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

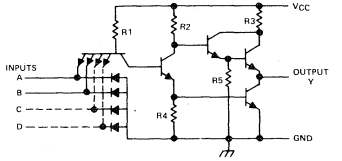
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low output		
		MIN	TYP	MAX	MIN	TYP	MAX
'28	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'37	C_L = 45 pF, R_L = 133 Ω		13	22		8	15
'40	C_L = 15 pF, R_L = 133 Ω		13	22		8	15
'H40	C_L = 25 pF, R_L = 93 Ω		8.5	12		6.5	12
'LS28	C_L = 45 pF, R_L = 667 Ω		12	24		12	24
'LS37			12	24		12	24
'LS40			12	24		12	24
'S40	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	2	4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on pages 148 and 149.

schematics (each gate)

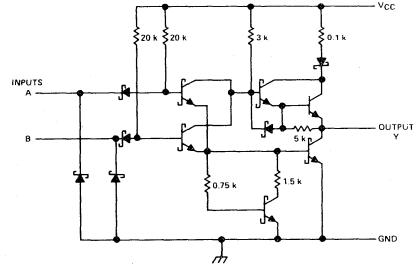


'28 CIRCUITS



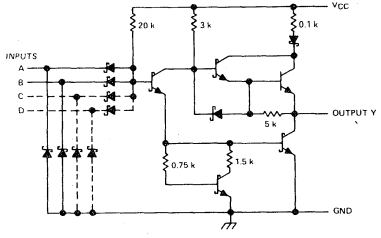
'37, '40, 'H40 CIRCUITS

	'37	'40	'H40
R1	4 k	4 k	1.4 k
R2	600	600	390
R3	100	100	45
R4	400	400	250
R5	4 k	4 k	2 k

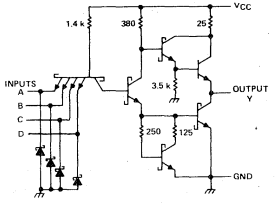


'LS28 CIRCUITS

Resistor values shown are nominal and in ohms.



'LS37, 'LS40 CIRCUITS



'S40 CIRCUITS

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '128			SERIES 54S SERIES 74S 'S140			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−29			−40	mA
	74 Family			−42.4			−40	
Low-level output current, I_{OL}				48			60	mA
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '128			SERIES 54S SERIES 74S 'S140			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = §				−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	54 Family	2.4	3.4					V
				74 Family	2.4	3.4					
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = −13.2 mA		2.4						
			V_{CC} = MIN, V_{IL} = 0.4 V, I_{OH} = MAX		2						
			V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −3 mA	54 Family				2.5	3.4		
				74 Family				2.7	3.4		
			V_{CC} = MIN, V_{IL} = 0.5 V, R_O = 50 Ω to GND					2			
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.26	0.4			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						100	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6				mA
				V_{IL} = 0.5 V						−4	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX		−70		−180	−50		−225	mA
I_{CC}	Supply current, Total, outputs high	7	V_{CC} = MAX			12	21		10	18	mA
	Supply current, Total, outputs low					33	57		25	44	
	Supply current, Average per gate		V_{CC} = 5 V, 50% duty cycle			5.63			8.75		

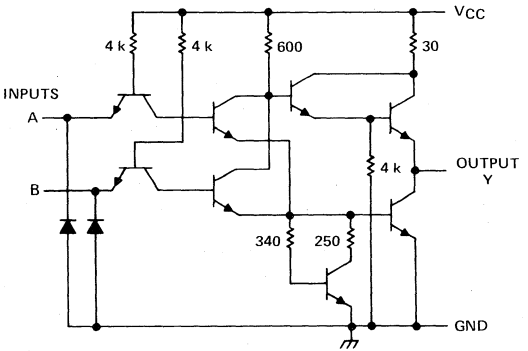
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for '128 and −18 mA for 'S140.
♦Not more than one output should be shorted at a time, and duration of short circuit should not exceed one second for '128 or 100 milliseconds for 'S140.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

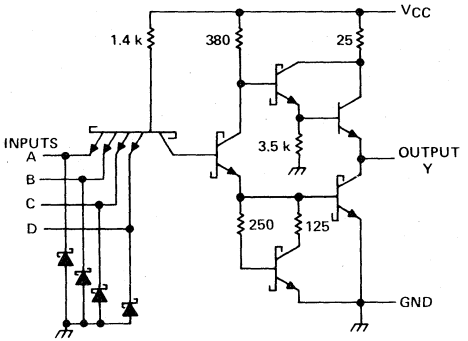
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'128	C_L = 50 pF, R_L = 133 Ω		6	9		8	12
	C_L = 150 pF, R_L = 133 Ω		10	15		12	18
'S140	C_L = 50 pF, R_L = 93 Ω	2	4	6.5	2	4	6.5
	C_L = 150 pF, R_L = 93 Ω		6			6	

#Load circuit and voltage waveforms are shown on page 148.

schematics (each driver)



'128 CIRCUITS



'S140 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74												SERIES 54LS / SERIES 74LS			UNIT
		'06, '07			'16, '17			'26			'33, '38			'LS33, 'LS38			
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				30			15			15			5.5			5.5	V
Low-level output current, I_{OL}	54 Family			30			30			16			48			12	mA
	74 Family			40			40			16			48			24	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74								SERIES 54LS / SERIES 74LS		UNIT
					'06, '07		'16, '17		'26		'33, '38		'LS33, 'LS38		
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1, 2			2		2		2		2		2		V
V_{IL}	Low-level input voltage	1, 2		54 Family		0.8		0.8		0.8		0.8		0.7	V
				74 Family		0.8		0.8		0.8		0.8		0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN,	I_I = §		*−1.5		*−1.5		*−1.5		−1.5		−1.5	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_I = ▲	V_{OH} = 12 V						50					μA
				V_{OH} = MAX		250		250		1000		250		100	
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{OL} = 16 mA	V_I = ▲,		0.4		0.4		0.4					V
			V_{CC} = MIN, V_I = ▲, I_{OL} = MAX	54 Family		0.7		0.7		0.4		0.4		0.4	
				74 Family		0.7		0.7		0.4		0.4		0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX,	V_I = 5.5 V		1		1		1		1		0.1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V		40		40		40		40			μA
				V_{IH} = 2.7 V										20	
I_{IL}	Low-level input current	5	V_{CC} = MAX,	V_{IL} = 0.4 V		−1.6		−1.6		−1.6		−1.6		−0.36	mA
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page										mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS'.
▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.
*The input clamp voltage specification is effective for Series 54/74 parts date-coded 7332 or higher.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'06, '16	30	48	32	51	5.17
'07, '17	29	41	21	30	4.17
'26	4	8	12	22	2.00
'33	12	21	33	57	5.63
'38	5	8.5	34	54	4.88
'LS33	1.8	3.6	6.9	13.8	1.09
'LS38	0.9	2	6	12	0.86

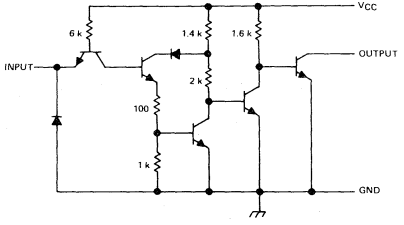
¶Maximum values of I_{CC} shown are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

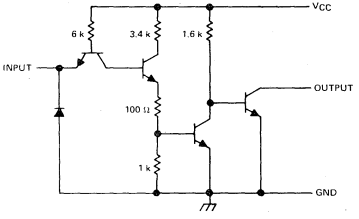
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'06, '16	C_L = 15 pF, R_L = 110 Ω		10	15		15	23
'07, '17			6	10		20	30
'26	C_L = 15 pF, R_L = 1 kΩ		16	24		11	17
'33	C_L = 50 pF, R_L = 133 Ω		10	15		12	18
	C_L = 150 pF, R_L = 133 Ω		15	22		16	24
'38	C_L = 45 pF, R_L = 133 Ω		14	22		11	18
'LS33	C_L = 45 pF, R_L = 667 Ω		20	32		18	28
'LS38			20	32		18	28

#Load circuit and voltage waveforms are shown on pages 148 and 149.

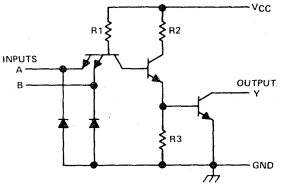
schematics (each gate)



'06, '16 CIRCUITS

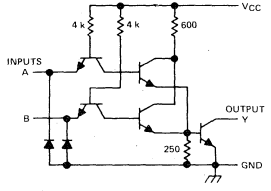


'07, '17 CIRCUITS

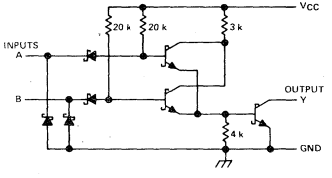


CIRCUITS	R1	R2	R3
'26	4 kΩ	1.6 kΩ	1 kΩ
'38	4 kΩ	600 Ω	400 Ω

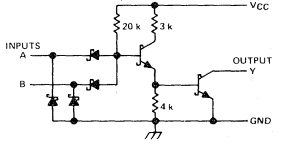
'26, '38 CIRCUITS



'33 CIRCUITS



'LS33 CIRCUITS



'LS38 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

	54 FAMILY 74 FAMILY	SERIES 54 SERIES 74 '32			SERIES 54LS SERIES 74LS 'LS32			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}				−800			−400	μA
Low-level output current, I_{OL}	54 Family			16			4	mA
	74 Family			16			8	
Operating free-air temperature, T_A	54 Family	−55		125	−55		125	°C
	74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '32			SERIES 54LS SERIES 74LS 'LS32			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		1, 2			2			2			V
V_{IL}	Low-level input voltage		1, 2		54 Family			0.8			0.7	V
					74 Family			0.8			0.8	
V_I	Input clamp voltage		3	V_{CC} = MIN, I_I = §				*−1.5			−1.5	V
V_{OH}	High-level output voltage		1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = MAX	54 Family	2.4	3.4		2.5	3.4		V
					74 Family	2.4	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		2	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OL} = MAX	54 Family		0.2	0.4		0.25	0.4	V
					74 Family		0.2	0.4		0.35	0.5	
I_I	Input current at maximum input voltage		4	V_{CC} = MAX, V_I = 5.5 V				1			0.1	mA
I_{IH}	High-level input current		4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
					V_{IH} = 2.7 V						20	
I_{IL}	Low-level input current		5	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−0.36	mA
I_{OS}	Short-circuit output current◆		6	V_{CC} = MAX	54 Family	−20		−55	−6		−40	mA
					74 Family	−18		−55	−5		−42	
I_{CC}	Supply current	Total, outputs high	7	V_{CC} = MAX			15	22		3.1	6.2	mA
		Total, outputs low					23	38		4.9	9.8	
		Average per gate		V_{CC} = 5 V, 50% duty cycle			4.75			1.00		

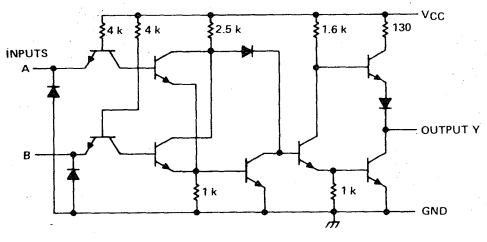
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54LS'/SN74LS'.
◆Not more than one output should be shorted at a time.
*The input clamp voltage specification is effective for Series 54/74 parts date-coded 7332 or higher.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

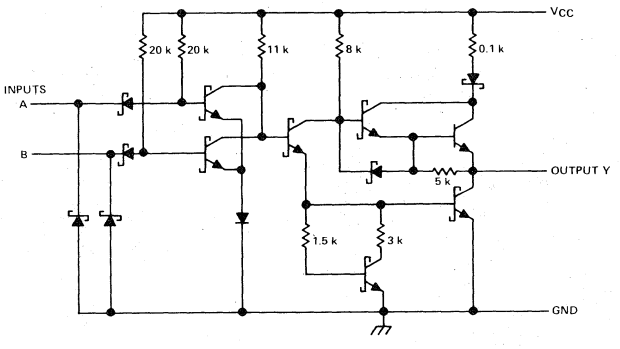
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'32	C_L = 15 pF, R_L = 400 Ω		10	15		14	22
'LS32	C_L = 15 pF, R_L = 2 kΩ		14	22		14	22

#Load circuit and voltage waveforms are shown on pages 148 and 149.

schematics (each gate)



'32 CIRCUITS



'LS32 CIRCUITS

Resistor values shown are nominal and in ohms.

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
			'51, '54			'H51, 'H54			'L51, 'L54, 'L55			'LS51, 'LS54, 'LS55			'S51, 'S64			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		54 Family			−400			−500			−100			−400			−1000	μA
		74 Family			−400			−500			−200			−400			−1000	
Low-level output current, I_{OL}		54 Family			16			20			2			4			20	mA
		74 Family			16			20			3.6			8			20	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74			SERIES 54H SERIES 74H			SERIES 54L SERIES 74L			SERIES 54LS SERIES 74LS			SERIES 54S SERIES 74S			UNIT
					'51, '54			'H51, 'H54			'L51, 'L54, 'L55			'LS51, 'LS54, 'LS55			'S51, 'S64			
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2			2			2			2			2			2			V
V_{IL}	Low-level input voltage	1, 2		54 Family			0.8			0.8			0.7			0.7			0.8	V
				74 Family			0.8			0.8			0.7			0.8			0.8	
V_I	Input clamp voltage	3	V_{CC} = MIN,	I_I = §			•−1.5			•−1.5						−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = V_{IL} max, I_{OH} = MAX	54 Family	2.4	3.4		2.4	3.4		2.4	3.3		2.5	3.4		2.5	3.4		V
				74 Family	2.4	3.4		2.4	3.4		2.4	3.2		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX	54 Family		0.2	0.4		0.2	0.4		0.15	0.3		0.25	0.4			0.5	V
				74 Family		0.2	0.4		0.2	0.4		0.2	0.4		0.35	0.5			0.5	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX,	V_I = 5.5 V			1			1			0.1			0.1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40			50			10							μA
				V_{IH} = 2.7 V												20			50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.3 V									−0.18							mA
				V_{IL} = 0.4 V			−1.6			−2						−0.36				
				V_{IL} = 0.5 V															−2	
I_{OS}	Short-circuit output current◆	6	V_{CC} = MAX	54 Family	−20		−55	−40		−100	−3		−15	−6		−40	−40		−100	mA
				74 Family	−18		−55	−40		−100	−3		−15	−5		−42	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table on next page															mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74', −8 mA for SN54H'/SN74H', and −18 mA for SN54LS'/SN74LS' and SN54S'/SN74S'.
◆Not more than one output should be shorted at a time, and for SN54H'/SN74H' and SN54S'/SN74S', duration of the short-circuit should not exceed one second.
•The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts date-coded 7332 or higher.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per AOI gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'51	4	8	7.4	14	2.85
'54	4	8	5.1	9.5	4.55
'H51	8.2	12.8	15.2	24	5.85
'H54	7.1	11	9.4	14	8.25
'L51	0.44	0.8	0.76	1.3	0.30
'L54	0.39	0.8	0.60	0.99	0.50
'L55	0.22	0.4	0.38	0.65	0.30
'LS51	0.8	1.6	1.4	2.8	0.55
'LS54	0.8	1.6	1.0	2	0.9
'LS55	0.4	0.8	0.7	1.3	0.55
'S51	8.2	17.8	13.6	22	5.45
'S64	7	12.5	8.5	16	7.75

¶ Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics at V_{CC} = 5 V, T_A = 25°C

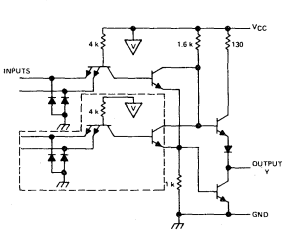
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output			t_{PHL} (ns) Propagation delay time, high-to-low-level output		
		MIN	TYP	MAX	MIN	TYP	MAX
'51, '54	C_L = 15 pF, R_L = 400 Ω		13	22		8	15
'H51	C_L = 25 pF, R_L = 280 Ω		6.8	11		6.2	11
'H54	C_L = 25 pF, R_L = 280 Ω		7	11		6.2	11
'L51, 'L54, 'L55	C_L = 50 pF, R_L = 4 kΩ		50	90		35	60
'LS51, 'LS55	C_L = 15 pF, R_L = 2 kΩ		12	20		12.5	20
'LS54	C_L = 15 pF, R_L = 2 kΩ		16	25		12.5	20
'S51, 'S64	C_L = 15 pF, R_L = 280 Ω	2	3.5	5.5	2	3.5	5.5
	C_L = 50 pF, R_L = 280 Ω		5			5.5	

#Load circuit and voltage waveforms are shown on pages 148 and 149.

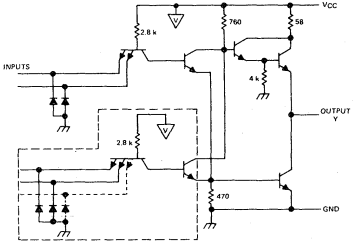
schematics (each gate)

The portion of the circuits within the dashed lines is repeated (with as many emitters or input diodes as applicable) for each additional AND section.

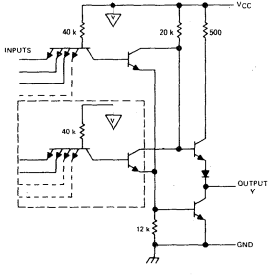
Resistor values shown are nominal and in ohms.



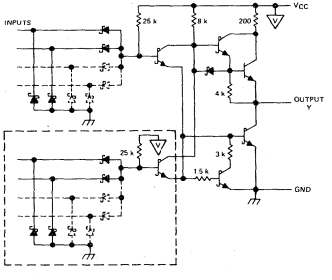
'51, '54 CIRCUITS



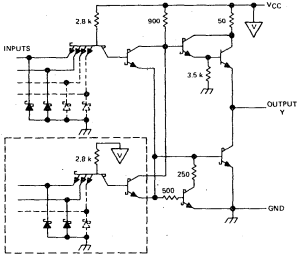
'H51, 'H54 CIRCUITS



'L51, 'L54, 'L55 CIRCUITS



'LS51, 'LS54, 'LS55 CIRCUITS



'S51, 'S64 CIRCUITS

recommended operating conditions

	SN54S65			SN74S65			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	'S65			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1, 2		2			V
V_{IL}	Low-level input voltage	1, 2				0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN, I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	1	V_{CC} = MIN, V_{IH} = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 2 V, I_{OL} = 20 mA			0.5	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.7 V			50	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.5 V			−2	mA
I_{CCH}	Supply current, output high	7	V_{CC} = MAX		6	11	mA
I_{CCL}	Supply current, output low	7	V_{CC} = MAX		8.5	16	mA

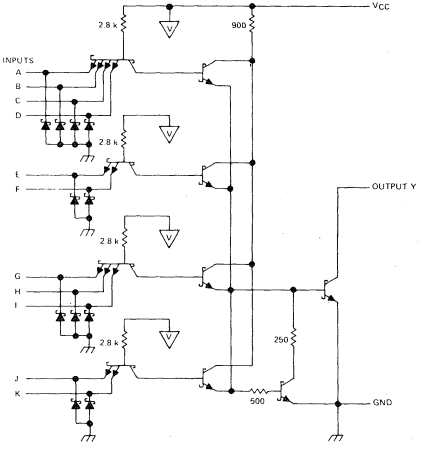
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS#	'S65			UNIT
			MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	ns
		C_L = 50 pF, R_L = 280 Ω		8		ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 280 Ω	2	5.5	8.5	ns
		C_L = 50 pF, R_L = 280 Ω		6.5		ns

#Load circuit and voltage waveforms are shown on page 148.

schematic



Resistor values shown are nominal and in ohms.

recommended operating conditions

		54 FAMILY 74 FAMILY	SERIES 54 SERIES 74						SERIES 54H SERIES 74H			UNIT
			'23			'50, '53			'H50, 'H52, 'H53, 'H55			
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400			−500	μA
Low-level output current, I_{OL}		54 Family			16			16			20	mA
		74 Family			16			16			20	
Operating free-air temperature range, T_A		54 Family	−55		125	−55		125	−55		125	°C
		74 Family	0		70	0		70	0		70	

The '23, '50, and '53 are designed for use with up to four '60 expanders.
The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.
The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 SERIES 74 '23 MIN	'23 TYP‡	'23 MAX	'50, '53 MIN	'50, '53 TYP‡	'50, '53 MAX	SERIES 54H SERIES 74H 'H50, 'H52 'H53, 'H55 MIN	'H50, 'H52 'H53, 'H55 TYP‡	'H50, 'H52 'H53, 'H55 MAX	UNIT
V_{IH} High-level input voltage		1, 2			2			2			2			V
V_{IL} Low-level input voltage		1, 2					0.8			0.8			0.8	V
V_I Input clamp voltage		3	V_{CC} = MIN, I_I = §				−1.5			*−1.5			*−1.5	V
V_{OH} High-level output voltage		1	V_{CC} = MIN, V_I = ▲,	I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		2	V_{CC} = MIN, V_I = ▲,	I_{OL} = MAX		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		4	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH} High-level input current	Data input	4	V_{CC} = MAX, V_{IH} = 2.4 V				40			40			50	μA
	Strobe of '23						160							
I_{IL} Low-level input current	Data inputs	5	V_{CC} = MAX, V_{IL} = 0.4 V				−1.6			−1.6			−2	mA
	Strobe of '23						−6.4							
I_{OS} Short-circuit output current◆		6	V_{CC} = MAX	54 Family	−20		−55	−20		−55	−40		−100	mA
				74 Family	−18		−55	−18		−55	−40		−100	
I_{CC} Supply current		7	V_{CC} = MAX		See table on next page									mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
▲The input voltage is V_{IH} = 2 V or V_{IL} = V_{IL} max, as appropriate. See tables with test figures 1 and 2.
◆Not more than one output should be shorted at a time, and for the SN54H'/SN74H', duration of short-circuit should not exceed one second.
*The input clamp voltage specification is effective for Series 54/74 and 54H/74H parts date-coded 7332 or higher.

electrical characteristics using expander inputs, V_{CC} = MIN, T_A = MIN (unless otherwise noted)

TYPE	$I_{\overline{X}}$ (mA) (I_X for 'H52) Expander current			$V_{BE(Q)}$ (V) Base-emitter voltage of output transistor Q			V_{OH} (V) High-level output voltage			V_{OL} (V) Low-level output voltage		
	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX	TEST CONDITIONS	MIN	TYP‡ MAX
SN5423, SN5450, SN5453	$V_{\overline{X}X}$ = 0.4 V, I_{OL} = 16 mA, See Figure 10		−2.9	$I_X + I_{\overline{X}}$ = 410 μA, $R_{\overline{X}X}$ = 0, I_{OL} = 16 mA, See Figure 11		1	I_X = 150 μA, $I_{\overline{X}}$ = −150 μA, I_{OH} = −400 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 300 μA, $R_{\overline{X}X}$ = 138 Ω, I_{OL} = 16 mA, See Figure 11		0.2 0.4
SN7423, SN5450, SN5453	$V_{\overline{X}X}$ = 0.4 V, I_{OL} = 16 mA, See Figure 10		−3.1	$I_X + I_{\overline{X}}$ = 620 μA, $R_{\overline{X}X}$ = 0, I_{OL} = 16 mA, See Figure 11		1	I_X = 270 μA, $I_{\overline{X}}$ = −270 μA, I_{OH} = −400 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 430 μA, $R_{\overline{X}X}$ = 130 Ω, I_{OL} = 16 mA, See Figure 11		0.2 0.4
SN54H50, SN54H53, SN54H55	$V_{\overline{X}}$ = 1.4 V, I_X = 0, I_{OL} = 0, See Figure 10		−5.85	$I_X + I_{\overline{X}}$ = 700 μA, $R_{\overline{X}X}$ = 0, I_{OL} = 20 mA, See Figure 11		1	I_X = 320 μA, $I_{\overline{X}}$ = −320 μA, I_{OH} = −500 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 470 μA, $R_{\overline{X}X}$ = 68 Ω, I_{OL} = 20 mA, See Figure 11		0.2 0.4
SN74H50, SN74H53, SN74H55	$V_{\overline{X}}$ = 1.4 V, I_X = 0, I_{OL} = 0, See Figure 10		−6.3	$I_X + I_{\overline{X}}$ = 1.1 mA, $R_{\overline{X}X}$ = 0, I_{OL} = 20 mA, See Figure 11		1	I_X = 570 μA, I_X = −570 μA, I_{OH} = −500 μA, See Figure 12	2.4	3.4	$I_X + I_{\overline{X}}$ = 600 μA, $R_{\overline{X}X}$ = 63 Ω, I_{OL} = 20 mA, See Figure 11		0.2 0.4
SN54H52, SN74H52	V_X = 1 V, I_{OH} = −500 μA, See Figure 13	−2.7	−4.5				V_X = 1 V, I_{OH} = −500 μA, See Figure 13	2.4	3.4	I_X = −300 μA, I_{OL} = 20 mA, T_A = MAX, See Figure 14		0.2 0.4

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

supply current¶

TYPE	I_{CCH} (mA) Total with outputs high		I_{CCL} (mA) Total with outputs low		I_{CC} (mA) Average per gate (50% duty cycle)
	TYP	MAX	TYP	MAX	TYP
'23	8	16	10	19	4.5
'50	4	8	7.4	14	2.85
'53	4	8	5.1	9.5	4.55
'H50	8.2	12.8	15.2	24	5.85
'H52	20	31	15.2	24	17.6
'H53	7.1	11	9.4	14	8.25
'H55	4.5	6.4	7.5	12	6.00

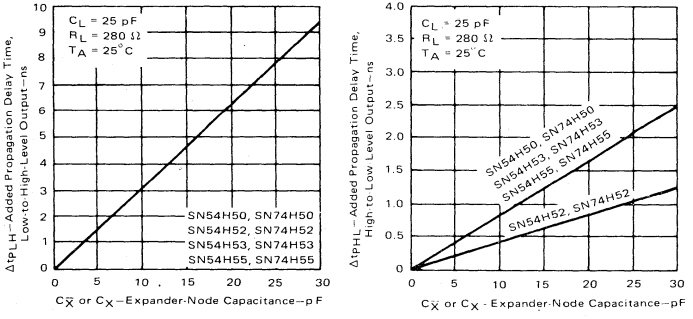
¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

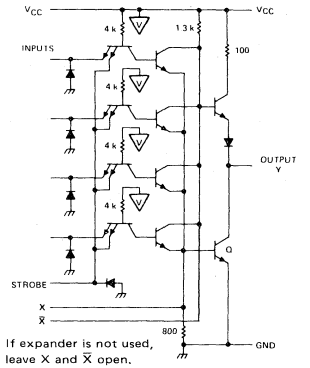
TYPE	TEST CONDITIONS#	t_{PLH} (ns) Propagation delay time, low-to-high-level output		t_{PHL} (ns) Propagation delay time, high-to-low-level output	
		TYP	MAX	TYP	MAX
'23, '50, '53	C_L = 15 pF, R_L = 400 Ω, Expander pins open	13	22	8	15
'50	C_L = 15 pF, R_L = 400 Ω, From input of '60 expander	15	30	10	20
'H50	C_L = 25 pF, R_L = 280 Ω, Expander pins open	6.8	11	6.2	11
'H52		10.6	15	9.2	15
'H53		7	11	6.2	11
'H55		7	11	6.5	11
'H50	C_L = 25 pF, R_L = 280 Ω, C = 15 pF (GND to $\overline{X}$ of 'H50, 'H53, or 'H55; or to X of 'H52)	11		7.4	
'H52		14.8		9.8	
'H53		11.4		7.4	
'H55		11.4		7.7	

#Load circuit and voltage waveforms are shown on page 148.

TYPICAL ADDED PROPAGATION DELAY TIME vs EXPANDER-NODE CAPACITANCE

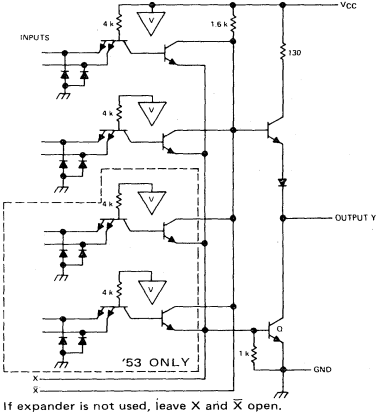


schematics (each gate)



If expander is not used, leave X and $\overline{X}$ open.

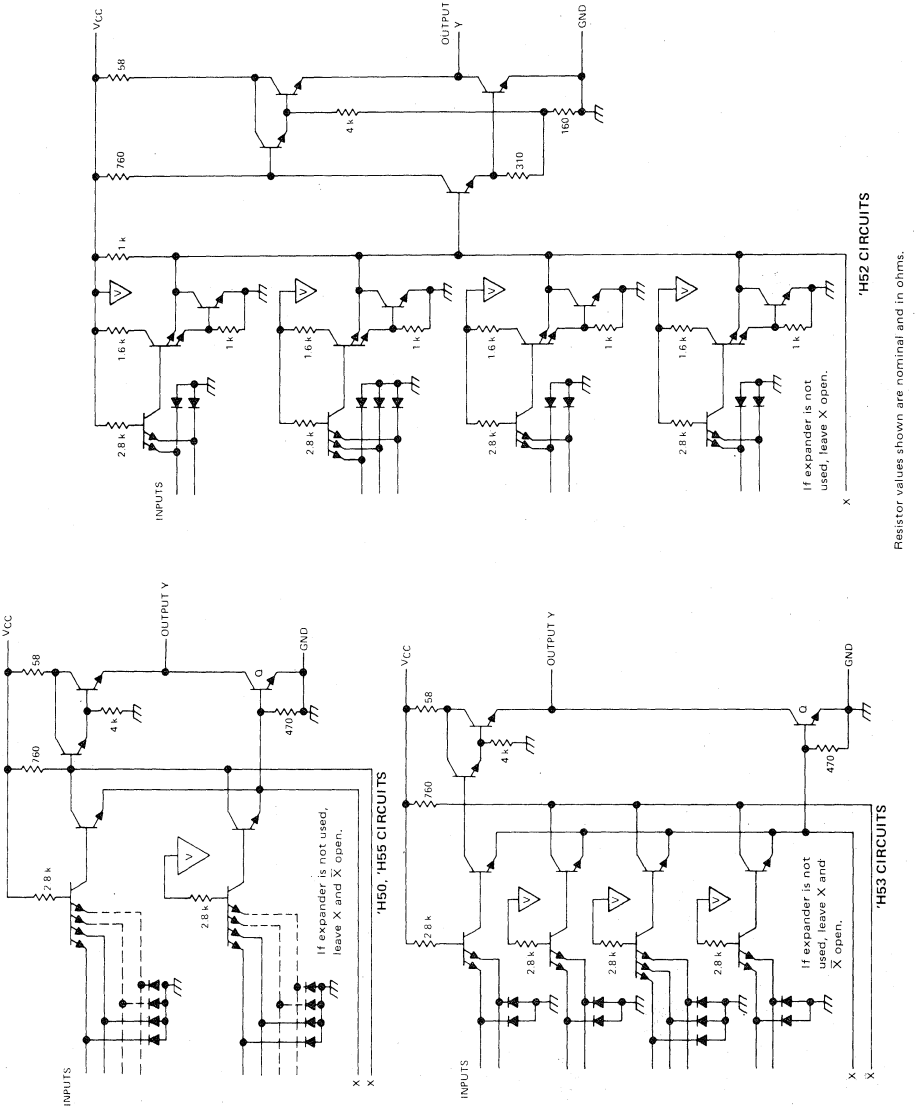
'23 CIRCUITS



If expander is not used, leave X and $\overline{X}$ open.

'50, '53 CIRCUITS

Resistor values shown are nominal and in ohms.

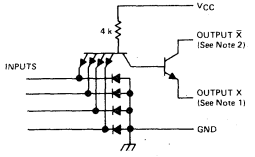

'H52 CIRCUITS
'H50, 'H55 CIRCUITS
'H53 CIRCUITS
VCC
OUTPUT Y
GND
INPUTS
If expander is not used, leave X open.
If expander is not used, leave X and X̄ open.
If expander is not used, leave X and X̄ open.
Resistor values shown are nominal and in ohms.

recommended operating conditions

	SN5460			SN7460			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

The '23, '50, and '53 are designed for use with up to four '60 expanders.

schematic (each gate)



'60 CIRCUITS

NOTES: 1. Connect to X input of '23, '50, or '53 circuit.
2. Connect to $\overline{X}$ input of '23, '50, or '53 circuit.

Resistor value shown is nominal and in ohms.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	SN5460 TEST CONDITIONS	SN5460 MIN	SN5460 TYP‡	SN5460 MAX	SN7460 TEST CONDITIONS	SN7460 MIN	SN7460 TYP‡	SN7460 MAX	UNIT
V_{IH}	High-level input voltage	15		2				2			V
V_{IL}	Low-level input voltage	16				0.8				0.8	V
$V_{\overline{X}X(on)}$	On-state voltage between expander outputs	15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 2.85 mA, T_A = −55°C			0.4	V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 3.05 mA, T_A = 0°C			0.4	V
$I_{X(on)}$	On-state expander current	15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = −55°C	−0.3			V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = 0°C	−0.43			mA
$I_{\overline{X}(off)}$	Off-state expander current	16	V_{CC} = 4.5 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 1.2 kΩ, T_A = −55°C			150	V_{CC} = 4.75 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 1.2 kΩ, T_A = 0°C			270	μA
I_I	Input current at maximum input voltage	4	V_{CC} = 5.5 V, V_I = 5.5 V			1	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = 5.5 V, V_I = 2.4 V			40	V_{CC} = 5.25 V, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	5	V_{CC} = 5.5 V, V_I = 0.4 V			−1.6	V_{CC} = 5.25 V, V_I = 0.4 V			−1.6	mA
$I_{CC(on)}$	Supply current, expander on	7	V_{CC} = 5.5 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.2	2.5	V_{CC} = 5.25 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.2	2.5	mA
$I_{CC(off)}$	Supply current, expander off	7	V_{CC} = 5.5 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		2	4	V_{CC} = 5.25 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		2	4	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

recommended operating conditions

	SN54H60 SN54H62			SN74H60 SN74H62			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

See schematics next page

The 'H50, 'H53, and 'H55 are designed for use with up to four 'H60 expanders or one 'H62 expander.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	SN54H60, SN54H62 TEST CONDITIONS	MIN	TYP‡	MAX	SN74H60, SN74H62 TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		15		2				2			V
V_{IL}	Low-level input voltage		16				0.8				0.8	V
$V_{\overline{X}X(on)}$	On-state voltage between expander outputs		15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 5.85 mA, T_A = −55°C			0.4	V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 6.3 mA, T_A = 0°C			0.4	V
				V_{CC} = 5.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 7.85 mA, T_A = 125°C			0.4	V_{CC} = 5.25 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 7.4 mA, T_A = 70°C			0.4	
$I_{X(on)}$	On-state expander current		15	V_{CC} = 4.5 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = −55°C	−470			V_{CC} = 4.75 V, V_{IH} = 2 V, V_X = 1 V, $I_{\overline{X}}$ = 0, T_A = 0°C	−600			mA
$I_{\overline{X}(off)}$	Off-state expander current		16	V_{CC} = 4.5 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 575 Ω, T_A = −55°C			320	V_{CC} = 4.75 V, V_{IL} = 0.8 V, $V_{\overline{X}}$ = 4.5 V, R_X = 575 Ω, T_A = 0°C			570	μA
I_I	Input current at maximum input voltage		4	V_{CC} = 5.5 V, V_I = 5.5 V			1	V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		4	V_{CC} = 5.5 V, V_I = 2.4 V			50	V_{CC} = 5.25 V, V_I = 2.4 V			50	μA
I_{IL}	Low-level input current		5	V_{CC} = 5.5 V, V_I = 0.4 V			−2	V_{CC} = 5.25 V, V_I = 0.4 V			−2	mA
$I_{CC(on)}$	Supply current, expander on	'H60	7	V_{CC} = 5.5 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0,		1.9	3.5	V_{CC} = 5.25 V, V_I = 4.5 V, V_X = 0.85 V, $I_{\overline{X}}$ = 0		1.9	3.5	mA
		'H62				3.8	7			3.8	7	
$I_{CC(off)}$	Supply current, expander off	'H60	7	V_{CC} = 5.5 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		3	4.5	V_{CC} = 5.25 V, V_I = 0, V_X = 0.85 V, $I_{\overline{X}}$ = 0		3	4.5	mA
		'H62				6	9			6	9	
$C_{\overline{X}}$	Expander output capacitance	'H60		V_{CC}, inputs, and X open; f = 1 MHz		5.4		V_{CC}, inputs, and X open; f = 1 MHz		5.4		pF
		'H62				6.0				6.0		

‡All typical values are at V_{CC} = 5 V (except $C_{\overline{X}}$), T_A = 25°C.

recommended operating conditions

	SN54H61			SN74H61			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Operating free-air temperature, T_A	−55		125	0		70	°C

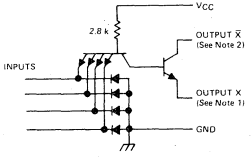
The 'H52 is designed for use with up to six 'H61 expanders.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

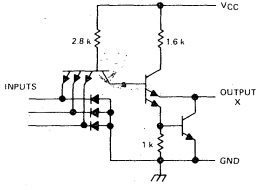
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	17		2			V
V_{IL}	Low-level input voltage	18				0.8	V
$V_{X(on)}$	On-state expander-output voltage	17	V_{CC} = MIN, V_{IH} = 2 V, I_X = 4.5 mA for SN54H61, 5.35 mA for SN74H61, T_A = MIN			1	V
$I_{X(off)}$	Off-state expander current	18	V_{CC} = MIN, V_{IL} = 0.8 V, V_X = 2.2 V, T_A = MAX			50	μA
I_I	Input current at maximum input voltage	4	V_{CC} = 5.5 V, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	4	V_{CC} = 5.5 V, V_I = 2.4 V			50	μA
I_{IL}	Low-level input current	5	V_{CC} = 5.5 V, V_I = 0.4 V			−2	mA
$I_{CC(on)}$	Supply current, expander on	7	V_{CC} = 5.5 V, V_I = 4.5 V		11	16	mA
$I_{CC(off)}$	Supply current, expander off	7	V_{CC} = 5.5 V, V_I = 0		5	7	mA
C_X	Expander output capacitance		V_{CC} and inputs open, f = 1 MHz		5.4		pF

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V (except C_X), T_A = 25°C.

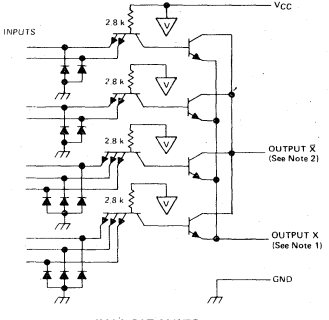
schematics (each gate)



'H60 CIRCUITS



'H61 CIRCUITS



'H62 CIRCUITS

NOTES: 1. Connect to X input of 'H50, 'H53, or 'H55 circuit.
2. Connect to $\overline{X}$ input of 'H50, 'H53, or 'H55 circuit.

Resistor values shown are nominal and in ohms.

recommended operating conditions

		SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−800			−800			−800	μA
Low-level output current, I_{OL}					16			16			16			16			16			16	mA
Pulse width, t_w	Clock high		20			20			30			20			25			25			ns
	Clock low		30			47			37			20			25			25			
	Preset or clear low		25			25			30			20			25			25			
Input setup time, t_{setup}			20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_{hold}			5↑			0↓			5↓			6↑			5↑			30↑			ns
Operating free-air temperature, T_A		Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74	0		70	0		70	0		70	0		70	0		70	0		70	

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			•−1.5			•−1.5			•−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4		•0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1			1			1	mA
I_{IH}	High-level input current	D, J, K, or $\overline{K}$	V_{CC} = MAX, V_I = 2.4 V			40			40			40			40			40			40	μA
		Clear				80			80			120			160			160			80	
		Preset				80			80			80			80			160			80	
		Clock				40			80			80			80			40			120	
I_{IL}	Low-level input current	D, J, K, or $\overline{K}$	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6			−1.6			−1.6			−1.6	mA
		Clear				−3.2			−3.2			−3.2			−4.8			−3.2			−3.2	
		Preset				−3.2			−3.2			−1.6			−3.2			−3.2			−3.2	
		Clock				−1.6			−3.2			−3.2			−3.2			−1.6			−4.8	
I_{OS}	Short-circuit output current◆	Series 54	V_{CC} = MAX	−20		−57	−20		−57	−20		−57	−30		−85	−20		−57	−20		−57	mA
		Series 74		−18		−57	−18		−57	−18		−57	−30		−85	−18		−57	−18		−57	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		13	26		10	20		8.5	15		9	15		20	34		14	20.5	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆ Not more than one output should be shorted at a time.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is at 4.5 V for the '70, '110, and '111, and is grounded for all the others.

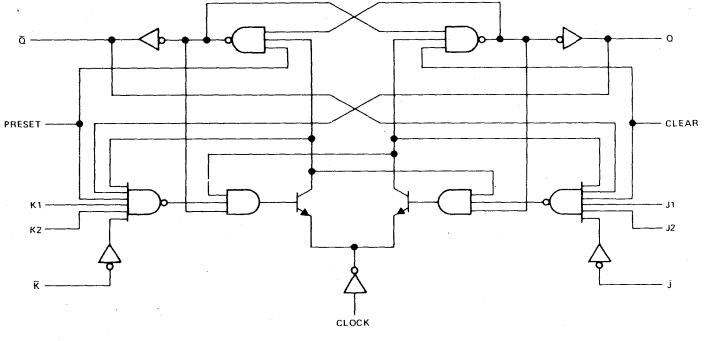
• The input clamp voltage specification is effective for Series 54/74 parts date-coded 7332 or higher.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

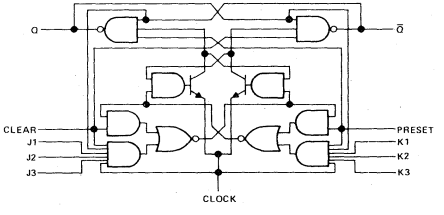
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73 '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}				20	35		15	20		15	25		25	33		20	25		20	25		MHz
t_{PLH}	Preset (as applicable)	Q	C_L = 15 pF, R_L = 400 Ω, See Note 2			50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		$\overline{Q}$				50		25	40			40		23	35		18	25		21	30	
t_{PLH}	Clear (as applicable)	$\overline{Q}$				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		Q				50		25	40			40		17	25		18	25		21	30	
t_{PLH}	Clock	Q or $\overline{Q}$		10	27	50	10	16	25	10	14	25	4	10	16	10	20	30	6	12	17	ns
t_{PHL}				10	18	50	10	25	40	10	20	40	9	18	28	6	13	20	10	20	30	

¶ f_{max} = maximum clock frequency; t_{PLH} = propagation delay time, low-to-high level output; t_{PHL} = propagation delay time, high-to-low-level output.
NOTE 2: Load circuit and voltage waveforms are shown on page 148.

functional block diagrams



'70—GATED J-K WITH CLEAR AND PRESET

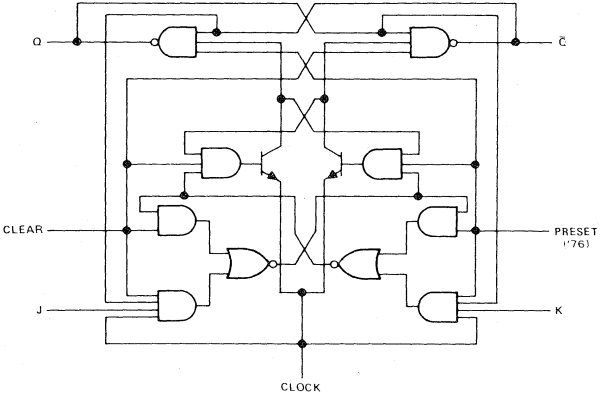


'72—GATED J-K WITH CLEAR AND PRESET

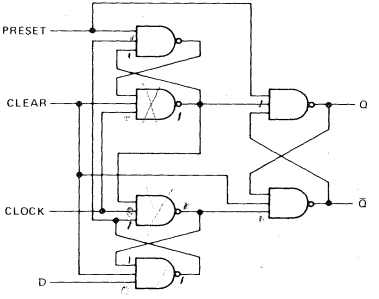
See following pages for:
'73—DUAL J-K WITH CLEAR
'74—DUAL D WITH CLEAR AND PRESET
'76—DUAL J-K WITH CLEAR AND PRESET
'107—DUAL J-K WITH CLEAR

'109—DUAL J-K̄ WITH CLEAR AND PRESET
'110—GATED J-K WITH CLEAR AND PRESET
'111—DUAL J-K WITH CLEAR AND PRESET

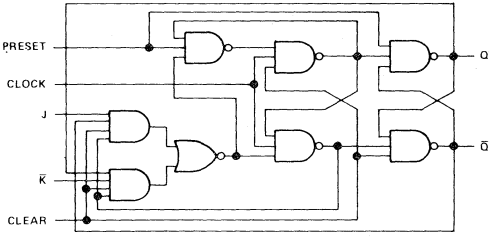
functional block diagrams (continued)



'73–DUAL J-K WITH CLEAR
'76–DUAL J-K WITH CLEAR AND PRESET
'107–DUAL J-K WITH CLEAR

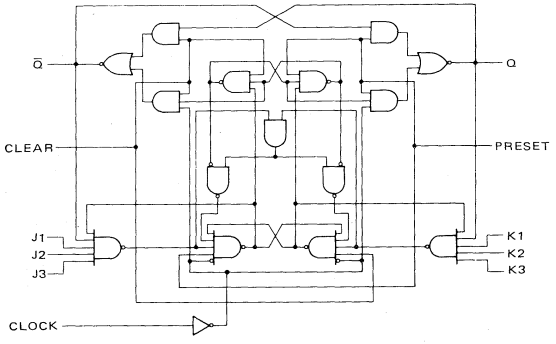


'74–DUAL D WITH CLEAR AND PRESET

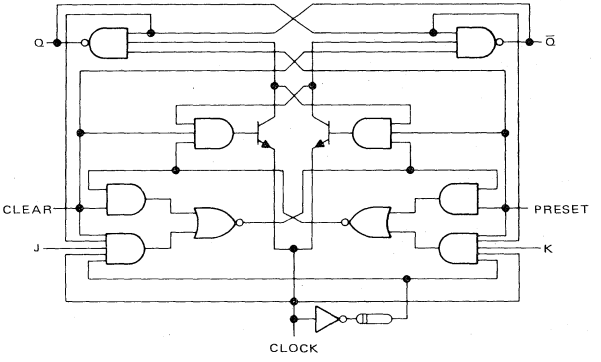


'109–DUAL J-$\overline{K}$ WITH CLEAR AND PRESET

functional block diagrams (continued)

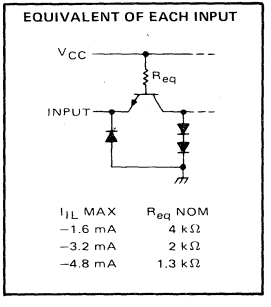


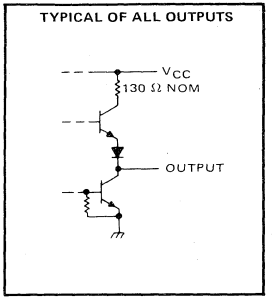
'110—GATED J-K WITH CLEAR AND PRESET



'111—DUAL J-K WITH CLEAR AND PRESET

schematics of inputs and outputs





recommended operating conditions

		SERIES 54H/74H	'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−1000			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		12			12			15			12			ns
	Clock low		28			28			13.5			28			
	Clear or preset low		16			16			25			16			
Setup time, t_{setup}	High-level data		0↑			0↑			10↑			0↑			ns
	Low-level data		0↑			0↑			15↑			0↑			
Hold time, t_{hold}			0↓			0↓			5↑			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓↑ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'H71			'H72, 'H73, 'H76			'H74			'H78			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			V
V_{IL}	Low-level input voltage						0.8			0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA				*−1.5			*−1.5			*−1.5			*−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1			1			1	mA
I_{IH}	High-level input current	D, J, or K	V_{CC} = MAX, V_I = 2.4 V				50			50			50			50	μA
		Clear								100			150			200	
		Preset					150			100			100			100	
		Clock					100			50			100			100	
I_{IL}	Low-level input current	D, J, or K	V_{CC} = MAX, V_I = 0.4 V				−2			−2			−2			−2	mA
		Clear								−4			−4			−8	
		Preset					−6			−4			−2			−4	
		Clock					−4			−2			−4			−4	
I_{OS}	Short-circuit output current◆		V_{CC} = MAX		−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1	Series 54H		19	30		16	25		15	21		16	25	mA
				Series 74H		19	30		16	25		15	25		16	25	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\bar{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

*The input clamp voltage specification is effective for Series 54H/74H parts date-coded [illegible]

switching characteristics, V_{CC} = 5 V, T_A = 25°C

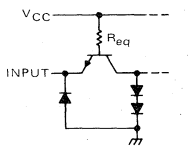
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'H71, 'H72, 'H73, 'H76, 'H78			'H74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}				25	30		35	43		MHz
t_{PLH}	Preset (as applicable)	Q	C_L = 25 pF, R_L = 280 Ω, See Note 2		6	13			20	ns
t_{PHL}		$\overline{Q}$			12	24			30	
t_{PLH}	Clear (as applicable)	$\overline{Q}$			6	13			20	ns
t_{PHL}		Q			12	24			30	
t_{PLH}	Clock	Q or $\overline{Q}$		6	14	21	4	8.5	15	ns
t_{PHL}				10	22	27	7	13	20	

¶ f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 148.

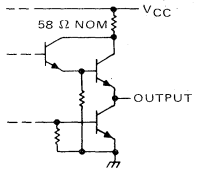
schematics of input and outputs

EQUIVALENT OF EACH INPUT

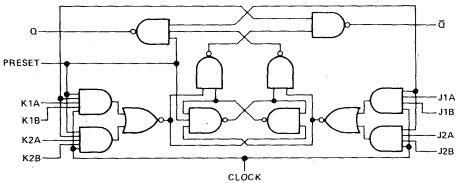


I_{IL} MAX	R_{eq} NOM
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	933 Ω
−8 mA	700 Ω

TYPICAL OF ALL OUTPUTS



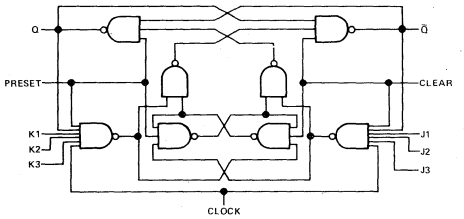
functional block diagrams



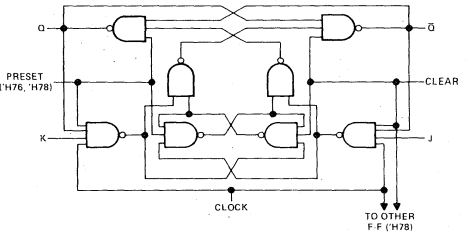
'H71—GATED J-K WITH PRESET

Same functional block diagram as for '74, see page 122.

'H74—DUAL D WITH CLEAR AND PRESET



'H72—GATED J-K WITH CLEAR AND PRESET



'H73—DUAL J-K WITH CLEAR
'H76—DUAL J-K WITH CLEAR AND PRESET
'H78—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SERIES 54H/74H	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54H	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74H	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−500			−500			−500			−500	μA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		10			10			10			10			ns
	Clock low		15			15			15			15			
	Clear or preset low		16			16			16			16			
Setup time, t_{setup}	High-level data		10↓			10↓			10↓			10↓			ns
	Low-level data		13↓			13↓			13↓			13↓			
Hold time, t_{hold}			0↓			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54H	−55		125	−55		125	−55		125	−55		125	°C
		Series 74H	0		70	0		70	0		70	0		70	

↓The arrow indicates that the falling edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'H101			'H102, 'H106			'H103			'H108			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			2			2			V
V_{IL} Low-level input voltage					0.8			0.8			0.8			0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −8 mA			*−1.5			*−1.5			*−1.5			*−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −500 μA	2.4	3.4		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH} High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V			50			50			50			50	μA
	Clear							100			100			200	
	Preset				100			100						100	
	Clock		0		−1	0		−1	0		−1	0		−1	mA
I_{IL} Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.4 V		−1	−2		−1	−2		−1	−2		−1	−2	mA
	Clear						−1	−2		−1	−2		−2	−4	
	Preset			−1	−2		−1	−2					−1	−2	
	Clock			−3	−4.8		−3	−4.8		−3	−4.8		−6	−9.6	
I_{OS} Short-circuit output current♦		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		20	38		20	38		20	38		20	38	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

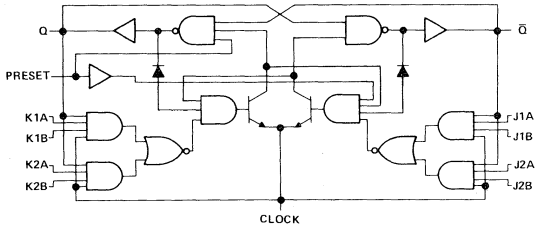
*The input clamp voltage specification is effective for Series 54H/74H parts date-coded 7332 or higher.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

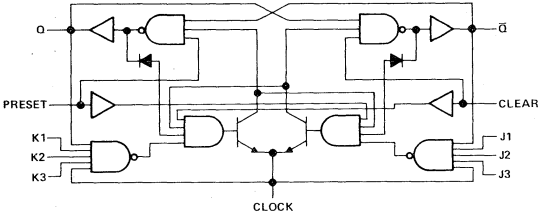
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 25 pF, R_L = 280 Ω, See Note 2	40	50		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			8	12	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			15	20	ns
	Preset or clear (clock low)				23	35	
t_{PLH}	Clock	Q or $\overline{Q}$		5	10	15	ns
t_{PHL}				8	16	20	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 148.

functional block diagrams

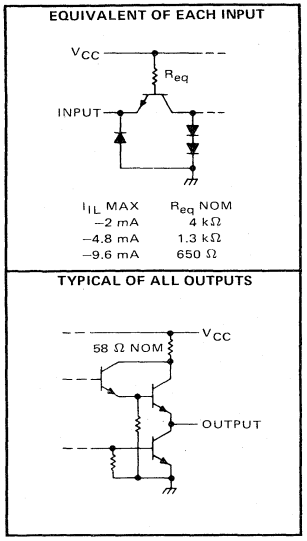


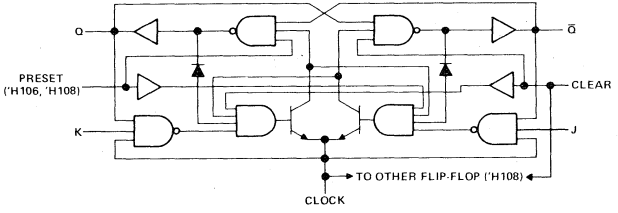
'H101—GATED J-K WITH PRESET



'H102—GATED J-K WITH CLEAR AND PRESET

schematics of inputs and outputs





'H103—DUAL J-K WITH CLEAR
'H106—DUAL J-K WITH CLEAR AND PRESET
'H108—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SERIES 54L/74L	'L71			'L72, 'L73			'L74			'L78			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54L	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74L	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		Series 54L			−100			−100			−100			−100	μA
		Series 74L			−200			−200			−200			−200	
Low-level output current, I_{OL}		Series 54L			2			2			2			2	mA
		Series 74L			3.6			3.6			3.6			3.6	
Pulse width, t_w	Clock high		200			200			200			200			ns
	Clock low		200			200			200			200			
	Clear or preset low		100			100			100			100			
Setup time, t_{setup}			0↑			0↑			50↑			0↑			ns
Hold time, t_{hold}			0↓			0↓			0↑			0↓			ns
Operating free-air temperature, T_A		Series 54L	−55		125	−55		125	−55		125	−55		125	°C
		Series 74L	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	'L71			'L72, 'L73			'L74			'L78			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			2			2			V
V_{IL} Low-level input voltage	Clock input				0.6			0.6			0.7			0.6	V
	All other inputs				0.7			0.7			0.7			0.7	
V_{OH} High-level output voltage	Series 54L	V_{CC} = MIN, V_{IH} = 2 V,	2.4	3.3		2.4	3.3		2.4	3.3		2.4	3.3		V
	Series 74L	V_{IL} = V_{IL} max, I_{OH} = MAX	2.4	3.2		2.4	3.2		2.4	3.2		2.4	3.2		
V_{OL} Low-level output voltage	Series 54L	V_{CC} = MIN, V_{IH} = 2 V,		0.15	0.3		0.15	0.3		0.15	0.3		0.15	0.3	V
	Series 74L	V_{IL} = V_{IL} max, I_{OL} = MAX		0.2	0.4		0.2	0.4		0.2	0.4		0.2	0.4	
I_I Input current at maximum input voltage	R, S, J, K, or D	V_{CC} = MAX, V_I = 5.5 V			100			100			100			100	μA
	Clear				200			200			300			400	
	Preset				200			200			200			200	
	Clock				200			200			200			400	
I_{IH} High-level input current	R, S, J, K, or D	V_{CC} = MAX, V_I = 2.4 V			10			10			10			10	μA
	Clear				20			20			30			40	
	Preset				20			20			20			20	
	Clock				−200			−200			20			−400	
I_{IL} Low-level input current	R, S, J, K, or D	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18			−0.18			−0.18	mA
	Clear				−0.36			−0.36			−0.36			−0.72	
	Preset				−0.36			−0.36			−0.18			−0.36	
	Clock				−0.36			−0.36			−0.36			−0.72	
I_{OS} Short-circuit output current		V_{CC} = MAX	−3		−15	−3		−15	−3		−15	−3		−15	mA
I_{CC} Supply current (Average per flip-flop)		V_{CC} = MAX, See Note 1		0.76	1.44		0.76	1.44		0.8	1.5		0.76	1.44	mA

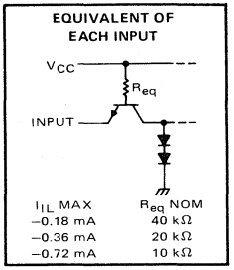
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

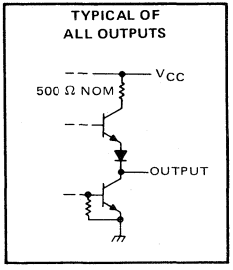
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'L71, 'L72, 'L73, 'L78			'L74			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 50 pF, R_L = 4 kΩ, See Note 2	2.5	3		2.5	3		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			35	75		50	75	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			60	150		80	150	ns
	Preset or clear (clock low)					200		80	150	
t_{PLH}	Clock	Q or $\overline{Q}$		10	35	75	10	65	100	ns
t_{PHL}				10	60	150	10	65	150	

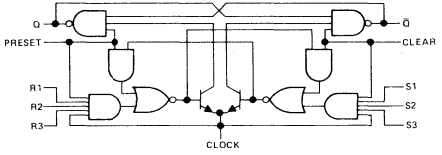
¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 149.

schematics of inputs and outputs

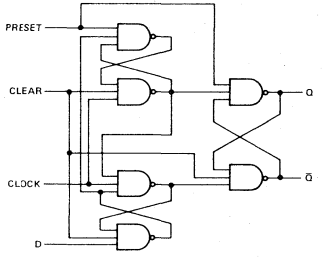




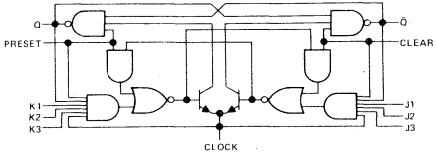
functional block diagrams



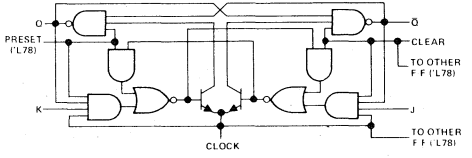
'L71—GATED R-S WITH CLEAR AND PRESET



'L74—DUAL D WITH CLEAR AND PRESET



'L72—GATED J-K WITH CLEAR AND PRESET



'L73—DUAL J-K WITH CLEAR
'L78—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

recommended operating conditions

		SERIES 54LS/74LS	'LS73, 'LS113			'LS74			'LS76, 'LS112			'LS78, 'LS114			'LS109			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54LS	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74LS	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−400			−400			−400			−400	μA
Low-level output current, I_{OL}		Series 54LS			4			4			4			4			4	mA
		Series 74LS			8			8			8			8			8	
Clock frequency, f_{clock}			0		30	0		25	0		30	0		30	0		25	MHz
Pulse width, t_w	Clock high		20			25			20			20			25			ns
	Preset or clear low		25			25			25			25			25			
Setup time, t_{setup}	High-level data		20↓			25↑			20↓			20↓			20↑			ns
	Low-level data		20↓			20↑			20↓			20↓			20↑			
Hold time, t_{hold}			0↓			5↑			0↓			0↓			5↑			ns
Operating free-air temperature, T_A		Series 54LS	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74LS	0		70	0		70	0		70	0		70	0		70	

↑↓ The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'LS73, 'LS113			'LS74			'LS76, 'LS112			'LS78, 'LS114			'LS109			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			2			2			2			V
V_{IL}	Low-level input voltage	Series 54LS					0.7			0.7			0.7			0.7			0.7	V
		Series 74LS					0.8			0.8			0.8			0.8			0.8	
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5			−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	Series 54LS	V_{CC} = MIN,	V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74LS	V_{IL} = V_{IL} max,	I_{OH} = −400 μA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage	Series 54LS	V_{CC} = MIN,	V_{IH} = 2 V,		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4		0.25	0.4	V
		Series 74LS	V_{IL} = V_{IL} max,	I_{OL} = MAX		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5		0.35	0.5	
I_I	Input current at maximum input voltage	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1			0.1			0.1			0.1	mA
		Clear					0.3			0.3			0.3			0.6			0.4	
		Preset					0.3			0.2			0.3			0.3			0.2	
		Clock					0.4			0.2			0.4			0.8			0.2	
I_{IH}	High-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 2.7 V			20			20			20			20			20	μA
		Clear					60			60			60			120			80	
		Preset					60			40			60			60			40	
		Clock					80			40			80			160			40	
I_{IL}	Low-level input current	D, J, K, or $\overline{R}$	V_{CC} = MAX,	V_I = 0.4 V			−0.36			−0.4			−0.36			−0.36			−0.4	mA
		Clear					−0.8			−1.2			−0.8			−1.6			−1.6	
		Preset					−0.8			−0.8			−0.8			−0.8			−0.8	
		Clock					−0.72			−0.8			−0.72			−1.44			−0.8	
I_{OS}	Short-circuit output current◆	Series 54LS	V_{CC} = MAX		−6		−40	−6		−40	−6		−40	−6		−40	−6		−40	mA
		Series 74LS			−5		−42	−5		−42	−5		−42	−5		−42	−5		−42	
I_{CC}	Supply current (Average per flip-flop)		V_{CC} = MAX,	See Note 1		2	4		2	4		2	4		2	4		2	4	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

◆Not more than one output should be shorted at a time.

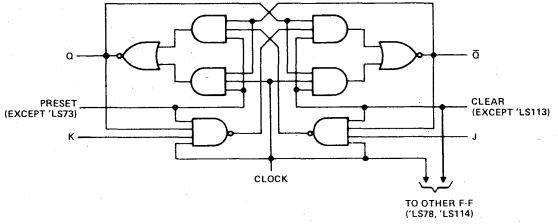
NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

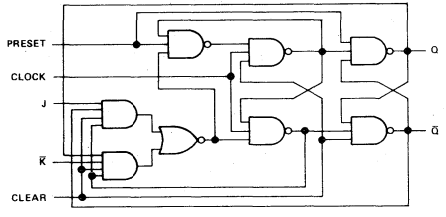
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS73, 'LS76, 'LS78 'LS112, 'LS113, 'LS114			'LS74, 'LS109			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF,	30	45		25	33		MHz
t_{PLH}	Clear, preset, or	Q or $\overline{Q}$	R_L = 2 kΩ,		11	20		13	25	ns
t_{PHL}	clock (as appropriate)		See Note 2		15	30		25	40	ns

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 149.

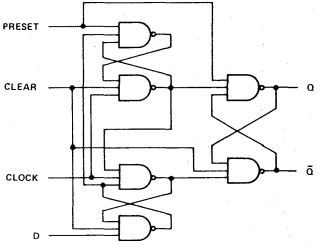
functional block diagrams and schematics of inputs and outputs



'LS73—DUAL J-K WITH CLEAR
'LS76, 'LS112—DUAL J-K WITH CLEAR AND PRESET
'LS78, 'LS114—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK
'LS113—DUAL J-K WITH PRESET

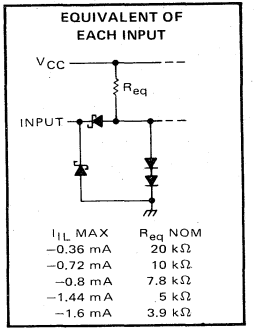


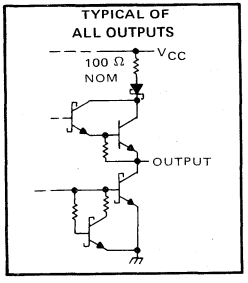
'LS109—DUAL J-$\overline{K}$ WITH CLEAR AND PRESET



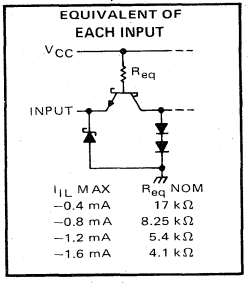
'LS74—DUAL D WITH CLEAR AND PRESET

'LS73, 'LS76, 'LS78, 'LS112, 'LS113, 'LS114





'LS74, 'LS109



recommended operating conditions

		SERIES 54S/74S	'S74			'S112			'S113			'S114			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−1			−1			−1			−1	mA
Low-level output current, I_{OL}					20			20			20			20	mA
Pulse width, t_w	Clock high		6			6			6			6			ns
	Clock low		7.3			6.5			6.5			6.5			
	Clear or preset low		7			8			8			8			
Input setup time, t_{setup}	High-level data		3↑	10		3↓			3↓			3↓			ns
	Low-level data		3↑	12		3↓			3↓			3↓			
Input hold time, t_{hold}			2↑			0↓			0↓			0↓			ns
Operating free-air temperature, T_A		Series 54S	−55		125	−55		125	−55		125	−55		125	°C
		Series 74S	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'S74			'S112			'S113			'S114			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	Series 54S	V_{CC} = MIN, V_{IH} = 2 V,	2.5	3.4		2.5	3.4		2.5	3.4		2.5	3.4		V
		Series 74S	V_{IL} = 0.8 V, I_{OH} = −1 mA	2.7	3.4		2.7	3.4		2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1			1			1	mA
I_{IH}	High-level input current	J, K, or D	V_{CC} = MAX, V_I = 2.7 V			50			50			50			50	μA
		Clear				150			100			200			200	
		Preset				100			100			100			100	
		Clock				100			100			100			200	
I_{IL}	Low-level input current	J, K, or D	V_{CC} = MAX, V_I = 0.5 V			−2			−1.6			−1.6			−1.6	mA
		Clear				−6			−7						−14	
		Preset				−4			−7			−7			−7	
		Clock				−4			−4			−4			−8	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX	−40		−100	−40		−100	−40		−100	−40		−100	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 1		15	25		15	25		15	25		15	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

♦Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.

NOTE 1: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

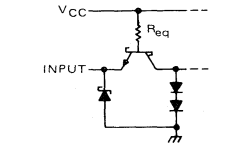
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'S74			'S112, 'S113, 'S114			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 280 Ω, See Note 2	75	110		80	125		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$			4	6	2	4	7	ns
t_{PHL}	Preset or clear (clock high)	$\overline{Q}$ or Q			9	13.5	2	5	7	ns
	Preset or clear (clock low)				5	8	2	5	7	
t_{PLH}	Clock	Q or $\overline{Q}$			6	9	2	4	7	ns
t_{PHL}					6	9	2	5	7	

¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 2: Load circuit and voltage waveforms are shown on page 148.

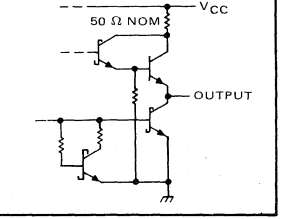
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

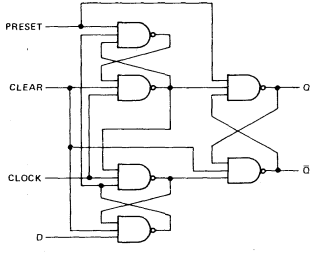


I_{IL} MAX	R_{eq} NOM
−1.6 mA	4 kΩ
−2 mA	2.8 kΩ
−4 mA	1.4 kΩ
−6 mA	940 Ω
−7 mA	900 Ω
−8 mA	700 Ω
−14 mA	450 Ω

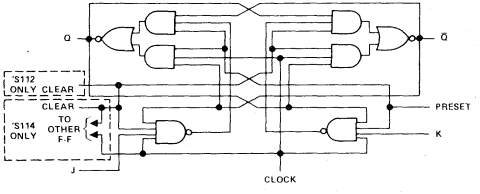
TYPICAL OF ALL OUTPUTS



functional block diagrams



'S74—DUAL D WITH CLEAR AND PRESET



'S112—DUAL J-K WITH CLEAR AND PRESET
'S113—DUAL J-K WITH PRESET
'S114—DUAL J-K WITH PRESET, COMMON CLEAR, AND COMMON CLOCK

description

These multivibrators feature dual negative-transition-triggered inputs and a single positive-transition-triggered input which can be used as an inhibit input. Complementary output pulses are provided.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for the B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with an excellent noise immunity of typically 1.2 volts. A high immunity to V_{CC} noise of typically 1.5 volts is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions of the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse length may be varied from 40 nanoseconds to 28 seconds by choosing appropriate timing components. With no external timing components (i.e., R_{int} connected to V_{CC}, C_{ext} and R_{ext}/C_{ext} open), an output pulse of typically 30 or 35 nanoseconds is achieved which may be used as a d-c triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 30 kΩ for the SN54121/SN54L121 and 2 kΩ to 40 kΩ for the SN74121/SN74L121). Throughout these ranges, pulse width is defined by the relationship $t_{w(out)} = C_T R_T \ln 2 \approx 0.7\, C_T R_T$. In circuits where pulse cutoff is not critical, timing capacitance up to 1000 μF and timing resistance as low as 1.4 kΩ may be used. Also, the range of jitter-free output pulse widths is extended if V_{CC} is held to 5 volts and free-air temperature is 25°C. Duty cycles as high as 90% are achieved when using maximum recommended R_T. Higher duty cycles are available if a certain amount of pulse-width jitter is allowed.

recommended operating conditions

		54 FAMILY / 74 FAMILY	SN54121 / SN74121			SN54L121 / SN74L121			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−200	μA
Low-level output current, I_{OL}					16			8	mA
Rate of rise or fall of input pulse, dv/dt	Schmitt input, B		1			1			V/s
	Logic inputs, A1, A2		1			1			V/μs
Input pulse width, $t_{w(in)}$			50			100			ns
External timing resistance, R_{ext}		54 Family	1.4		30	1.4		30	kΩ
		74 Family	1.4		40	1.4		40	
External timing capacitance, C_{ext}			0		1000	0		1000	μF
Duty cycle	R_T = 2 kΩ				67			67	%
	R_T = MAX R_{ext}				90			90	
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54121 SN74121			SN54L121 SN74L121			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{T+}	Positive-going threshold voltage at A input	V_{CC} = MIN			1.4	2		1.4	2	V
V_{T-}	Negative-going threshold voltage at A input	V_{CC} = MIN		0.8	1.4		0.8	1.4		V
V_{T+}	Positive-going threshold voltage at B input	V_{CC} = MIN			1.55	2		1.55	2	V
V_{T-}	Negative-going threshold voltage at B input	V_{CC} = MIN		0.8	1.35		0.8	1.35		V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			*−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = MAX	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = MAX		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	A1 or A2			40			20	μA
			B			80			40	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	A1 or A2			−1.6			−0.8	mA
			B			−3.2			−1.6	
I_{OS}	Short-circuit output current♦	V_{CC} = MAX	54 Family	−20		−55	−10		−27	mA
			74 Family	−18		−55	−9		−27	
I_{CC}	Supply current	V_{CC} = MAX	Quiescent		13	25		7	12	mA
			Triggered		23	40		9	20	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦Not more than one output should be shorted at a time.
*The input clamp voltage specification is effective for Series 54/74 parts date-coded 7332 or higher.

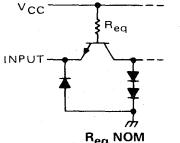
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		'121			'L121			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level Q output from either A input	C_L = 15 pF, R_L = 400 Ω for '121, R_L = 800 Ω for 'L121, See Note 1	C_T = 80 pF, R_{int} to V_{CC}	25	45	70			140	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from B input			15	35	55			110	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from either A input			30	50	80			160	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output from B input			20	40	65			130	ns
$t_{w(out)}$	Pulse width obtained using internal timing resistor		C_T = 80 pF, R_{int} to V_{CC}	70	110	150	70	225	260	ns
$t_{w(out)}$	Pulse width obtained with zero timing capacitance		C_T = 0, R_{int} to V_{CC}	20	30	50	20	35	70	ns
$t_{w(out)}$	Pulse width obtained using external timing resistor		C_T = 100 pF, R_T = 10 kΩ	600	700	800	600	700	850	ns
			C_T = 1 μF, R_T = 10 kΩ	6	7	8	6	7	8	ms

NOTE 1: Load circuit and voltage waveforms are shown on page 148.

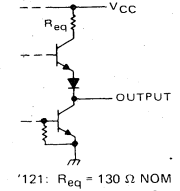
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



INPUT	'121	'L121
	R_{eq} NOM	
A1	4 kΩ	8 kΩ
A2	4 kΩ	8 kΩ
B	2 kΩ	4 kΩ

TYPICAL OF BOTH OUTPUTS



'121: R_{eq} = 130 Ω NOM
'L121: R_{eq} = 260 Ω NOM

TYPICAL CHARACTERISTICS§

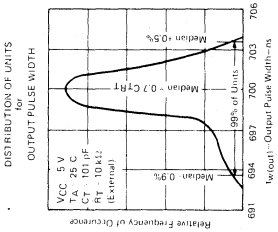


FIGURE 1

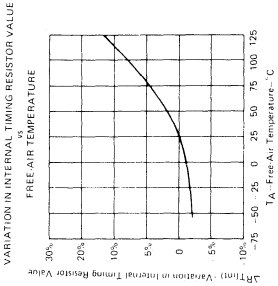


FIGURE 2

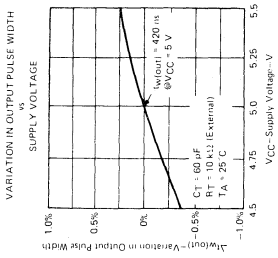


FIGURE 3

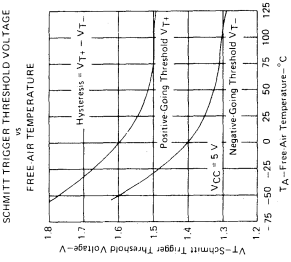


FIGURE 5

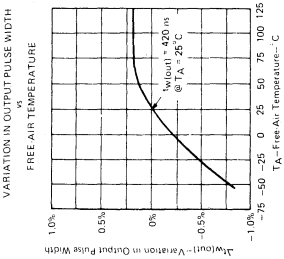


FIGURE 4

§ Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121 only.

TYPICAL CHARACTERISTICS§ (continued)

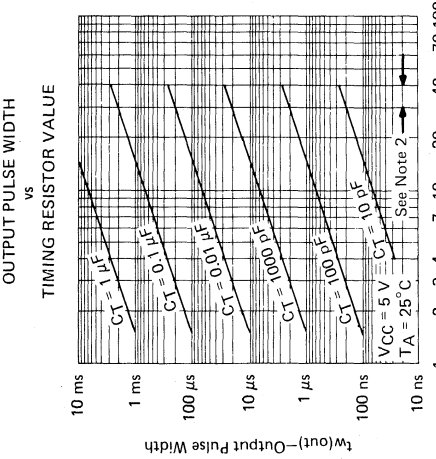


FIGURE 6

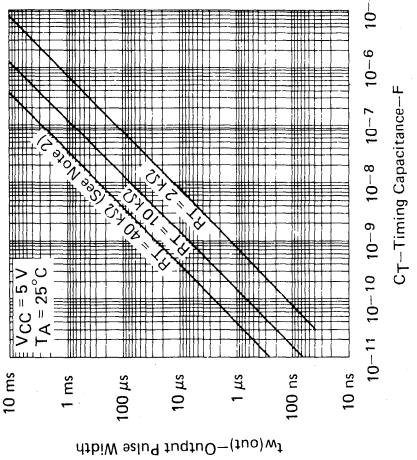
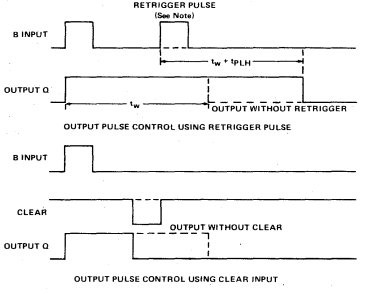


FIGURE 7

§Data for temperatures below 0°C and above 70°C are applicable for SN54121 and SN54L121 only.
NOTE 2: These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54121 and SN54L121.

description

The '122, '123, 'L122, and 'L123 multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.



NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

FIGURE A–TYPICAL INPUT/OUTPUT PULSES

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. The '122 and 'L122 each has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths (up to 28 seconds) and not requiring the clear feature can best be satisfied with '121 or 'L121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_W) is defined as:

$$t_W = K \cdot R_T \cdot C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor),
C_{ext} is in pF,
t_w is in ns,
K is 0.32 for '122, 0.28 for '123, 0.37 for 'L122, 0.33 for 'L123.

For pulse widths when $C_{ext} \leq 1000$ pF, see Figures B and C.

'122, '123
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

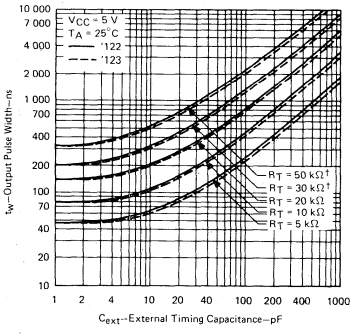


FIGURE B

'L122
TYPICAL OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

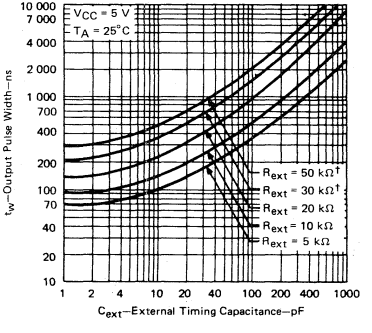


FIGURE C

†These values of resistance exceed the maximum recommended for use over the full temperature range of the SN54' and SN54L' circuits.

recommended operating conditions

		54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '122, '123			SERIES 54L / SERIES 74L 'L122, 'L123			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−800			−400	μA
Low-level output current, I_{OL}					16			8	mA
Pulse width, t_w	A or B inputs high		40			50			ns
	A or B inputs low		40			50			
	Clear low		40			50			
External timing resistance, R_{ext}		54 Family	5		25	5		25	kΩ
		74 Family	5		50	5		50	
External capacitance, C_{ext}			No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal					50			50	pF
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SERIES 54 / SERIES 74 '122, '123			SERIES 54L / SERIES 74L 'L122, 'L123			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX, See Note 1	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX, See Note 1		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Data inputs	V_{CC} = MAX, V_I = 2.4 V			40			20	μA
		Clear input				80			40	
I_{IL}	Low-level input current	Data inputs	V_{CC} = MAX, V_I = 0.4 V			−1.6			−0.8	mA
		Clear input				−3.2			−1.6	
I_{OS}	Short-circuit output current♦		V_{CC} = MAX, See Note 1	−10		−40	−5		−20	mA
I_{CC}	Supply current (quiescent or triggered)	'122, 'L122	V_{CC} = MAX, See Notes 2 and 3		23	28		11	14	mA
		'123, 'L123			46	66		23	33	

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦*Not more than one output should be shorted at a time.*

NOTES: 1. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
2. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 or 'L122 is open.
3. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of '122 or 'L122 is open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 4

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	'122, '123 TEST CONDITIONS	'122, '123 MIN	'122, '123 TYP	'122, '123 MAX	'L122, 'L123 TEST CONDITIONS	'L122, 'L123 MIN	'L122, 'L123 TYP	'L122, 'L123 MAX	UNIT
t_{PLH}	A	Q	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 400 Ω		22	23	C_{ext} = 0, R_{ext} = 5 kΩ, C_L = 15 pF, R_L = 800 Ω		44	66	ns
	B				19	28			38	56	
t_{PHL}	A	$\overline{Q}$			30	40			60	80	ns
	B				27	36			54	72	
t_{PHL}	Clear	Q			18	27			36	54	ns
t_{PLH}		$\overline{Q}$			30	40			60	80	
t_{wQ} (min)	A or B	Q			45	65			90★	130★	ns
t_{wQ}	A or B	Q	C_{ext} = 1000 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 400 Ω		'122		C_{ext} = 400 pF, R_{ext} = 10 kΩ, C_L = 15 pF, R_L = 800 Ω		'L122		μs
				3.08	3.42	3.76		1.7	1.9	2.1	
					'123				'L123		
				2.76	3.03	3.37		1.5★		2.1★	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{wQ} ≡ width of pulse at output Q
★These values for 'L123 are tentative.
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

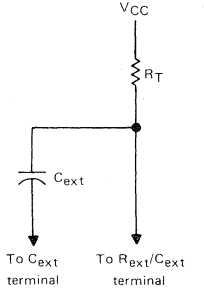
TYPICAL APPLICATION DATA

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure E be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

$$t_W = K_D \cdot R_{ext} \cdot C_{ext} \left(1 + \frac{0.7}{R_{ext}}\right)$$

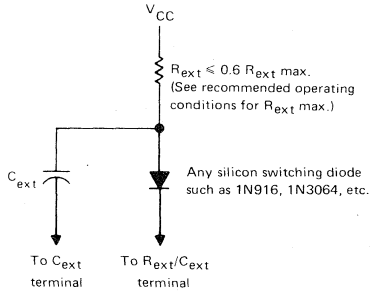
where

R_{ext} is in kΩ,
C_{ext} is in pF,
t_W is in ns,
K_D is 0.28 for '122, 0.25 for '123, 0.33 for 'L122, and 0.29 for 'L123.



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} \leq$ 1000 pF

FIGURE D



TIMING COMPONENT CONNECTIONS WHEN $C_{ext} >$ 1000 pF AND CLEAR IS USED

FIGURE E

recommended operating conditions

	SN54279			SN74279			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54279	−18		−55	mA
			SN74279	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 1			18	30	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 1: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5 V, and all outputs open.

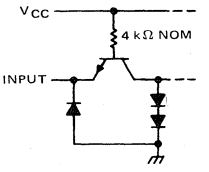
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{S}$ input	C_L = 15 pF, R_L = 400 Ω, See Note 2		12	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{S}$ input			9	15	
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{R}$ input			15	27	

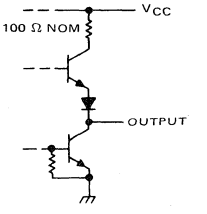
NOTE 2: Load circuit and voltage waveforms are shown on page 148.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



recommended operating conditions

		54 FAMILY / 74 FAMILY	SERIES 54 / SERIES 74 '125, '126			SERIES 54S / SERIES 74S 'S134			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		54 Family	4.5	5	5.5	4.5	5	5.5	V
		74 Family	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}		54 Family			−2			−2	mA
		74 Family			−5.2			−6.5	
Low-level output current, I_{OL}					16			20	mA
Operating free-air temperature, T_A		54 Family	−55		125	−55		125	°C
		74 Family	0		70	0		70	

supply current¶

TYPE	TEST CONDITIONS: DATA INPUTS	TEST CONDITIONS: OUTPUT CONTROLS	I_{CC} (mA): MIN	TYP	MAX
'125	0 V	4.5 V		32	54
'126	0 V	0 V		36	62
'S134	0 V	0 V		7	13
	5 V	0 V		9	16
	5 V	5 V		14	25

¶Maximum values of I_{CC} are over the recommended operating ranges of V_{CC} and T_A; typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES 54 / SERIES 74 '125, '126 MIN	TYP‡	MAX	SERIES 54S / SERIES 74S 'S134 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1, 2			2			2			V
V_{IL}	Low-level input voltage	1, 2					0.8			0.8	V
V_I	Input clamp voltage	3	V_{CC} = MIN,	I_I = §			−1.5			−1.2	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	54 Family	2.4	3.3		2.4	3.4		V
				74 Family	2.4	3.1		2.4	3.2		
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = MAX			0.4			0.5	V
$I_{O(off)}$	Off-state (high-impedance state) output current	19	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			40			50	μA
				V_O = 0.4 V			−40				
				V_O = 0.5 V						−50	
I_I	Input current at maximum input voltage	4	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX	V_{IH} = 2.4 V			40				μA
				V_{IH} = 2.7 V						50	
I_{IL}	Low-level input current	5	V_{CC} = MAX	V_{IL} = 0.4 V			−1.6				mA
				V_{IL} = 0.5 V						−2	
I_{OS}	Short-circuit output current♦	6	V_{CC} = MAX	54 Family	−30		−70	−40		−100	mA
				74 Family	−28		−70	−40		−100	
I_{CC}	Supply current	7	V_{CC} = MAX		See table						mA

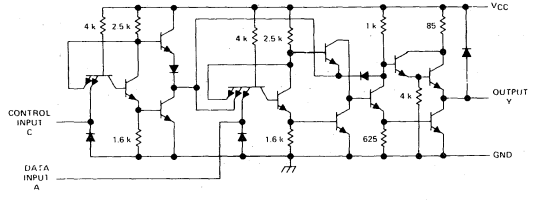
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§I_I = −12 mA for SN54'/SN74' and −18 mA for SN54S'/SN74S'.
♦Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

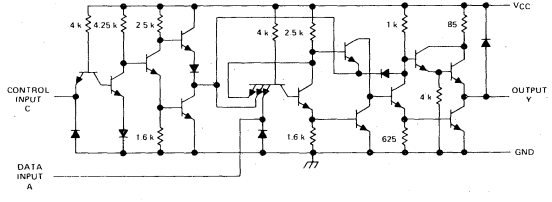
PARAMETER	TEST CONDITIONS#	SERIES 54/74 '125 MIN	'125 TYP	'125 MAX	'126 MIN	'126 TYP	'126 MAX	SERIES 54S/74S TEST CONDITIONS#	'S134 MIN	'S134 TYP	'S134 MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 400 Ω		8	13		8	13	C_L = 15 pF, R_L = 280 Ω	2	4	6	ns
								C_L = 50 pF, R_L = 280 Ω		5.5		
t_{PHL} Propagation delay time, high-to-low-level output			12	18		12	18	C_L = 15 pF, R_L = 280 Ω	2	5	7.5	ns
								C_L = 50 pF, R_L = 280 Ω		7		
t_{ZH} Output enable time to high level			11	17		11	18	C_L = 50 pF, R_L = 280 Ω		13	19.5	ns
t_{ZL} Output enable time to low level			16	25		16	25			14	21	ns
t_{HZ} Output disable time from high level	C_L = 5 pF, R_L = 400 Ω		5	8		10	16	C_L = 5 pF, R_L = 280 Ω		5.5	8.5	ns
t_{LZ} Output disable time from low level			7	12		12	18			9	14	ns

#Load circuit and voltage waveforms are shown on page 148.

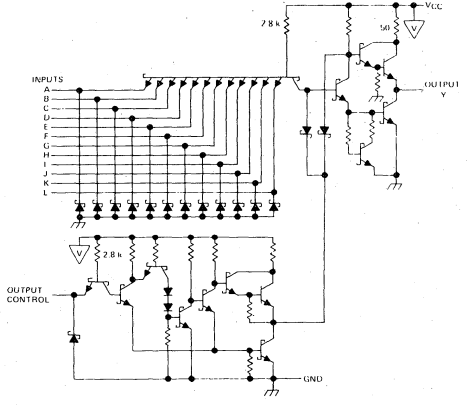
schematics (each gate)



'125 CIRCUITS



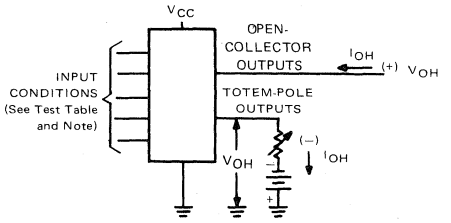
'126 CIRCUITS



'S134 CIRCUITS

Resistor values shown are nominal and in ohms.

PARAMETER MEASUREMENT INFORMATION

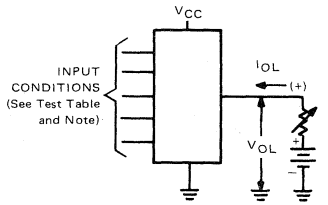


NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	Input under test at V_{IL} max, all others at 4.5 V
AND	All inputs at V_{IH} min
NOR	All inputs at V_{IL} max
OR	Input under test at V_{IH} min, all others at GND
AND-OR-INVERT	Inputs under test (a set including one input of each AND gate) at V_{IL} max, all others at 4.5 V
AND-OR	All inputs of AND gate under test at V_{IH} min, all others at GND

FIGURE 1–V_{IH}, V_{IL}, V_{OH}, I_{OH}

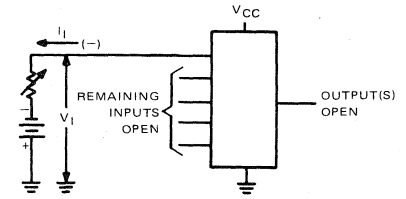


NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

TEST TABLE

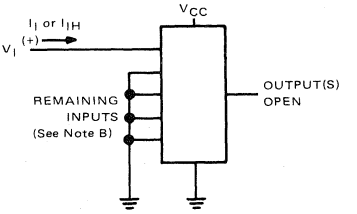
FUNCTION	INPUT CONDITIONS
NAND	All inputs at V_{IH} min
AND	Input under test at V_{IL} max, all others at 4.5 V
NOR	Input under test at V_{IH} min, others at GND
OR	All inputs at V_{IL} max
AND-OR-INVERT	All inputs of AND gate under test at V_{IH} min, all others at GND
AND-OR	Inputs under test (a set including one input of each AND gate) at V_{IH} min, all others at 4.5 V

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



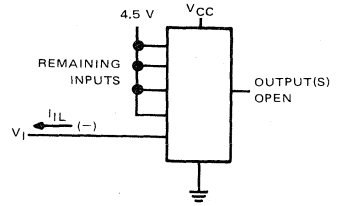
NOTE: Each input is tested separately.

FIGURE 3–V_I



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open when testing I_I and grounded when testing I_{IH}.

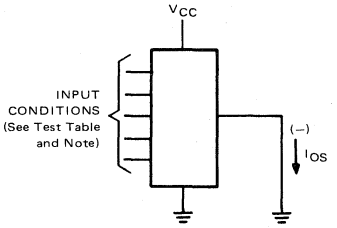
FIGURE 4–I_I, I_{IH}



NOTES: A. Each input is tested separately.
B. When testing AND-OR-INVERT or AND-OR gates, each AND gate is tested separately with inputs of AND gates not under test open.

FIGURE 5–I_{IL}

PARAMETER MEASUREMENT INFORMATION

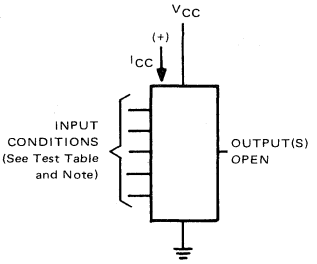


TEST TABLE

FUNCTION	INPUT CONDITIONS
NAND	All inputs at GND
AND	All inputs at 4.5 V
NOR	All inputs at GND
OR	All inputs at 4.5 V
AND-OR-INVERT	All inputs at GND
AND-OR	All inputs at 4.5 V

NOTE: For functions having three-state outputs, input conditions are maintained which will cause the outputs to be enabled (low-impedance).

FIGURE 6–I_{OS}



TEST TABLE

FUNCTION	INPUT CONDITIONS FOR I_{CCH}	INPUT CONDITIONS FOR I_{CCL}
NAND	All inputs at GND	All inputs at 4.5 V
AND	All inputs at 4.5 V	All inputs at GND
NOR	All inputs at GND	One input at 4.5 V, all others at GND
OR	One input at 4.5 V, all others at GND	All inputs at GND
AND-OR-INVERT	All inputs at GND	All inputs of one AND gate at 4.5 V, all others at GND
AND-OR	All inputs of one AND gate at 4.5 V, all others at GND	All inputs at GND

NOTE: I_{CC} is measured simultaneously for all functions in a package. The average-per-gate values are calculated from the appropriate one of the following equations:

$$I_{CC},\ I_{CCH},\ \text{or}\ I_{CCL}\ \text{(average per gate or flip-flop)} = \frac{\text{total } I_{CC},\ I_{CCH},\ \text{or } I_{CCL}}{\text{(number of gates or flip-flops in package)}}$$

$$I_{CC}\ \text{(average per gate, 50\% duty cycle)} = \frac{I_{CCH} + I_{CCL}}{2\ \text{(number of gates in package)}}$$

FIGURE 7–I_{CC}

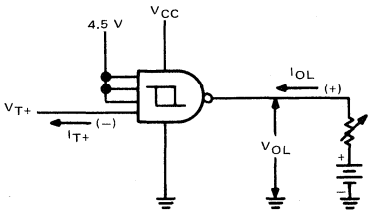


FIGURE 8–V_{T+}, I_{T+}, V_{OL} (FOR NAND SCHMITT TRIGGERS)

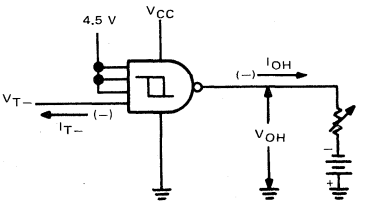
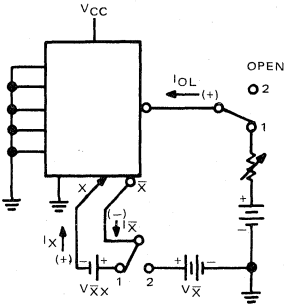


FIGURE 9–V_{T-}, I_{T-}, V_{OH} (FOR NAND SCHMITT TRIGGERS)

PARAMETER MEASUREMENT INFORMATION



NOTES: A. Switches are in position 1 for SN54'/SN74', position 2 for SN54H'/SN74H'.

B. The $I_{\overline{X}}$ limit for SN54' and SN74' circuits may be verified by an alternate equivalent procedure. The $V_{\overline{X}X}$ source is replaced by a resistor (138 Ω for SN54', 130 Ω for SN74') in parallel with a voltmeter between the X and $\overline{X}$ pins. If the measured voltage, $V_{\overline{X}X}$, is less than 0.4 V, the specified limit for $I_{\overline{X}}$ is met.

FIGURE 10–$I_{\overline{X}}$ (FOR EXPANDABLE GATES)

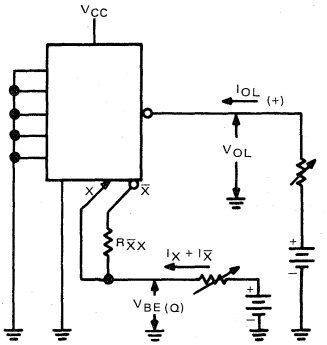


FIGURE 11–$V_{BE(Q)}$ (FOR EXPANDABLE GATES)

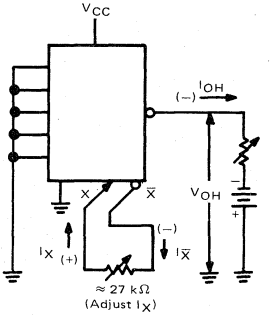


FIGURE 12–V_{OH} (FOR EXPANDABLE GATES)

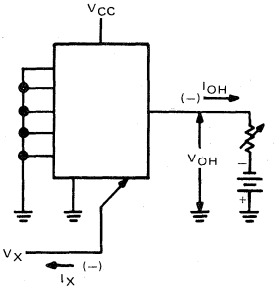


FIGURE 13–V_{OH} (FOR EXPANDABLE GATES)

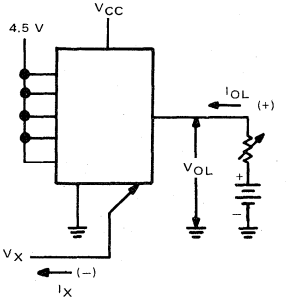


FIGURE 14–V_{OL} (FOR EXPANDABLE GATES)

PARAMETER MEASUREMENT INFORMATION

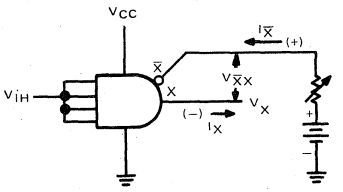


FIGURE 15–ON-STATE CHARACTERISTICS FOR EXPANDERS

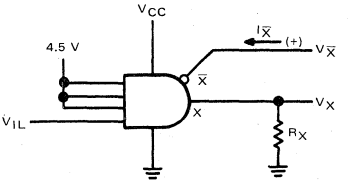


FIGURE 16–OFF-STATE CHARACTERISTICS FOR EXPANDERS

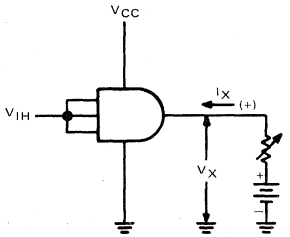


FIGURE 17–ON-STATE CHARACTERISTICS FOR EXPANDERS

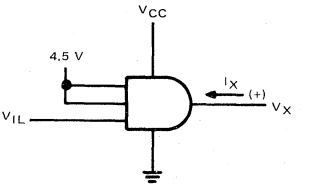
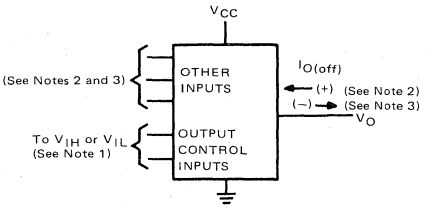


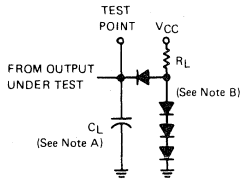
FIGURE 18–OFF-STATE CHARACTERISTICS FOR EXPANDERS



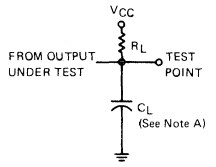
NOTES: 1. Input conditions are maintained which will ensure that the three-state output(s) is (are) disabled to the high-impedance state. See function table or logic for the particular device.
2. When testing for current into the output with a high-level output voltage, input conditions are applied that would cause the output to be low if it were enabled.
3. When testing for current out of the output with a low-level output voltage, input conditions are applied that would cause the output to be high if it were enabled.

FIGURE 19–$I_{O(off)}$ (THREE-STATE OUTPUTS)

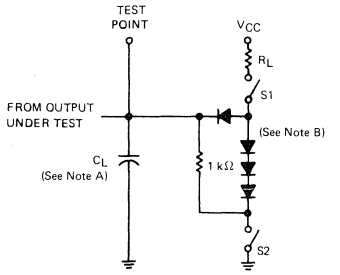
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



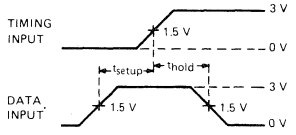
LOAD CIRCUIT FOR OPEN-COLLOCTOR OUTPUTS



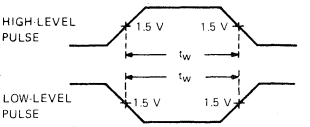
LOAD CIRCUIT FOR THREE-STATE OUTPUTS

2

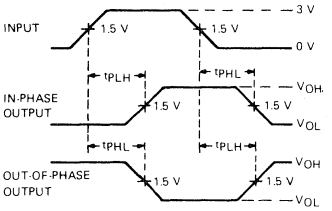
NOTES. A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.



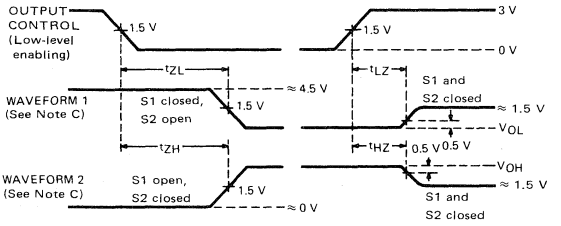
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

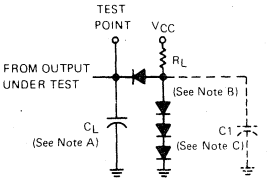


VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

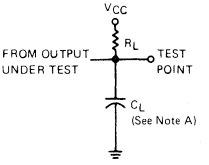
NOTES: C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$ and:
For Series 54/74 and 54H/74H, $t_r \leq 7$ ns, $t_f \leq 7$ ns;
For Specified† Series 54L/74L devices: $t_r \leq 10$ ns, $t_f \leq 10$ ns;
For Series 54S/74S, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

†'L42, 'L43, 'L44, 'L46, 'L47, 'L75, 'L77, 'L96, 'L121, 'L122, 'L123, 'L153, 'L154, 'L157, 'L164

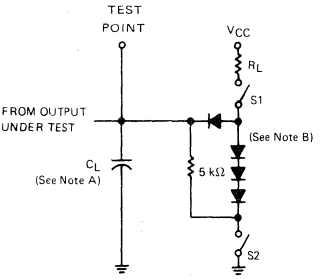
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

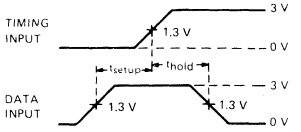


LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

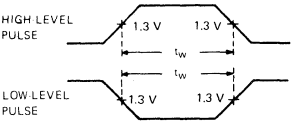


LOAD CIRCUIT FOR THREE-STATE OUTPUTS

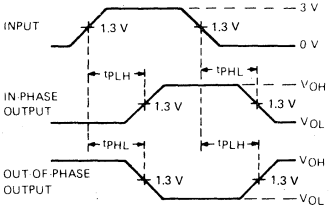
NOTES A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N3064.
C. C1 (30 pF) is used for testing Series 54L/74L devices only.



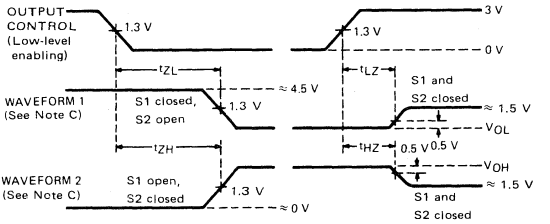
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS

NOTES: D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
E. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
F. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$ and:
For Series 54L/74L gates and inverters, t_r = 60 ns, t_f = 60 ns;
For Series 54L/74L flip-flops and MSI, $t_r \leq 25$ ns, $t_f \leq 25$ ns;
For Series 54LS/74LS, $t_r \leq 15$ ns, $t_f \leq 6$ ns.

†Except 'L42, 'L43, 'L44, 'L46, 'L47, 'L75, 'L77, 'L96, 'L121, 'L122, 'L123, 'L153, 'L154, 'L157, 'L164

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

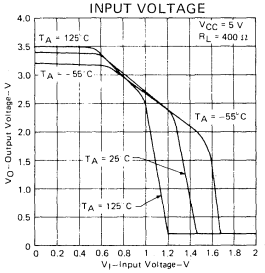


FIGURE A1

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

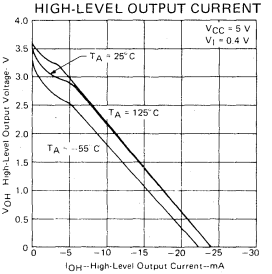


FIGURE A2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

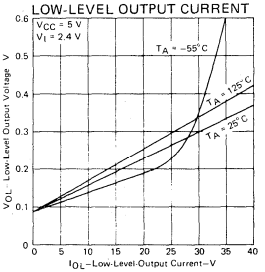


FIGURE A3

AVERAGE PROPAGATION DELAY TIME,
vs
FREE-AIR TEMPERATURE

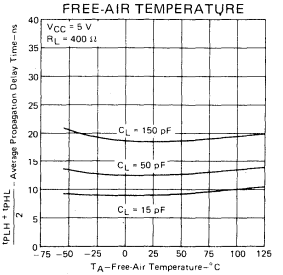


FIGURE A4

PROPAGATION DELAY TIME,
LOW-TO-HIGH LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

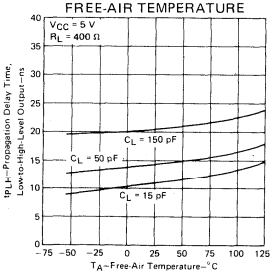


FIGURE A5

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

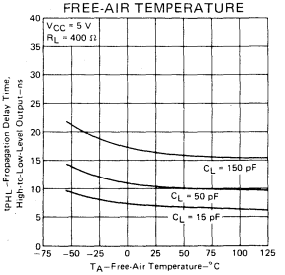


FIGURE A6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54 circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

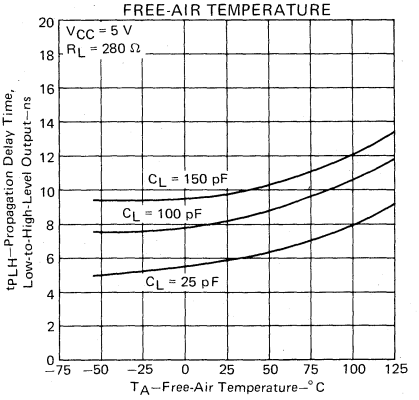


FIGURE B1

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

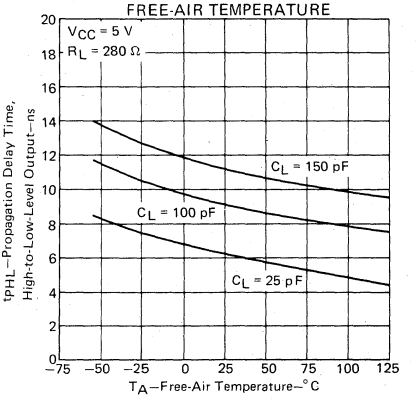


FIGURE B2

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

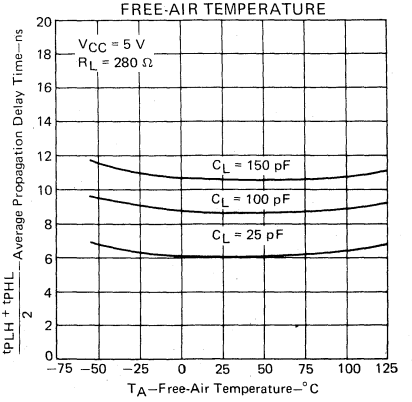


FIGURE B3

†Data for temperatures below 0°C and above 70°C are applicable for Series 54H circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

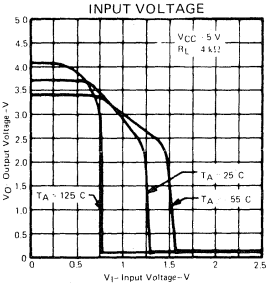


FIGURE C1

OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

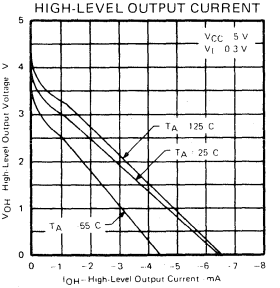


FIGURE C2

OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

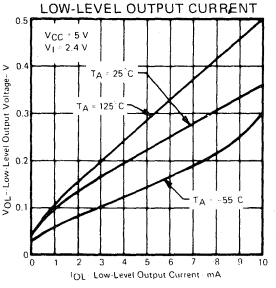


FIGURE C3

CLOCK INPUT CURRENT PER FLIP-FLOP
vs
INPUT VOLTAGE

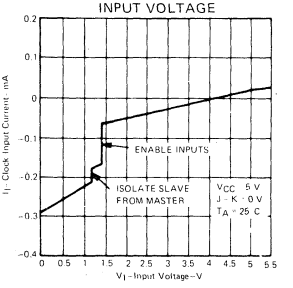


FIGURE C4

POWER DISSIPATION PER FLIP-FLOP
vs
FREQUENCY

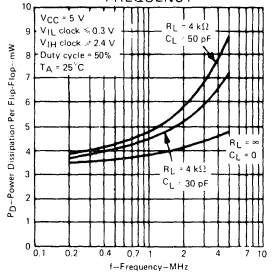


FIGURE C5

AVERAGE TOTAL D-C POWER DISSIPATION
PER FLIP-FLOP
vs
FREE-AIR TEMPERATURE

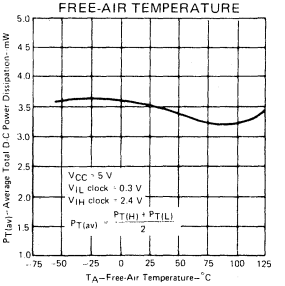


FIGURE C6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54L circuits only.
§Unless otherwise noted, data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

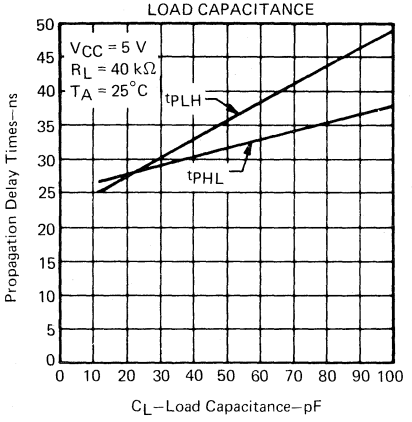


FIGURE C7

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

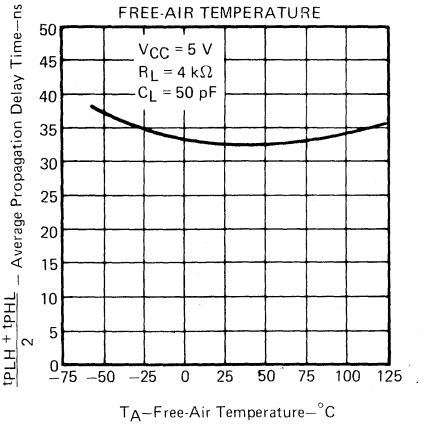


FIGURE C8

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

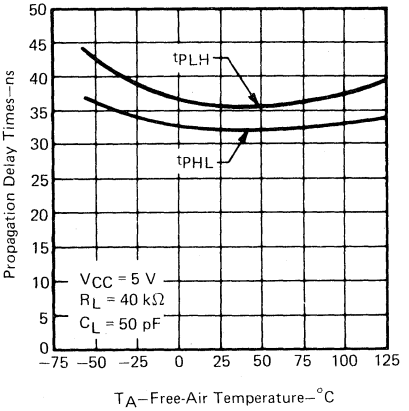


FIGURE C9

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

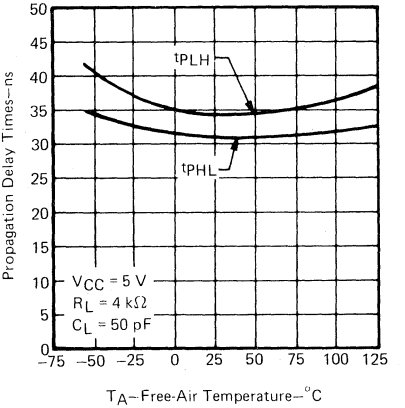


FIGURE C10

†Data for temperatures below 0°C and above 70°C are applicable for Series 54L circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

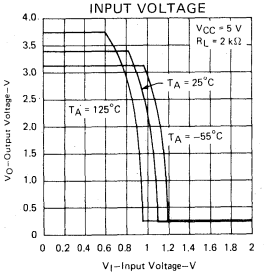


FIGURE D1

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

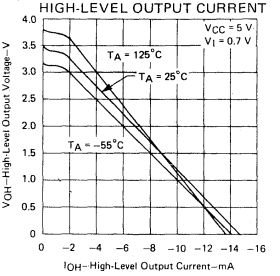


FIGURE D2

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

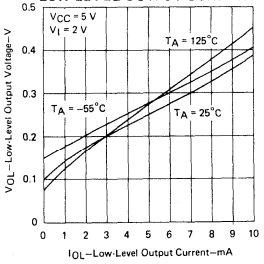


FIGURE D3

POWER DISSIPATION PER GATE
vs
FREQUENCY

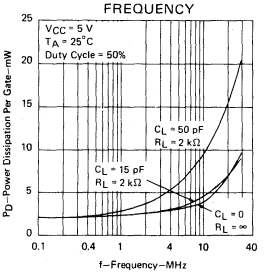


FIGURE D4

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

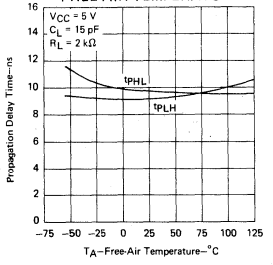


FIGURE D5

PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

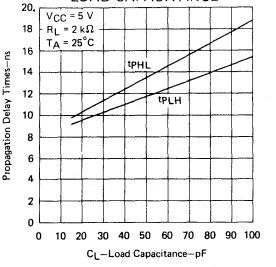


FIGURE D6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54LS circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

OUTPUT VOLTAGE
vs
INPUT VOLTAGE

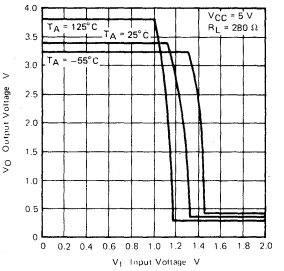


FIGURE E1

INPUT-CLAMPING-DIODE
FORWARD VOLTAGE
vs
FREE-AIR TEMPERATURE

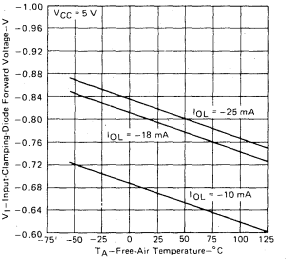


FIGURE E2

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

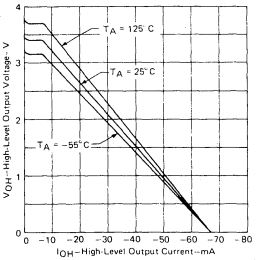


FIGURE E3

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

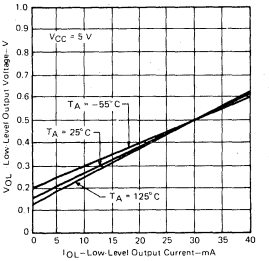


FIGURE E4

INPUT CURRENT
vs
INPUT VOLTAGE

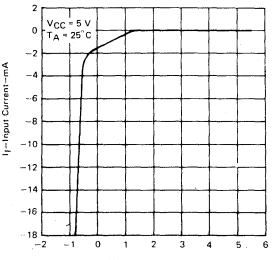


FIGURE E5

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

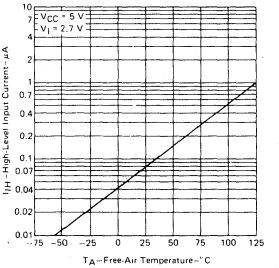


FIGURE E6

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS†§

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

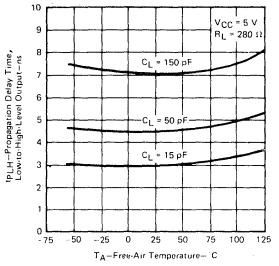


FIGURE E7

PROPAGATION DELAY TIME,
LOW-TO-HIGH-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

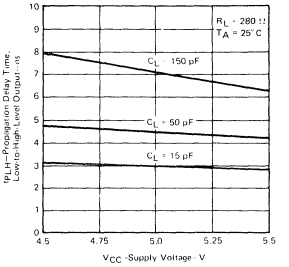


FIGURE E8

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
FREE-AIR TEMPERATURE

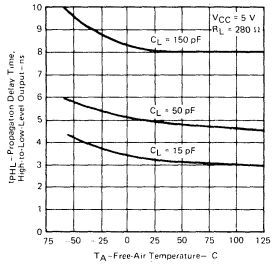


FIGURE E9

PROPAGATION DELAY TIME,
HIGH-TO-LOW-LEVEL OUTPUT
vs
SUPPLY VOLTAGE

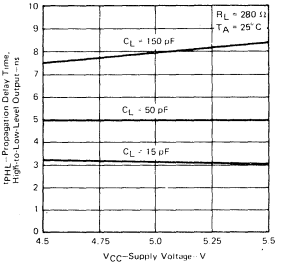


FIGURE E10

AVERAGE PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

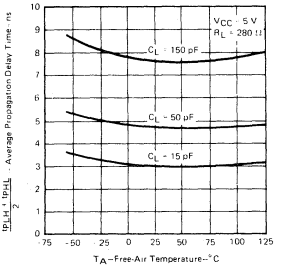


FIGURE E11

POWER DISSIPATION PER GATE
vs
FREQUENCY

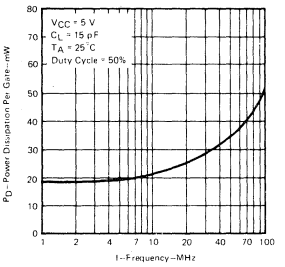


FIGURE E12

†Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.
§Data as shown are applicable specifically for the NAND gates with totem-pole outputs.

TYPICAL CHARACTERISTICS FOR FLIP-FLOPS†

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

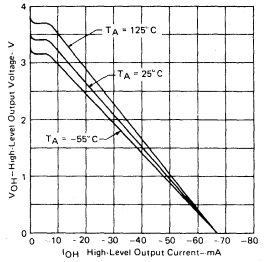


FIGURE E13

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

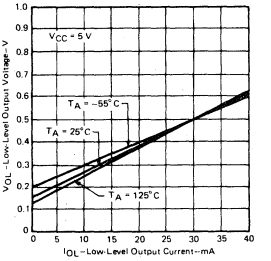


FIGURE E14

'S112, 'S113
INPUT CURRENT
vs
INPUT VOLTAGE

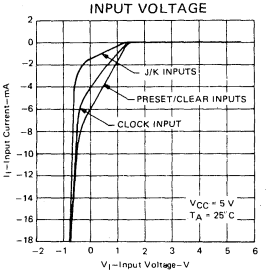


FIGURE E15

HIGH-LEVEL INPUT CURRENT
vs
FREE-AIR TEMPERATURE

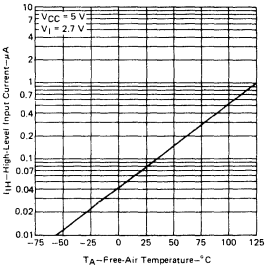


FIGURE E16

'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
FREE-AIR TEMPERATURE

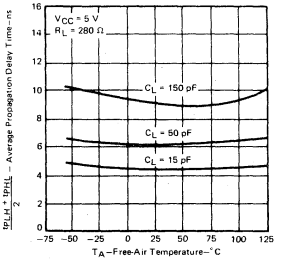


FIGURE E17

'S112, 'S113, 'S114
AVERAGE PROPAGATION DELAY TIME,
CLOCK TO OUTPUT
vs
LOAD CAPACITANCE

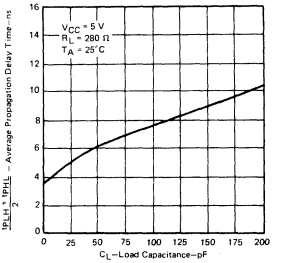


FIGURE E18

† Data for temperatures below 0°C and above 70°C are applicable for Series 54S circuits only.

2

54/74 Family
MSI/LSI Circuits

3

ADDERS

DESCRIPTION	TYPICAL CARRY TIME	TYPICAL ADD TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
SINGLE 1-BIT GATED FULL ADDERS	10.5 ns	52 ns	105 mW	SN5480	SN7480	J, N, W	187
SINGLE 2-BIT FULL ADDERS	14.5 ns	25 ns	87 mW	SN5482	SN7482	J, N, W	195
SINGLE 4-BIT FULL ADDERS	10 ns	16 ns	76 mW	SN5483A	SN7483A	J, N, W	198
	10 ns	16 ns	76 mW	SN54283	SN74283	J, N, W	494
	50 ns	33 ns	19 mW	SN54LS83	SN74LS83	J, N, W	198
DUAL 1-BIT CARRY-SAVE FULL ADDERS	11 ns	11 ns	110 mW	SN54H183	SN74H183	J, N, W	396
4-BIT ARITHMETIC LOGIC UNITS/ FUNCTION GENERATORS	7 ns	11 ns	600 mW	SN54S181	SN74S181	J, N†, W	381
	12.5 ns	24 ns	455 mW	SN54181	SN74181	J, N, W	
	16 ns	24 ns	102 mW	SN54LS181	SN74LS181	J, N, W	
LOOK-AHEAD CARRY GENERATORS	7 ns		260 mW	SN54S182	SN74S182	J, N, W	392
	13 ns		180 mW	SN54182	SN74182	J, N, W	

MULTIPLIERS

DESCRIPTION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS (8-BIT PRODUCT IN 40 ns TYPICAL)	SN54284, SN54285	SN74284, SN74285	J, N, W	496
25-MHz 6-BIT-BINARY RATE MULTIPLIERS	SN5497	SN7497	J, N†, W	248
25-MHz DECADE RATE MULTIPLIERS	SN54167	SN74167	J, N, W	347

COMPARATORS

DESCRIPTION	TYPICAL COMPARE TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
4-BIT MAGNITUDE COMPARATORS	11.5 ns	365 mW	SN54S85	SN74S85	J, N, W	202
	21 ns	275 mW	SN5485	SN7485	J, N, W	
	82 ns	20 mW	SN54L85	SN74L85	J, N	

PARITY GENERATORS/CHECKERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	13 ns	335 mW	SN54S280	SN74S280	J, N, W	491
8-BIT ODD/EVEN PARITY GENERATORS/CHECKERS	35 ns	170 mW	SN54180	SN74180	J, N, W	379

OTHER ARITHMETIC OPERATORS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH TOTEM-POLE OUTPUTS	7 ns	250 mW	SN54S86	SN74S86	J, N, W	209
	10 ns	30 mW	SN54LS86	SN74LS86	J, N, W	
	14 ns	150 mW	SN5486	SN7486	J, N, W	
	55 ns	15 mW	SN54L86	SN74L86	J, N, T	
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS	18 ns	30 mW	SN54LS136	SN74LS136	J, N, W	271
	27 ns	150 mW	SN54136	SN74136	J, N, W	
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES	18 ns	40 mW	SN54LS266	SN74LS266	J, N, W	486
QUADRUPLE EXCLUSIVE OR/NOR GATES	8 ns	325 mW	SN54S135	SN74S135	J, N, W	269
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT	14 ns	270 mW	SN54H87	SN74H87	J, N, W	214

†SN54S181, SN5497 not available in the N package.

SHIFT REGISTERS

DESCRIPTION	NO OF BITS	SHIFT FREQ	SERIAL DATA INPUT	ASYNC CLEAR	MODES S-R‡	MODES S-L‡	MODES LOAD	MODES HOLD	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
PARALLEL-IN, PARALLEL-OUT (BIDIRECTIONAL)	8	25 MHz	D	Low	X	X	X	X	360 mW		SN74198	J, N, W	456
	4	70 MHz	D	Low	X	X	X	X	450 mW	SN54S194	SN74S194	J, N, W	437
		25 MHz	D	Low	X	X	X	X	195 mW	SN54194	SN74194	J, N, W	437
		20 MHz	D	Low	X	X	X	X	60 mW	SN54LS194	SN74LS194	J, N, W	437
PARALLEL-IN, PARALLEL-OUT	8	25 MHz	J-$\overline{K}$	Low	X		X	X	360 mW	SN54199	SN74199	J, N, W	456
	5	10 MHz	D	Low	X		X		240 mW	SN5496	SN7496	J, N, W	243
		5 MHz	D	Low	X		X		120 mW	SN54L96	SN74L96	J, N	243
	4	70 MHz	J-$\overline{K}$	Low	X		X		375 mW	SN54S195	SN74S195	J, N, W	444
		30 MHz	J-$\overline{K}$	Low	X		X		195 mW	SN54195	SN74195	J, N, W	444
		25 MHz	D	None	X		X		195 mW	SN5495A	SN7495A	J, N, W	237
		25 MHz	D	Low	X		X	X	230 mW	SN54179	SN74179	J, N, W	375
		25 MHz	D	None	X		X	X	230 mW	SN54178	SN74178	J, N, W	375
		20 MHz	J-$\overline{K}$	Low	X		X		50 mW	SN54LS195	SN74LS195	J, N, W	444
		20 MHz	D	None	X		X		50 mW	SN54LS95A	SN74LS95A	J, N, W	237
		20 MHz	D	None	X		X		62 mW	SN54LS295	SN74LS295	J, N, W	502
		3 MHz	J-$\overline{K}$	None	X		X		19 mW	SN54L99	SN74L99	J, N	255
		3 MHz	D	None	X		X		19 mW	SN54L95	SN74L95	J, N, T	237
SERIAL-IN, PARALLEL-OUT	8	25 MHz	Gated D	Low	X				167 mW	SN54164	SN74164	J, N, W	334
		12 MHz	Gated D	Low	X				84 mW	SN54L164	SN74L164	J, N, T	334
PARALLEL-IN, SERIAL-OUT	8	25 MHz	D	None	X		X	X	210 mW	SN54165	SN74165	J, N, W	339
		20 MHz	D	Low	X		X	X	360 mW	SN54166	SN74166	J, N, W	343
	4	10 MHz	D	High	X		X		175 mW	SN5494	SN7494	J, N, W	234
SERIAL-IN, SERIAL-OUT	8	10 MHz	Gated D	None	X				175 mW	SN5491A	SN7491A	J, N, W	230
		3 MHz	Gated D	None	X				17.5 mW	SN54L91	SN74L91	J, N, T	230

‡S-R ≡ shift right, S-L ≡ shift left

REGISTER FILES

DESCRIPTION	TYPICAL ADDRESS TIME	TYP READ ENABLE TIME	DATA INPUT RATE	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
EIGHT WORDS OF TWO BITS	33 ns	15 ns	20 MHz	560 mW		SN74172	J, N	356
FOUR WORDS OF FOUR BITS	30 ns	15 ns	20 MHz	635 mW	SN54170	SN74170	J, N†, W	351

OTHER REGISTERS

DESCRIPTION	FREQ	ASYNC CLEAR	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
HEX D-TYPE REGISTERS	75 MHz	Low	450 mW	SN54S174	SN74S174	J, N†, W	363
	30 MHz	Low	65 mW	SN54LS174	SN74LS174	J, N, W	363
	25 MHz	Low	225 mW	SN54174	SN74174	J, N, W	363
QUADRUPLE D-TYPE REGISTERS	75 MHz	Low	300 mW	SN54S175	SN74S175	J, N, W	363
	30 MHz	Low	45 mW	SN54LS175	SN74LS175	J, N, W	363
	25 MHz	Low	150 mW	SN54175	SN74175	J, N, W	363
QUADRUPLE MULTIPLEXERS WITH STORAGE	25 MHz	None	195 mW	SN54298	SN74298	J, N, W	505
	3 MHz	None	25 mW	SN54L98	SN74L98	J, N	253
QUADRUPLE BUS-BUFFER REGISTERS	25 MHz	High	250 mW	SN54173	SN74173	J, N, W	360

PULSE SYNCHRONIZERS

DESCRIPTION	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE –55°C to 125°C	TEMPERATURE RANGE 0°C to 70°C	PACKAGES	PAGE NO.
DUAL 30-MHz PULSE SYNCHRONIZERS/DRIVERS	16 ns	255 mW	SN54120	SN74120	J, N, W	264

†SN54170, SN54S174 not available in the N package.

LATCHES

DESCRIPTION	NO. OF BITS	CLEAR	OUTPUTS	TYPICAL DELAY TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
						−55°C to 125°C	0°C to 70°C		
D_G (CLOCKED) LATCHES	8	Low	Q	11 ns	250 mW	SN54116	SN74116	J, N, W	261
		None	Q	15 ns	320 mW	SN54100	SN74100	J, N, W	259
	4	None	Q, $\overline{Q}$	15 ns	160 mW	SN5475	SN7475	J, N, W	182
		None	Q	15 ns	160 mW	SN5477	SN7477	W	182
		None	Q, $\overline{Q}$	30 ns	80 mW	SN54L75	SN74L75	J, N	182
		None	Q	30 ns	80 mW	SN54L77	SN74L77	T	182
$\overline{S}$-$\overline{R}$ Latches (SSI)	4	None	Q	12 ns	90 mW	SN54279	SN74279	J, N, W	85

READ-ONLY MEMORIES (ROM's, PROM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPICAL ADDRESS TIME	TYPICAL ENABLE TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE		PACKAGES	PAGE NO.
						−55°C to 125°C	0°C to 70°C		
1024-BIT ROM	256 X 4	O-C	40 ns	20 ns	0.46 mW	SN54187	SN74187	J, N†, W	410
512-BIT PROM	64 X 8	O-C	50 ns	47 ns	0.6 mW	SN54186	SN74186	J, N, W	404
256-BIT PROM	32 X 8	O-C	29 ns	28 ns	1.3 mW		SN74188A	J, N	414
256-BIT ROM	32 X 8	O-C	26 ns	22 ns	1.1 mW	SN5488A	SN7488A	J, N, W	216

READ/WRITE MEMORIES (RAM's)

DESCRIPTION	ORGANIZATION	TYPE OF OUTPUT	TYPICAL ADDRESS TIME	TYPICAL ENABLE TIME	TYP POWER DISSIPATION PER BIT	TEMPERATURE RANGE		PACKAGES	PAGE NO.
						−55°C to 125°C	0°C to 70°C		
256-BIT READ/WRITE MEMORY	256 X 1	3-State	30 ns	9 ns	1.7 mW	SN54S200	SN74S200	J, N, W	466
	256 X 1	3-State	42 ns	17 ns	1.8 mW		SN74200	J, N	463
	256 X 1	O-C	32 ns	17 ns	1.7 mW	SN54S206	SN74S206	J, N, W	470
64-BIT READ/WIRTE MEMORY	16 X 4	O-C	32 ns	30 ns	5.9 mW		SN7489	J, N, W	220
16-BIT READ/WRITE MEMORY	16 X 1	O-C	15 ns	15 ns	14 mW	SN5481A	SN7481A	J, N, W	190
	16 X 1	O-C	15 ns	15 ns	14 mW	SN5484A	SN7484A	J, N, W	190
16-BIT MULTIPLE-PORT REGISTER FILE	8 X 2	3-State	33 ns	15 ns	35 mW		SN74172	J, N	356
16-BIT REGISTER FILE	4 X 4	O-C	30 ns	15 ns	40 mW	SN54170	SN74170	J, N†, W	351

CODE CONVERTERS

DESCRIPTION	TYPICAL DELAY TIME PER PACKAGE LEVEL	TYPICAL TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
			−55°C to 125°C	0°C to 70°C		
6-LINE-BCD TO 6-LINE BINARY, OR 4-LINE TO 4-LINE BCD 9's/BCD 10's CONVERTERS	25 ns	280 mW	SN54184	SN74184	J, N, W	398
6-BIT-BINARY TO 6-BIT-BCD CONVERTERS	25 ns	280 mW	SN54185A	SN74185A	J, N, W	398

†SN54187, SN54170 not available in the N package.

DATA SELECTORS/MULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL DELAY TIMES			TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
		DATA TO INV OUTPUT	DATA TO NON-INV OUTPUT	FROM ENABLE		−55°C to 125°C	0°C to 70°C		
16-LINE-TO-1-LINE	2-state	11 ns		18 ns	200 mW	SN54150	SN74150	J, N, W	294
8-LINE-TO-1-LINE	3-state	4.5 ns	8 ns	14 ns	275 mW	SN54S251	SN74S251	J, N, W	473
	3-state	17 ns	21 ns	21 ns	250 mW	SN54251	SN74251	J, N, W	473
	3-state	17 ns	21 ns	21 ns	35 mW	SN54LS251	SN74LS251	J, N, W	473
	2-state	4.5 ns	8 ns	9 ns	225 mW	SN54S151	SN74S151	J, N, W	294
	2-state	8 ns	16 ns	22 ns	145 mW	SN54151A	SN74151A	J, N, W	294
	2-state	8 ns			130 mW	SN54152A	SN74152A	W	294
	2-state	11 ns	18 ns	27 ns	30 mW	SN54LS151	SN74LS151	J, N, W	294
	2-state	11 ns		18 ns	28 mW	SN54LS152	SN74LS152	W	294
DUAL 4-LINE-TO-1-LINE	3-state		12 ns	16 ns	35 mW	SN54LS253	SN74LS253	J, N, W	480
	2-state		6 ns	9.5 ns	225 mW	SN54S153	SN74S153	J, N, W	302
	2-state		14 ns	17 ns	180 mW	SN54153	SN74153	J, N, W	302
	2-state		14 ns	17 ns	31 mW	SN54LS153	SN74LS153	J, N, W	302
	2-state		27 ns	34 ns	90 mW	SN54L153	SN74L153	J, N	302
QUADRUPLE 2-LINE-TO-1-LINE WITH STORAGE	2-state		20 ns from clock		195 mW	SN54298	SN74298	J, N, W	505
QUADRUPLE 2-LINE-TO-1-LINE	3-state	4 ns		14 ns	280 mW	SN54S258	SN74S258	J, N, W	483
	3-state		5 ns	14 ns	320 mW	SN54S257	SN74S257	J, N, W	483
	2-state	4 ns		7 ns	195 mW	SN54S158	SN74S158	J, N, W	317
	2-state		5 ns	8 ns	250 mW	SN54S157	SN74S157	J, N, W	317
	2-state		9 ns	14 ns	150 mW	SN54157	SN74157	J, N, W	317
	2-state		18 ns	27 ns	75 mW	SN54L157	SN74L157	J, N	317

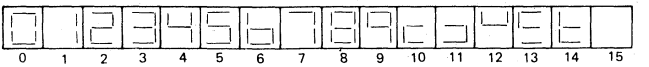
DECODERS/DEMULTIPLEXERS

DESCRIPTION	TYPE OF OUTPUT	TYPICAL SELECT TIME	TYPICAL ENABLE TIME	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
4-LINE-TO-16-LINE	Totem-Pole	23 ns	19 ns	170 mW	SN54154	SN74154	J, N, W	308
	Totem-Pole	46 ns	38 ns	85 mW	SN54L154	SN74L154	J, N	308
	Open-Collector	24 ns	19 ns	170 mW	SN54159	SN74159	J, N, W	323
4-LINE-TO-10-LINE, BCD-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5442A	SN7442A	J, N, W	167
	Totem-Pole	34 ns		70 mW	SN54L42	SN74L42	J, N	167
4-LINE-TO-10-LINE, EXCESS-3-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5443A	SN7443A	J, N, W	167
	Totem-Pole	34 ns		70 mW	SN54L43	SN74L43	J, N	167
4-LINE-TO-10-LINE EXCESS-3-GRAY-TO-DECIMAL	Totem-Pole	17 ns		140 mW	SN5444A	SN7444A	J, N, W	167
	Totem-Pole	34 ns		70 mW	SN54L44	SN74L44	J, N	167
3-LINE-TO-8-LINE	Totem-Pole	8 ns	7 ns	225 mW	SN54S138	SN74S138	J, N, W	274
	Totem-Pole	22 ns	21 ns	31 mW	SN54LS138	SN74LS138	J, N, W	274
DUAL 2-LINE-TO-4-LINE	Totem-Pole	7.5 ns	6 ns	300 mW	SN54S139	SN74S139	J, N, W	274
	Totem-Pole	22 ns	19 ns	34 mW	SN54LS139	SN74LS139	J, N, W	274
	Totem-Pole	18 ns	15 ns	30 mW	SN54LS155	SN74LS155	J, N, W	312
	Totem-Pole	21 ns	16 ns	250 mW	SN54155	SN74155	J, N, W	312
	Open-Collector	23 ns	18 ns	250 mW	SN54156	SN74156	J, N, W	312

OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					–55°C to 125°C	0°C to 70°C		
BCD-TO-DECIMAL DECODERS/DRIVERS	80 mA	30 V	215 mW	Invalid Codes	SN5445	SN7445	J, N, W	171
	80 mA	15 V	215 mW	Invalid Codes	SN54145	SN74145	J, N, W	288
	7 mA	60 V	80 mW	Invalid Codes		SN74141	J, N, W	278
BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS	40 mA	30 V	320 mW	Ripple	SN5446A	SN7446A	J, N, W	173
	40 mA	15 V	320 mW	Ripple	SN5447A	SN7447A	J, N, W	173
	20 mA	30 V	133 mW	Ripple	SN54L46	SN74L46	J, N	173
	20 mA	15 V	133 mW	Ripple	SN54L47	SN74L47	J, N	173
	10 mA	5.5 V	265 mW	Ripple	SN5448	SN7448	J, N, W	173
	6.4 mA	5.5 V	165 mW	Direct	SN5449	SN7449	W	173

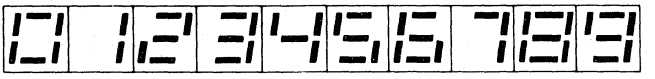
RESULTANT DISPLAYS USING '46A, '47A, '48, '49, 'L46, 'L47



OPEN-COLLECTOR DISPLAY DECODERS/DRIVERS WITH COUNTER/LATCH

DESCRIPTION	OUTPUT SINK CURRENT	OFF-STATE OUTPUT VOLTAGE	TYP TOTAL POWER DISSIPATION	BLANKING	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					–55°C to 125°C	0°C to 70°C		
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-DECIMAL DECODER/DRIVER	7 mA	55 V	340 mW			SN74142	J, N	280
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN SEGMENT DECODER/ LED DRIVER	Constant Current 15 mA	7 V	280 mW	Ripple	SN54143	SN74143	J, N, W	283
BCD COUNTER/ 4-BIT LATCH/ BCD-TO-SEVEN-SEGMENT DECODER/ LAMP DRIVER	20 mA	15 V	280 mW	Ripple	SN54144		J, N, W	283
	25 mA	15 V	280 mW	Ripple		SN74144	J, N, W	283

RESULTANT DISPLAYS USING '143, '144



ASYNCHRONOUS COUNTERS (RIPPLE CLOCK)—NEGATIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ	PARALLEL LOAD	CLEAR	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
DECADE	50 MHz	Yes	Low	240 mW	SN54196	SN74196	J, N, W	451
	35 MHz	Yes	Low	150 mW	SN54176	SN74176	J, N, W	369
	32 MHz	Set-to-9	High	160 mW	SN5490A	SN7490A	J, N, W	224
	32 MHz	Set-to-9	High	160 mW	SN54290	SN74290	J, N, W	499
	30 MHz	Yes	Low	60 mW	SN54LS196	SN74LS196	J, N, W	451
	3 MHz	Set-to-9	High	20 mW	SN54L90	SN74L90	J, N, T	224
4-BIT BINARY	50 MHz	Yes	Low	240 mW	SN54197	SN74197	J, N, W	451
	35 MHz	Yes	Low	150 mW	SN54177	SN74177	J, N, W	369
	32 MHz	None	High	160 mW	SN5493A	SN7493A	J, N, W	224
	32 MHz	None	High	160 mW	SN54293	SN74293	J, N, W	499
	30 MHz	Yes	Low	60 mW	SN54LS197	SN74LS197	J, N, W	451
	3 MHz	None	High	20 mW	SN54L93	SN74L93	J, N, T	224
DIVIDE-BY-12	32 MHz	None	High	160 mW	SN5492A	SN7492A	J, N, W	224

SYNCHRONOUS COUNTERS—POSITIVE-EDGE TRIGGERED

DESCRIPTION	COUNT FREQ	PARALLEL LOAD	CLEAR	TYP TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
					−55°C to 125°C	0°C to 70°C		
DECADE	25 MHz	Sync	Sync-L	305 mW	SN54162	SN74162	J, N, W	325
	25 MHz	Sync	Async-L	305 mW	SN54160	SN74160	J, N, W	325
DECADE UP/DOWN	25 MHz	Async	Async-H	85 mW	SN54LS192	SN74LS192	J, N, W	427
	25 MHz	Async	Async-H	325 mW	SN54192	SN74192	J, N, W	427
	20 MHz	Async	None	90 mW	SN54LS190	SN74LS190	J, N, W	417
	20 MHz	Async	None	325 mW	SN54190	SN74190	J, N, W	417
	3 MHz	Async	Async-H	42 mW	SN54L192	SN74L192	J, N	427
DECADE RATE MULTIPLIER, $\frac{1}{N_{10}}$	25 MHz	Set-to-9	Async-H	270 mW	SN54167	SN74167	J, N, W	347
4-BIT BINARY	25 MHz	Sync	Sync-L	305 mW	SN54163	SN74163	J, N, W	325
	25 MHz	Sync	Async-L	305 mW	SN54161	SN74161	J, N, W	325
4-BIT BINARY	25 MHz	Async	Async-H	85 mW	SN54LS193	SN74LS193	J, N, W	427
	25 MHz	Async	Async-H	325 mW	SN54193	SN74193	J, N, W	427
	20 MHz	Async	None	90 mW	SN54LS191	SN74LS191	J, N, W	417
	20 MHz	Async	None	325 mW	SN54191	SN74191	J, N, W	417
	3 MHz	Async	Async-H	42 mW	SN54L193	SN74L193	J, N	427
6-BIT BINARY RATE MULTIPLIER, $\frac{1}{N_2}$	25 MHz		Async-H	345 mW	SN5497	SN7497	J, N†, W	248

†SN5497 not available in N package

PRIORITY ENCODERS/REGISTERS

DESCRIPTION	TYPICAL PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION	TEMPERATURE RANGE		PACKAGES	PAGE NO.
			−55°C to 125°C	0°C to 70°C		
FULL BCD PRIORITY ENCODERS	10 ns	225 mW	SN54147	SN74147	J, N, W	290
CASCADABLE OCTAL PRIORITY ENCODERS	10 ns	190 mW	SN54148	SN74148	J, N, W	290
4-BIT CASCADABLE PRIORITY REGISTERS	35 ns	275 mW	SN54278	SN74278	J, N, W	488

TYPES SN5442A THRU SN5444A, SN54L42 THRU SN54L44, SN7442A THRU SN7444A, SN74L42 THRU SN74L44 4-LINE-TO-10-LINE DECODERS (1-OF-10)

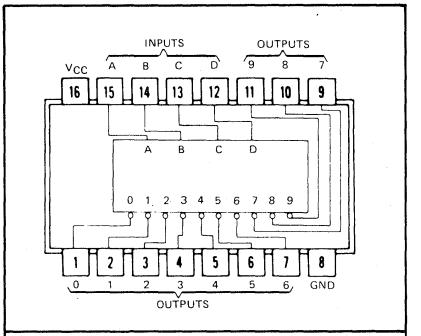
BULLETIN NO. DL-S 7211861, DECEMBER 1972

'42A, 'L42 . . . BCD-TO-DECIMAL
'43A, 'L43 . . . EXCESS-3-TO-DECIMAL
'44A, 'L44 . . . EXCESS-3-GRAY-TO-DECIMAL

- Also for Application as
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A, '43A, '44A	140 mW	17 ns
'L42, 'L43, 'L44	70 mW	49 ns

SN54'/SN74' . . . J, N, OR W PACKAGE
SN54L'/SN74L' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'L42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt.

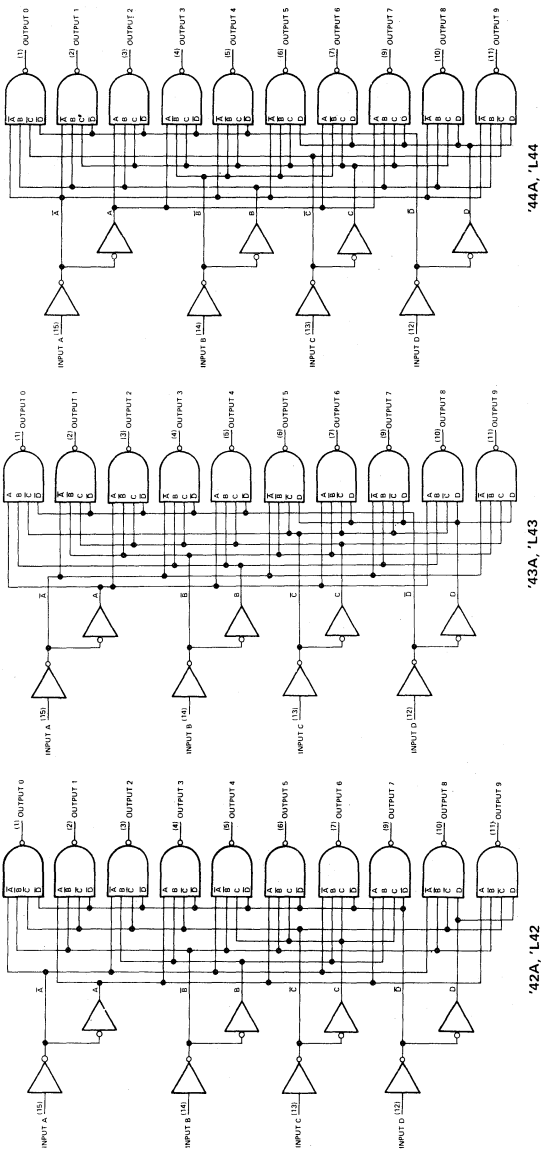
The 'L42, 'L43, 'L44 decoders are designed specifically for power-critical or battery-operated systems. The '42A, '43A, and '44A decoders are intended for higher-performance systems, especially new designs, where power is not critical. For ultra-high performance and/or speed-critical memory decoders, the SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

FUNCTION TABLE

NO.	'42A, 'L42 BCD INPUT				'43A, 'L43 EXCESS-3-INPUT				'44A, 'L44 EXCESS-3-GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
	D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	L	H	H	L	L	H	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	L	H	L	L	L	H	H	L	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	L	H	H	L	L	H	L	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	L	H	H	H	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	L	L	L	H	H	L	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	L	L	H	H	H	L	H	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	L	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	L	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	L	L	H	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

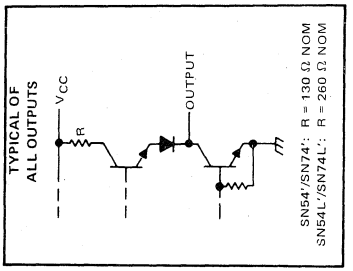
functional block diagrams and schematics of inputs and outputs

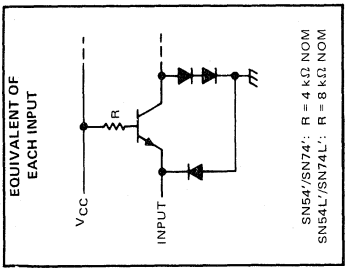


'42A, 'L42
BCD-TO-DECIMAL DECODERS

'43A, 'L43
EXCESS-3-TO-DECIMAL DECODERS

'44A, 'L44
EXCESS-3-GRAY-TO-DECIMAL DECODERS





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5442A, SN5443A, SN5444A			SN7442A, SN7443A, SN7444A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5442A, SN5443A, SN5444A			SN7442A, SN7443A, SN7444A			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		28	41		28	56	mA

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 3: Load circuits and waveforms are shown on page 148.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54L' Circuits . . . . . −55°C to 125°C
SN74L' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54L42 SN54L43 SN54L44			SN74L42 SN74L43 SN74L44			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 8 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−9		−28	mA
I_{CC}	Supply Current	V_{CC} = MAX, See Note 2		SN54L'		14	22	mA
				SN74L'		14	28	

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	C_L = 15 pF, R_L = 800 Ω, See Note 3	10	44	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			46	70	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic		10	34	50	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			52	70	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN5445, SN7445
BCD-TO-DECIMAL DECODERS/DRIVERS

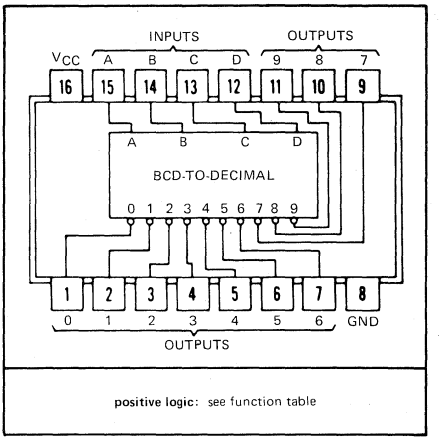
BULLETIN NO. DL-S 7211816, DECEMBER 1972

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



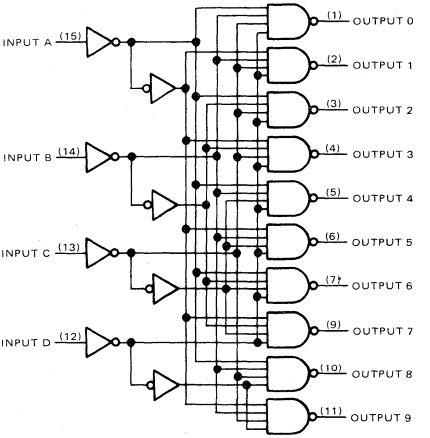
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS								
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monolithic BCD-to-decimal decoders/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (30 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Maximum current into any output (off-state) . . . . . 1 mA
Operating free-air temperature range: SN5445 Circuits . . . . . −55°C to 125°C
SN7445 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5445			SN7445			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			30			30	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	$I_{O(on)}$ = 80 mA		0.5	0.9	V
			$I_{O(on)}$ = 20 mA			0.4	
$V_{O(off)}$	Off-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(off)}$ = 250 μA		30			V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN5445		43	62	mA
			SN7445		43	70	

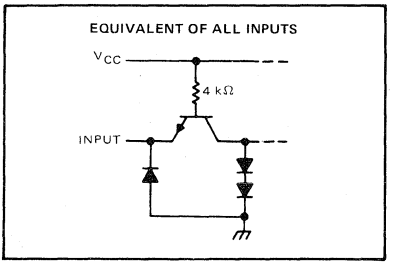
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

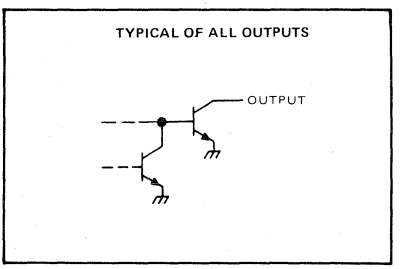
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Note 3			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

NOTE 3: Load circuit and waveforms are shown on page 148.

schematics of inputs and outputs





'46A, '47A, 'L46, 'L47 feature

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'48 features

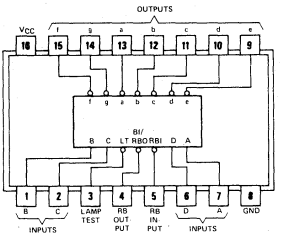
- Internal Pull-Ups Eliminate Need for External Resistors
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

'49 features

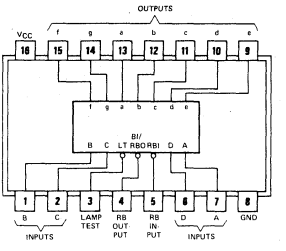
- Open-Collector Outputs
- Blanking Input

- All Circuit Types Feature Lamp Intensity Modulation Capability

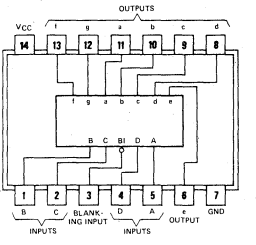
'46A, '47A . . . J, N, OR W PACKAGE
'L46, 'L47 . . . J OR N PACKAGE
(TOP VIEW)



'48 . . . J, N, OR W PACKAGE
(TOP VIEW)



'49 . . . W PACKAGE
(TOP VIEW)



positive logic: see function tables

description

Of these BCD-to-seven-segment decoder/driver circuits, the '46A, 'L46, '47A, and 'L47 feature active-low outputs designed for driving indicators directly, and the other two, '48 and '49, feature active-high outputs for driving lamp buffers. The following table summarizes the differences in the driver outputs and gives the typical power dissipation.

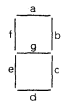
TYPE	DRIVER OUTPUTS				TYPICAL POWER DISSIPATION
	ACTIVE-LEVEL	OUTPUT CONFIGURATION	I_{OL}, SINK CURRENT	MAX VOLTAGE	
'46A	low	open-collector	40 mA	30 V	320 mW
'L46	low	open-collector	20 mA	30 V	160 mW
'47A	low	open-collector	40 mA	15 V	320 mW
'L47	low	open-collector	20 mA	15 V	160 mW
'48A	high	2-kΩ pull-up	6.4 mA	5.5 V	265 mW
'49A	high	open-collector	10 mA	5.5 V	165 mW

All of the circuits except '49 have full ripple-blanking input/output controls and a lamp test input. The '49 circuit incorporates a direct blanking input. Segment identification with resultant displays are shown on the following page. Display patterns for BCD input counts above 9 are unique symbols to authenticate input conditions.

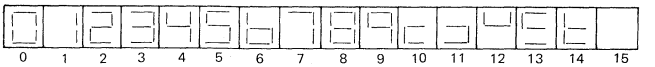
description (continued)

The '46A, '47A, '48, 'L46, and 'L47 circuits incorporate automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) of these types may be performed at any time when the BI/RBO node is at a high level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity by pulsing or to inhibit the outputs. Inputs and outputs are entirely compatible for use with TTL or DTL logic outputs.

Series 54 and Series 54L devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and Series 74L devices are characterized for operation from 0°C to 70°C.



SEGMENT IDENTIFICATION



NUMERICAL DESIGNATIONS AND RESULTANT DISPLAYS

'46A, '47A, 'L46, 'L47
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF	1
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF	1
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON	
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON	
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON	
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON	
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON	
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF	
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON	
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON	
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON	
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON	
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON	
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON	
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON	
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	2
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF	3
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are off regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go off and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are on.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'48
FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high, if blanking of a decimal zero is not desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.
3. When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).
4. When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are high.

†BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

'49
FUNCTION TABLE

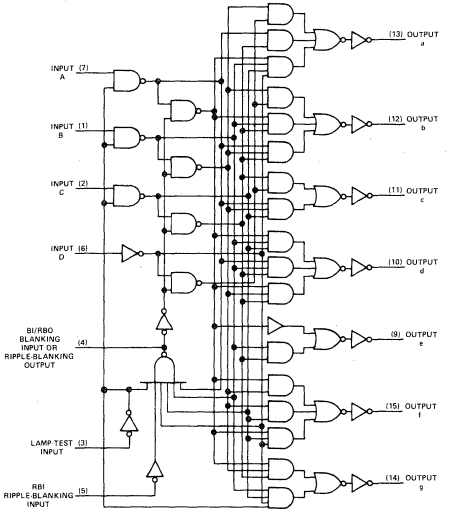
DECIMAL OR FUNCTION	INPUTS					OUTPUTS							NOTE
	D	C	B	A	BI	a	b	c	d	e	f	g	
0	L	L	L	L	H	H	H	H	H	H	H	L	1
1	L	L	L	H	H	L	H	H	L	L	L	L	
2	L	L	H	L	H	H	H	L	H	H	L	H	
3	L	L	H	H	H	H	H	H	H	L	L	H	
4	L	H	L	L	H	L	H	H	L	L	H	H	
5	L	H	L	H	H	H	L	H	H	L	H	H	
6	L	H	H	L	H	L	L	H	H	H	H	H	
7	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	L	L	L	L	L	L	L	L	2

H = high level, L = low level, X = irrelevant

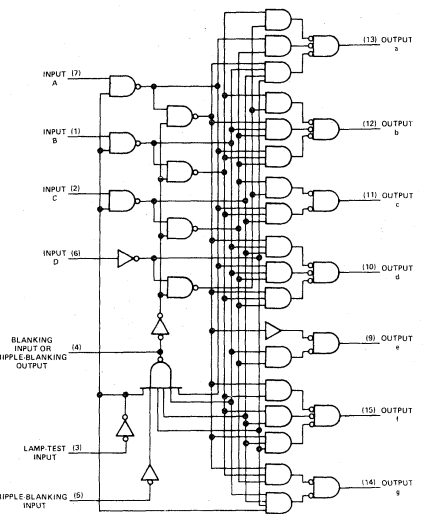
NOTES: 1. The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired.
2. When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

functional block diagrams

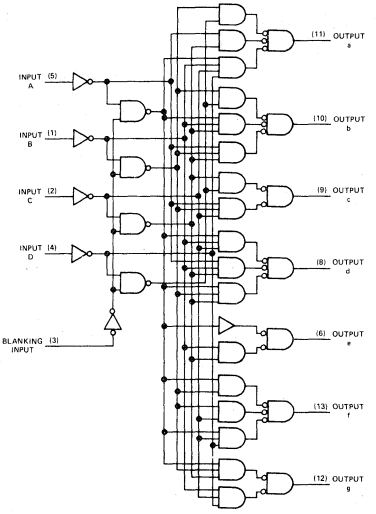
'46A, '47A, 'L46, 'L47



'48

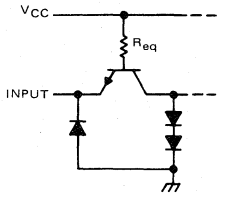


'49



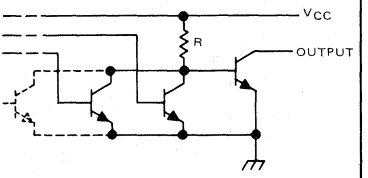
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT
EXCEPT BI/RBO



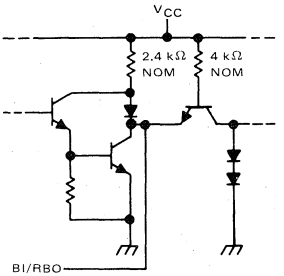
SN54'/SN74': R_{eq} = 4 kΩ NOM
SN54L'/SN74L': R_{eq} = 8 kΩ NOM

'46A, '47A, 'L46, 'L47
TYPICAL OF OUTPUTS
a THRU g

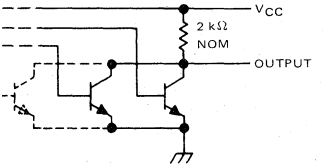


'46A, '47A: R = 2 kΩ NOM
'L46, 'L47: R = 4 kΩ NOM

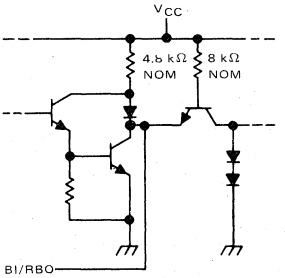
'46A, '47A, '48
EQUIVALENT OF BI/RBO



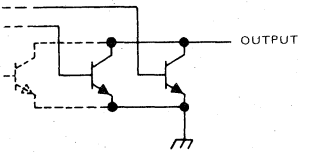
'48
TYPICAL OF OUTPUTS
a THRU g



'L46, 'L47
EQUIVALENT OF BI/RBO



'49
TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN5446A, SN5447A Circuits . . . . . −55°C to 125°C
SN7446A, SN7447A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5446A			SN5447A			SN7446A			SN7447A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			40			40			40			40	mA
High-level output current, I_{OH}	BI/RBO			−200			−200			−200			−200	μA
Low-level output current, I_{OL}	BI/RBO			8			8			8			8	mA
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage, any input except BI/RBO		V_{CC} = MIN, I_I = −10 mA				−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA		2.4	3.7		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.3	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = MAX				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(on)}$ = 40 mA			0.3	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		BI/RBO					−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX				−4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	SN54'		64	85	mA
				SN74'		64	103	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 120 Ω, See Note 3			100	ns
t_{on}	Turn-on time from A input				100	
t_{off}	Turn-off time from RBI input				100	ns
t_{on}	Turn-on time from RBI input				100	

NOTE 3: Load circuit and voltage waveforms are shown on page 148. t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Peak output current ($t_w \leqslant 1$ ms, duty cycle $\leqslant 10\%$) . . . . . 200 mA
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN54L46, SN54L47 Circuits . . . . . −55°C to 125°C
SN74L46, SN74L47 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54L46			SN54L47			SN74L46			SN74L47			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	4.75	5	5.25	4.75	5	5.25	V
Off-state output voltage, $V_{O(off)}$	a thru g			30			15			30			15	V
On-state output current, $I_{O(on)}$	a thru g			20			20			20			20	mA
High-level output current, I_{OH}	BI/RBO			−100			−100			−100			−100	μA
Low-level output current, I_{OL}	BI/RBO			4			4			4			4	mA
Operating free-air temperature, T_A		−55		125	−55		125	0		70	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage, any input except BI/RBO		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −100 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	BI/RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 4 mA			0.2	0.4	V
$I_{O(off)}$	Off-state output current	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $V_{O(off)}$ = MAX				250	μA
$V_{O(on)}$	On-state output voltage	a thru g	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(on)}$ = 20 mA				0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V				−0.8	mA
		BI/RBO					−2	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX				−2	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	SN54L'		32	43	mA
				SN74L'		32	52	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{off}	Turn-off time from A input	C_L = 15 pF, R_L = 280 Ω, See Note 3			200	ns
t_{on}	Turn-on time from A input				200	
t_{off}	Turn-off time from RBI input				200	ns
t_{on}	Turn-on time from RBI input				200	

NOTE 3: Load circuit and voltage waveforms are shown on page 148; t_{off} corresponds to t_{PLH} and t_{on} corresponds to t_{PHL}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5448 Circuits . . . . . −55°C to 125°C
SN7448 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5448			SN7448			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	a thru g			−400			−400	μA
	BI/RBO			−200			−200	
Low-level output current, I_{OL}	a thru g			6.4			6.4	mA
	BI/RBO			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage, any input except BI/RBO		V_{CC} = MIN, I_I = −10 mA				−1.5	V
V_{OH}	High-level output voltage	a thru g	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	4.2		V
		BI/RBO			2.4	3.7		
I_O	Output current	a thru g	V_{CC} = MIN, V_O = 0.85 V, Input conditions as for V_{OH}		−1.3	−2		mA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.27	0.4	V
I_I	Input current at maximum input voltage	Any input except BI/RBO	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	Any input except BI/RBO	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		BI/RBO					−4	
I_{OS}	Short-circuit output current	BI/RBO	V_{CC} = MAX				−4	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	SN5448		53	76	mA
				SN7448		53	90	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, See Note 4, SN5448: R_L = 1 kΩ, SN7448: R_L = 667 Ω			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 148.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current forced into any output in the off state . . . . . 1 mA
Operating free-air temperature range: SN5449 Circuits . . . . . −55°C to 125°C
SN7449 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5449			SN7449			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			10			10	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5449			SN7449			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.6			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −10 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 10 mA		0.27	0.4		0.27	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		33	47		33	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output from A input	C_L = 15 pF, See Note 4, SN5449: R_L = 1 kΩ, SN7449: R_L = 667 Ω			100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from A input				100	
t_{PHL}	Propagation delay time, high-to-low-level output from RBI input				100	ns
t_{PLH}	Propagation delay time, low-to-high-level output from RBI input				100	

NOTE 4: Load circuit and voltage waveforms are shown on page 148.

TYPES SN5475, SN5477, SN54L75, SN54L77, SN7475, SN7477, SN74L75, SN74L77
4-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7211851, DECEMBER 1972

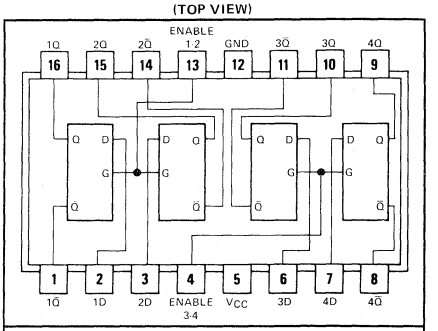
logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

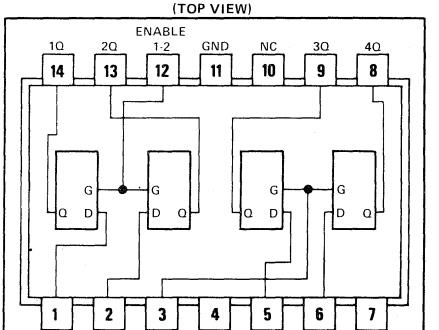
H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

'75 . . . J, N, OR W PACKAGE
'L75 . . . J OR N PACKAGE
(TOP VIEW)



logic: see function table

'77 . . . W PACKAGE
'L77 . . . T PACKAGE
(TOP VIEW)



logic: see function table

NC—No internal connection

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

The '75 and 'L75 feature complementary Q and $\bar{Q}$ outputs from a 4-bit latch, and are available in various 16-pin packages. For higher component density applications, the '77 and 'L77 4-bit latches are available in 14-pin flat packages.

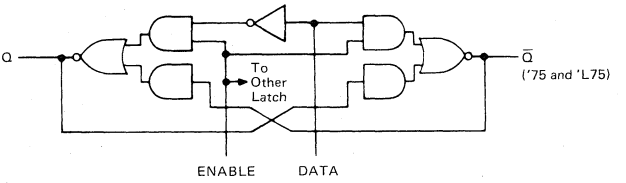
These circuits are completely compatible with all popular TTL or DTL families. All outputs are diode-clamped to minimize transmission-line effects and simplify system design. Series 54 and 54L devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74L devices are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

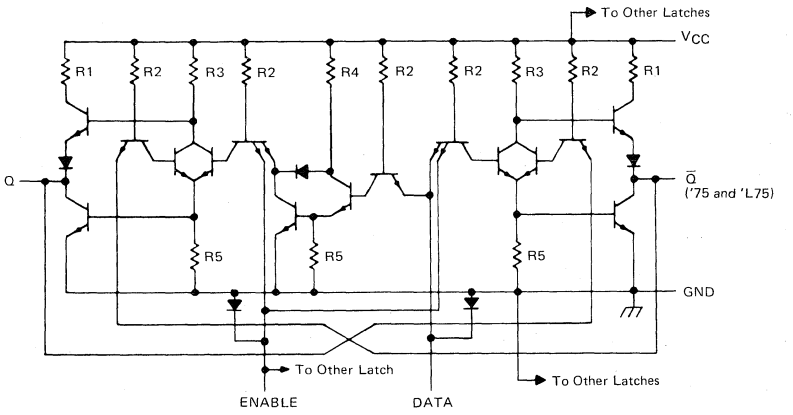
Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54', SN54L' Circuits	−55°C to 125°C
SN74', SN74L' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

functional block diagram (each latch)



schematic (each latch)



NOMINAL RESISTOR VALUES

RESISTOR	'75, '77	'L75, 'L77
R1	130 Ω	260 Ω
R2	4 kΩ	8 kΩ
R3	1.6 kΩ	3.2 kΩ
R4	2.5 kΩ	5 kΩ
R5	1 kΩ	2 kΩ

recommended operating conditions

	SN5475, SN5477			SN7475, SN7477			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{setup}	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		G input					160	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		G input					−6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	mA
				SN74'	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54'		32	46	mA
				SN74'		32	53	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◊	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		16	30	ns
t_{PHL}					14	25	
t_{PLH}¶	D	$\overline{Q}$			24	40	ns
t_{PHL}¶					7	15	
t_{PLH}	G	Q			16	30	ns
t_{PHL}					7	15	
t_{PLH}¶	G	$\overline{Q}$			16	30	ns
t_{PHL}¶					7	15	

◊t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
¶These parameters are not applicable for the SN5477 and SN7477.

recommended operating conditions

	SN54L75, SN54L77			SN74L75, SN74L77			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−200	μA
Low-level output current, I_{OL}			8			8	mA
Width of enabling pulse, t_w	100			100			ns
Setup time, t_{setup}	40			40			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				40	μA
		G input					80	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		G input					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54L'	−10		−29	mA
				SN74L'	−9		−29	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54L'		16	23	mA
				SN74'L		16	27	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

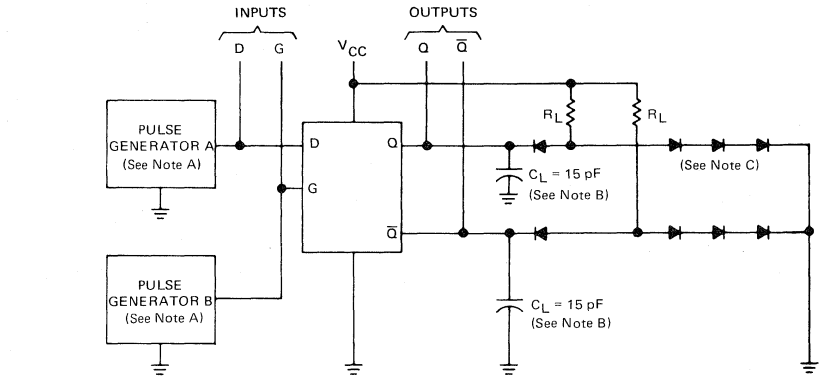
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 800 Ω, See Figure 1		32	60	ns
t_{PHL}					28	50	
t_{PLH}¶	D	$\overline{Q}$			48	80	ns
t_{PHL}¶					14	30	
t_{PLH}	G	Q			32	60	ns
t_{PHL}					14	30	
t_{PLH}¶	G	$\overline{Q}$			32	60	ns
t_{PHL}¶					14	30	

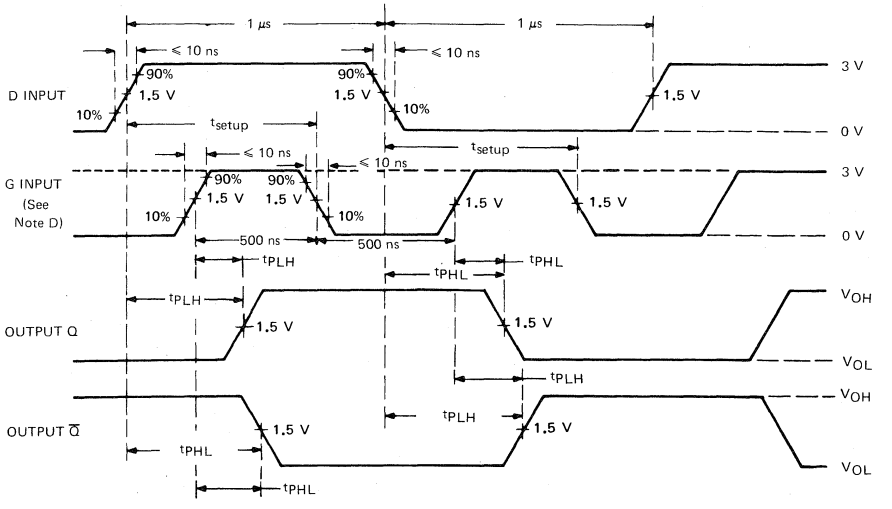
◇t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
¶These parameters are not applicable for the SN54L77 and SN74L77.

PARAMETER MEASUREMENT INFORMATION

switching characteristics†



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, for pulse generator A, PRR ⩽ 500 kHz; for pulse generator B, PRR ⩽ 1 MHz. Positions of D and G input pulses are varied with respect to each other to verify setup times.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. When measuring propagation delay times from the D input, the corresponding G input must be held high.

†Complementary $\overline{Q}$ outputs are on the '75 and 'L75 only.

FIGURE 1

TYPES SN5480, SN7480
GATED FULL ADDERS

BULLETIN NO. DL-S 7211809, DECEMBER 1972

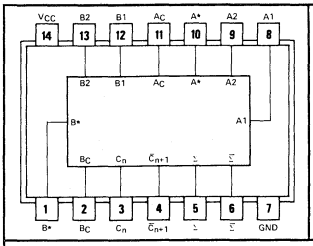
logic

FUNCTION TABLE
(See Notes 1, 2, and 3)

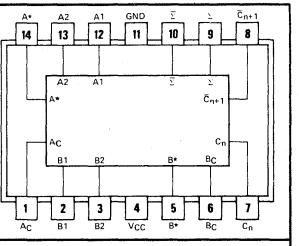
INPUTS			OUTPUTS		
C_n	B	A	$\overline{C}_{n+1}$	$\overline{\Sigma}$	Σ
L	L	L	H	H	L
L	L	H	H	L	H
L	H	L	H	L	H
L	H	H	L	H	L
H	L	L	H	L	H
H	L	H	L	H	L
H	H	L	L	H	L
H	H	H	L	L	H

H = high level, L = low level

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



W
FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NOTES: 1. $A = \overline{A}_C + \overline{A}\star + A1 \cdot A2$, $B = \overline{B}_C + \overline{B}\star + B1 \cdot B2$.
2. When A★ is used as an input, A1 or A2 must be low. When B★ is used as an input, B1 or B2 must be low.
3. When A1 and A2 or B1 and B2 are used as inputs, A★ or B★, respectively, must be open or used to perform dot-AND logic.

3

description

These single-bit, high-speed, binary full adders with gated complementary inputs, complementary sum (Σ and $\overline{\Sigma}$) outputs and inverted carry output are designed for medium- and high-speed, multiple-bit, parallel-add/serial-carry applications. These circuits (see schematic) utilize diode-transistor logic (DTL) for the gated inputs, and high-speed, high-fan-out transistor-transistor logic (TTL) for the sum and carry outputs and are entirely compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN5480 Circuits . . . . . −55°C to 125°C
SN7480 Circuits . . . . . 0° to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 4. Voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN5480			SN7480			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Σ or $\overline{\Sigma}$			−400			−400	μA
	$\overline{C}_{n+1}$			−200			−200	
	A★ or B★			−120			−120	
Low-level output current, I_{OL}	Σ or $\overline{\Sigma}$			16			16	mA
	$\overline{C}_{n+1}$			8			8	
	A★ or B★			4.8			4.8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN5480			SN7480			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{OH}	High-level output voltage	Σ or $\overline{\Sigma}$	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
		$\overline{C}_{n+1}$		I_{OH} = −200 μA							
		A★ or B★		I_{OH} = −120 μA							
V_{OL}	Low-level output voltage	Σ or $\overline{\Sigma}$	V_{CC} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 16 mA		0.22	0.4		0.22	0.4	V
		$\overline{C}_{n+1}$		I_{OL} = 8 mA							
		A★ or B★		I_{OL} = 4.8 mA							
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	A_1, A_2, B_1, B_2, A_C, or B_C	V_{CC} = MAX, V_I = 2.4 V				15			15	μA
		A★ or B★					−1.1			−1.1	
		C_n					200			200	
I_{IL}	Low-level input current	A1, A2, B1, B2, A_C, or B_C	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		A★ or B★					−2.6			−2.6	
		C_n					−8			−8	
I_{OS}	Short-circuit output-current§	Σ or $\overline{\Sigma}$	V_{CC} = MAX		−20		−57	−18		−57	mA
		$\overline{C}_{n+1}$			−20		−70	−18		−70	
		A★ or B★			−0.9		−2.9	−0.9		−2.9	
I_{CC}	Supply current		V_{CC} = MAX, See Note 6			21	31		21	35	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 6: I_{CC} is measured with all inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

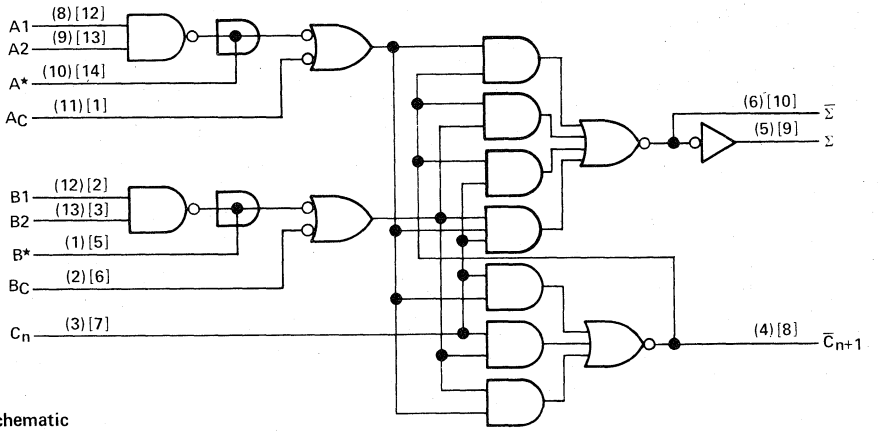
PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	$\overline{C}_{n+1}$	C_L = 15 pF, R_L = 780 Ω, See Note 7		13	17	ns
t_{PHL}					8	12	
t_{PLH}	B_C	$\overline{C}_{n+1}$			18	25	
t_{PHL}					38	55	
t_{PLH}	A_C	Σ	C_L = 15 pF, R_L = 400 Ω, See Note 7		52	70	ns
t_{PHL}					62	80	
t_{PLH}	B_C	$\overline{\Sigma}$			38	55	
t_{PHL}					56	75	
t_{PLH}	A1	A★	C_L = 15 pF, See Note 7		48	65	ns
t_{PHL}					17	25	
t_{PLH}	B1	B★			48	65	
t_{PHL}					17	25	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

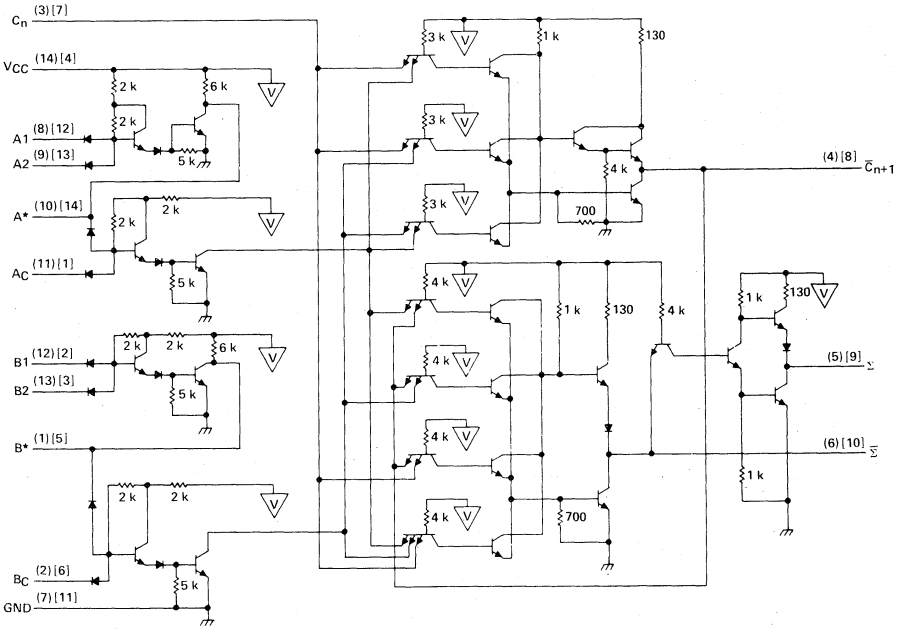
NOTE 7: The load for testing outputs A★ and B★ consists only of capacitance C_L to ground. The load circuit for the other outputs and voltage waveforms are shown on page 148.

functional block diagram

(DUAL-IN-LINE) [FLAT PACKAGE]



schematic



▽ . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

TYPES SN5481A, SN5484A, SN7481A, SN7484A
16-BIT ACTIVE-ELEMENT MEMORIES

BULLETIN NO. DL-S 7211581, DECEMBER 1972

description

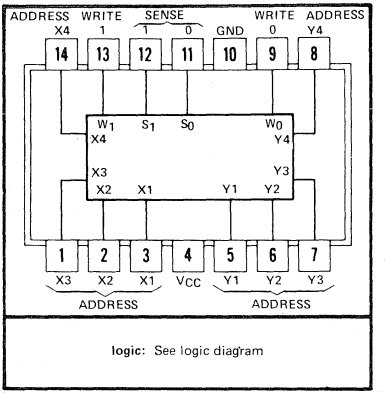
Each of these 16-bit active-element memories is a high-speed, monolithic, transistor-transistor-logic (TTL) array of 16 flip-flops and two write amplifiers interconnected to form a scratch-pad memory with direct-address and nondestructive read-out. These devices are interchangeable with and replace SN5481, SN7481, SN5484, and SN7484, but feature diode-clamped inputs, improved switching speeds, and lower supply current requirements.

The flip-flops are arranged in a four-by-four matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled three-emitter transistors, is used to store one bit. To determine if a logic 1 or logic 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logic 1 sensing outputs are connected to the sense 1 (S_1) amplifier input and all 16 of the logic 0 sensing outputs are connected to the sense 0 (S_0) amplifier input. The two remaining emitters of each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low and currents from all conducting flip-flop transistors flow out of these address lines.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a high level. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a low level and no change will occur in those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense 1 amplifier or the sense 0 amplifier is activated. When this occurs, the output of the activated sense amplifier drops from a high logic level to a low logic level. The memory is nondestructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

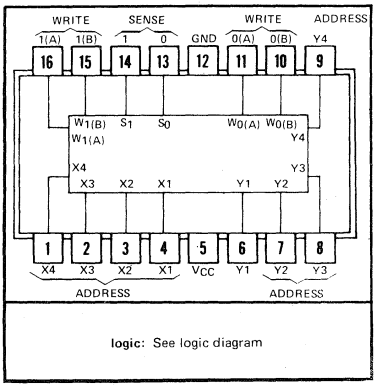
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)

SN5481A/SN7481A CIRCUITS



logic: See logic diagram

SN5484A/SN7484A CIRCUITS



logic: See logic diagram

To store new information in a flip-flop, it is necessary to address it and apply a high-level voltage to the appropriate write amplifier. (The SN5484A and SN7484A have gated write-amplifier inputs). The output of the write amplifier responds by dropping to a low logic level. Since all Sense 0 lines are connected to the output of the write 0 amplifier and all sense 1 lines are connected to the output of the write 1 amplifier, a low level at the output of a write amplifier

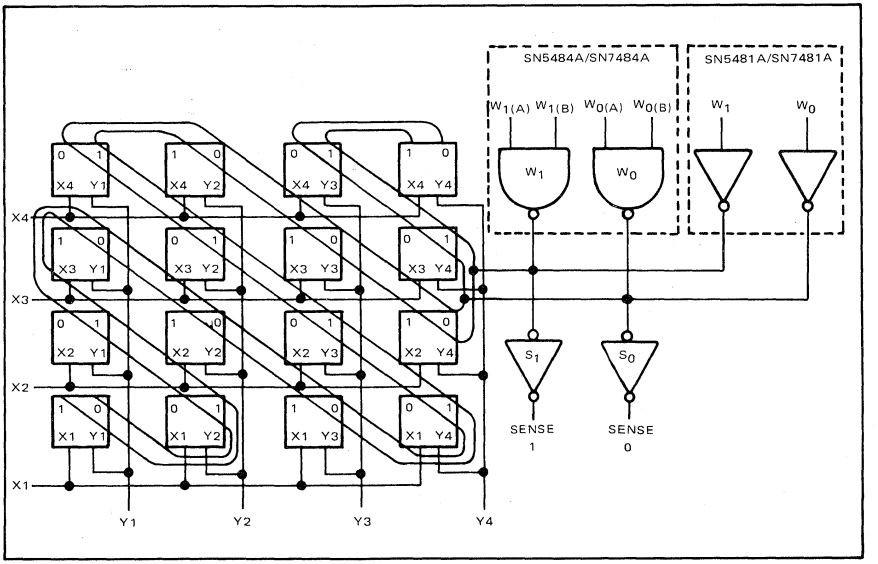
description (continued)

will cause the emitters of all flip-flop transistors connected to that amplifier to go low. In all the flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. Two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. If the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

A number of active-element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). All inputs and outputs are compatible with most DTL and TTL circuits. Average power dissipation is typically 225 milliwatts, and the open-collector outputs may be wire-AND connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 12 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance. The SN5481A and SN5484A circuits are designed for operation over the full military temperature range of −55°C to 125°C; the SN7481A circuits are designed for operation from 0°C to 70°C.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
High-level output voltage . . . . . 5.5 V
Operating free-air temperature range: SN5481A, SN5484A Circuits . . . . . −55°C to 125°C
SN7481A, SN7484A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to any X input in conjunction with any Y input.

recommended operating conditions

	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			40	mA
Width of write pulse, $t_{w(write)}$ (see Figure 1)	20			20			ns
Address input setup time, t_{setup} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level voltage at any input			2			2			V
V_{IL}	Low-level voltage at address inputs	to prevent writing				0.8			0.8	V
		to prevent sensing				1			1	
V_{IL}	Low-level voltage at write inputs					0.8			1	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX			0.4			0.4	V
I_I	Input current at maximum input voltage	Write	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		Address				3			3	
I_{IH}	High-level input current	Write	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Address	V_{CC} = MAX, V_I = 4.5 V			400			400	
I_{IL}	Low-level input current	Write	V_{CC} MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Address				−11			−11	
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 0 V			70			65	mA
			V_{CC} = 5 V, All inputs at 0 V		45	60		45	60	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

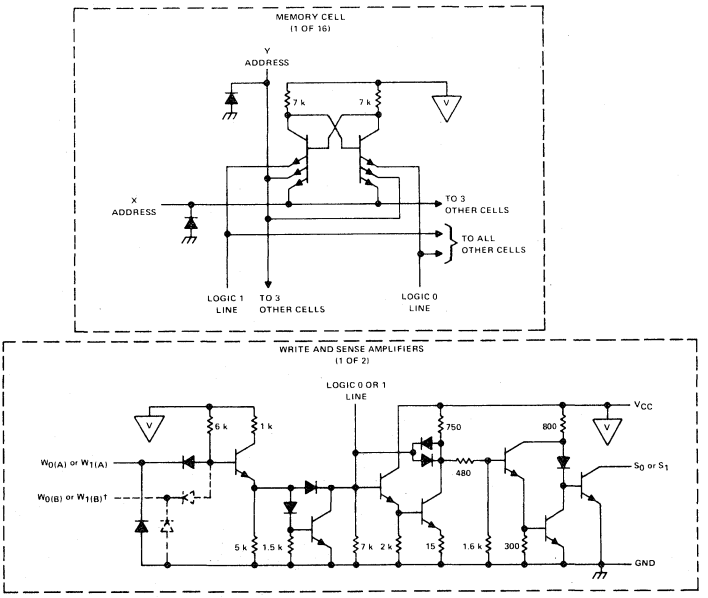
switching characteristics, V_{CC} = 5 V, I_{OL} = MAX†, T_A = 25°C, see figure 1

PARAMETER§	LOCATION ADDRESSED	TEST CONDITIONS	SN5481A, SN5484A			SN7481A, SN7484A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{SR}	X1 – Y1	C_L = 30 pF		13			13		ns
		C_L = 200 pF		18	30		18	30	
t_{PHL}	X1 – Y1	C_L = 30 pF		11	19		12	20	ns
		C_L = 200 pF		17	26		18	27	
t_{PLH}		C_L = 30 pF		13	20		12	19	
		C_L = 200 pF		27	40		18	27	
t_{PHL}	X1 thru X4 and Y1	C_L = 30 pF		10	18		11	19	ns
		C_L = 200 pF		16	25		17	26	
t_{PLH}		C_L = 30 pF		13	20		13	20	
		C_L = 200 pF		27	40		19	28	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

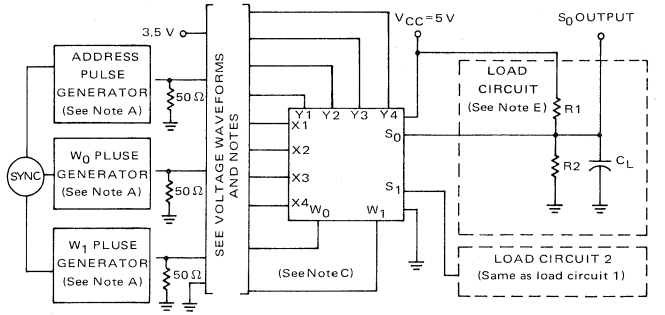
§t_{SR} = Sense recovery time after writing
t_{PHL} = Propagation delay time, high-to-low-level output
t_{PLH} = Propagation delay time, low-to-high-level output

schematic

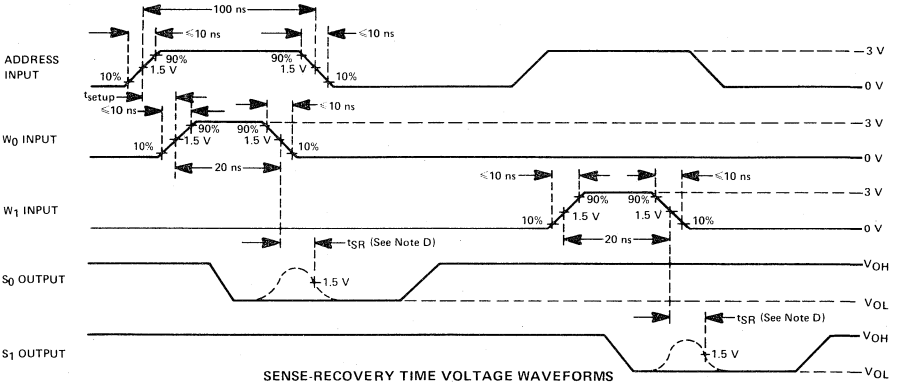


†$W_{0(B)}$ and $W_{1(B)}$ inputs (indicated with dashed lines) are applicable for the SN5484A, SN7484A only.
▽ . . . V_{CC} bus
Resistor values shown are nominal and in ohms.

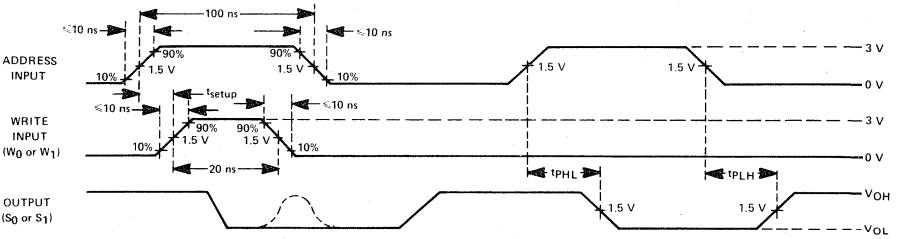
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



SENSE-RECOVERY TIME VOLTAGE WAVEFORMS



PROPAGATION DELAY TIME VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: for the address pulse generator, PRR = 2 MHz; for the W_0 and W_1 pulse generators, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. For the SN5484A and SN7484A, unused W_0 and W_1 inputs are at 3.5 V.
D. t_{SR} = sense-recovery time
E. For the SN5481A and SN5484A: R1 = 240 Ω and R2 = 560 Ω. For the SN7481A and SN7484A: R1 = 120 Ω and R2 = 330 Ω.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPES SN5482, SN7482
2-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7211836, DECEMBER 1972

For applications in:

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

FUNCTION TABLE

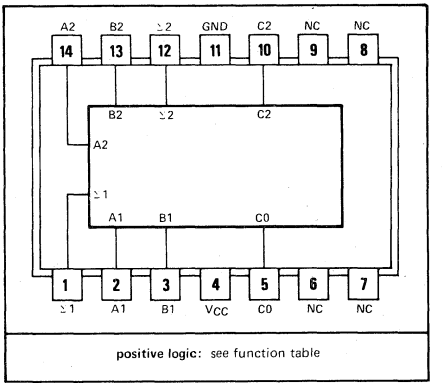
INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

description

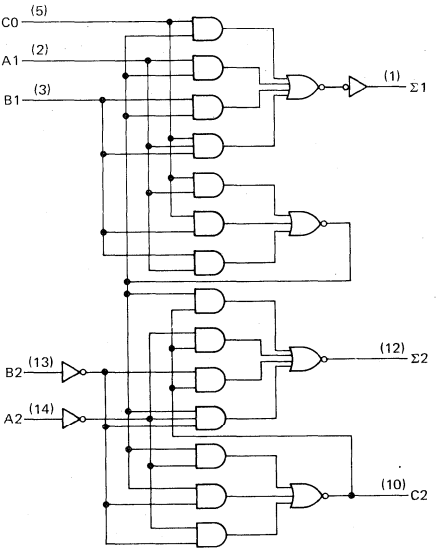
These full adders perform the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, these circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) and are compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



NC—No internal connection

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5482 Circuits . . . . . −55°C to 125°C
SN7482 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN5482			SN7482			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Σ1 or Σ2			−400			−400	μA
	C2			−200			−200	
Low-level output current, I_{OL}	Σ1 or Σ2			16			16	mA
	C2			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN5482			SN7482			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{OH}	High-level output voltage	Σ1 or Σ2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
		C2		I_{OH} = −200 μA							
V_{OL}	Low-level output voltage	Σ1 or Σ2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.4 V	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
		C2		I_{OL} = 8 mA							
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	A1, B1, or C0	V_{CC} = MAX, V_I = 2.4 V				160			160	μA
		A2 or B2					40			40	
I_{IL}	Low-level input current	A1, B1, or C0	V_{CC} = MAX, V_I = 0.4 V				−6.4			−6.4	mA
		A2 or B2					−1.6			−1.6	
I_{OS}	Short-circuit output current§	Σ1 or Σ2	V_{CC} = MAX		−20		−55	−18		−55	mA
		C2			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			35	50		35	58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, B1 and B2 grounded, and 4.5 V applied to A1, A2, and C0.

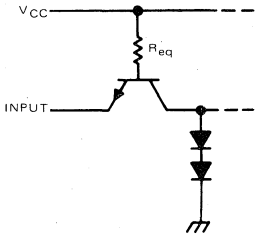
switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{PHL}						40	
t_{PLH}	B2	Σ2				40	ns
t_{PHL}						35	
t_{PLH}	C0	Σ2				38	ns
t_{PHL}						42	
t_{PLH}	C0	C2	C_L = 15 pF, R_L = 780 Ω		12	19	ns
t_{PHL}					17	27	

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

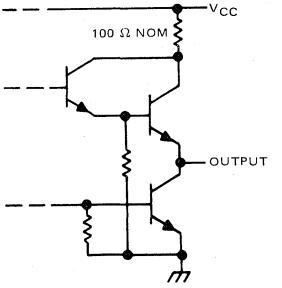
schematics of inputs and outputs

EQUIVALENT OF ALL INPUTS

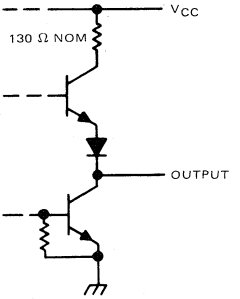


A1, B1, C0: R_{eq} = 1 kΩ NOM
A2, B2: R_{eq} = 4 kΩ NOM

C2 OUTPUT



Σ1 AND Σ2 OUTPUTS



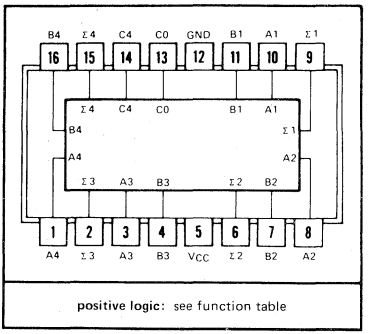
TYPES SN5483A, SN54LS83, SN7483A, SN74LS83
4-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7211853, DECEMBER 1972

- For applications in:
  Digital Computer Systems
  Data-Handling Systems
  Control Systems
- SN54283/SN74283 Are Recommended For New Designs as They Feature Supply Voltage and Ground on Corner Pins to Simplify Board Layout

TYPE	TYPICAL ADD TIMES: TWO 8-BIT WORDS	TYPICAL ADD TIMES: TWO 16-BIT WORDS	TYPICAL POWER DISSIPATION PER 4-BIT ADDER
'83A	23 ns	43 ns	310 mW
'LS83	89 ns	165 ns	75 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. The adders are designed so that logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion. Designed for medium-to-high-speed, the circuits utilize high-speed, high-fan-out transistor-transistor logic (TTL) but are compatible with both DTL and TTL families.

The '83A circuits feature full look ahead across four bits to generate the carry term in typically 10 nanoseconds to achieve partial look-ahead performance with the economy of ripple carry.

The 'LS83 can reduce power requirements to less than 20 mW/bit for power-sensitive applications. These circuits are implemented with single-inversion, high-speed, Darlington-connected serial-carry circuits within each bit.

Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS are characterized for 0°C to 70°C operation.

FUNCTION TABLE

INPUT				OUTPUT: WHEN C0 = L, WHEN C2 = L				WHEN C0 = L, WHEN C2 = H			
A1 A3	B1 B3	A2 A4	B2 B4	Σ1 Σ3	Σ2 Σ4	C2 C4		Σ1 Σ3	Σ2 Σ4	C2 C4	
L	L	L	L	L	L	L		H	L	L	
H	L	L	L	H	L	L		L	H	L	
L	H	L	L	H	L	L		L	H	L	
H	H	L	L	L	H	L		H	H	L	
L	L	H	L	L	H	L		H	H	L	
H	L	H	L	H	H	L		L	L	H	
L	H	H	L	H	H	L		L	L	H	
H	H	H	L	L	L	H		H	L	H	
L	L	L	H	L	H	L		H	H	L	
H	L	L	H	H	H	L		L	L	H	
L	H	L	H	H	H	L		L	L	H	
H	H	L	H	L	L	H		H	L	H	
L	L	H	H	L	L	H		H	L	H	
H	L	H	H	H	L	H		L	H	H	
L	H	H	H	H	L	H		L	H	H	
H	H	H	H	L	H	H		H	H	H	

H = high level, L = low level

NOTE: Input conditions at A3, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

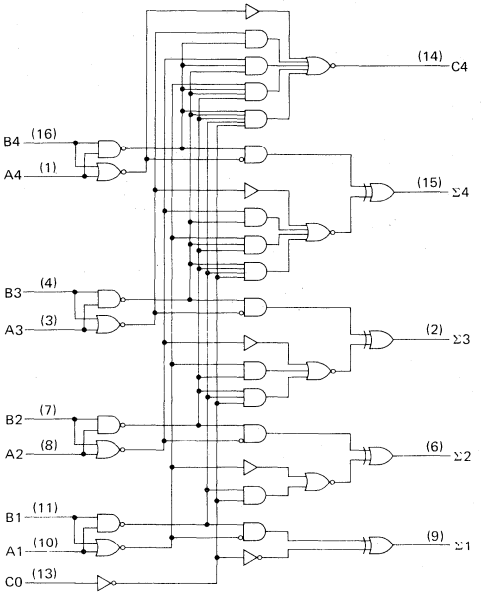
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

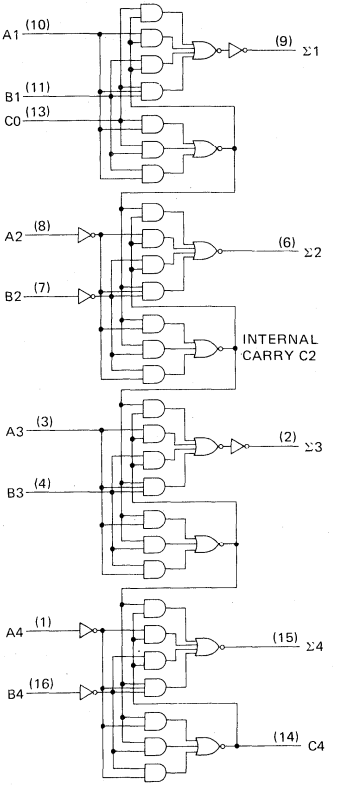
NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the '83A, this rating applies between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4. For the 'LS83, this rating applies between the following pairs: A1 and B1, A1 and C0, B1 and C0, A3 and B3.

functional block diagrams

'83A

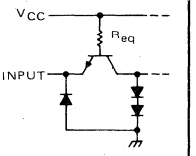


'LS83



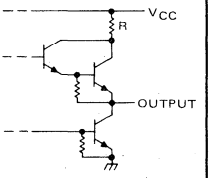
schematics of inputs and outputs

'83A
EQUIVALENT OF EACH INPUT



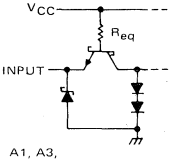
C0 input: R_{eq} = 4 kΩ NOM
Any A or B: R_{eq} = 3.5 kΩ NOM

'83A
TYPICAL OF ALL Σ OUTPUTS



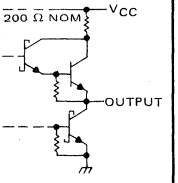
C4 output: R = 100 Ω NOM
Any Σ: R = 120 Ω NOM

'LS83
EQUIVALENT OF EACH INPUT



A1, A3,
B1, B3, C0: R_{eq} = 4.8 kΩ NOM
A2, A4,
B2, B4: R_{eq} = 24 kΩ NOM

'LS83
TYPICAL OF ALL OUTPUTS



recommended operating conditions

		SN5483A			SN7483A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−800			−800	μA
	Output C4			−400			−400	
Low-level output current, I_{OL}	Any output except C4			16			16	mA
	Output C4			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN5483A			SN7483A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = MAX	2.4	3.6		2.4	3.6		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = MAX		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−20		−55	−18		−55	mA
		Output C4			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All B low, other inputs at 4.5 V		56			56		mA
				All inputs at 4.5 V		66	99		66	110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	21	ns
t_{PHL}					12	21	
t_{PLH}	A_i or B_i	Σ_i			16	24	ns
t_{PHL}					16	24	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 780 Ω, See Note 3		9	14	ns
t_{PHL}					11	16	
t_{PLH}	A_i or B_i	C4			9	14	ns
t_{PHL}					11	16	

¶t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

recommended operating conditions

	SN54LS83			SN74LS83			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS83			SN74LS83			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.9	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OH} = −200 μA	2.4	3.4					V
				I_{OH} = −400 μA				2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.4	0.5				V
				I_{OL} = 8 mA					0.5	0.6	
I_I	Input current at maximum input voltage	A1, A3, B1, B3, or C0	V_{CC} = MAX, V_I = 5.5 V				0.4			0.4	mA
		A2, A4, B2, or B4					0.1			0.1	
I_{IH}	High-level input current	A1, A3, B1, B3, or C0	V_{CC} = MAX, V_I = 2.7 V				80			80	μA
		A2, A4, B2, or B4					20			20	
I_{IL}	Low-level input current	A1, A3, B1, B3, or C0	V_{CC} = MAX, V_I = 0.5 V				−1.44			−1.44	mA
		A2, A4, B2, or B4					−0.36			−0.36	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			15	22		15	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs open, all B inputs grounded, and all A inputs and C0 at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1	C_L = 15 pF, R_L = 2 kΩ, See Note 5		23	44	ns
t_{PHL}					29	49	
t_{PLH}	C0	Σ2			31	54	ns
t_{PHL}					33	54	
t_{PLH}	C0	Σ3			41	60	ns
t_{PHL}					48	68	
t_{PLH}	C0	Σ4			53	75	ns
t_{PHL}					49	72	
t_{PLH}	C0	C4			40	59	ns
t_{PHL}					35	55	
t_{PLH}	A2 or B2	Σ2			27	56	ns
t_{PHL}					21	56	
t_{PLH}	A4 or B4	Σ4			26	63	ns
t_{PHL}					21	55	
t_{PLH}	A1	C4			35	55	ns
t_{PHL}					35	55	

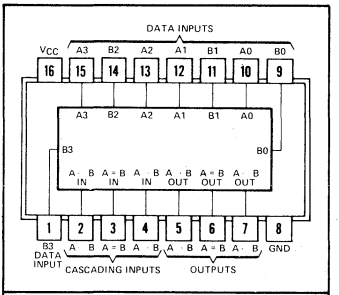
¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Load circuit and voltage waveforms are shown on page 149.

TYPES SN5485, SN54L85, SN54S85, SN7485, SN74L85, SN74S85
4-BIT MAGNITUDE COMPARATORS

BULLETIN NO. DL-S 7211810, DECEMBER 1972

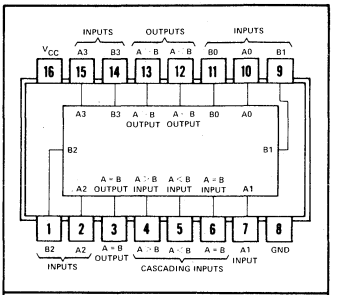
TYPE	TYPICAL POWER DISSIPATION	TYPICAL DELAY (4-BIT WORDS)
'85	275 mW	23 ns
'L85	20 mW	90 ns
'S85	365 mW	11 ns

'85, 'S85
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function tables

'L85
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function tables

description

These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input and additionally for the 'L85, low-level voltages applied to the A > B and A < B inputs. The cascading paths of the '85 and 'S85 are implemented with only a two-gate-level delay to reduce overall comparison times for long words. An alternate method of cascading which further reduces the comparison time is shown in the typical application data.

FUNCTION TABLES

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

'85, 'S85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

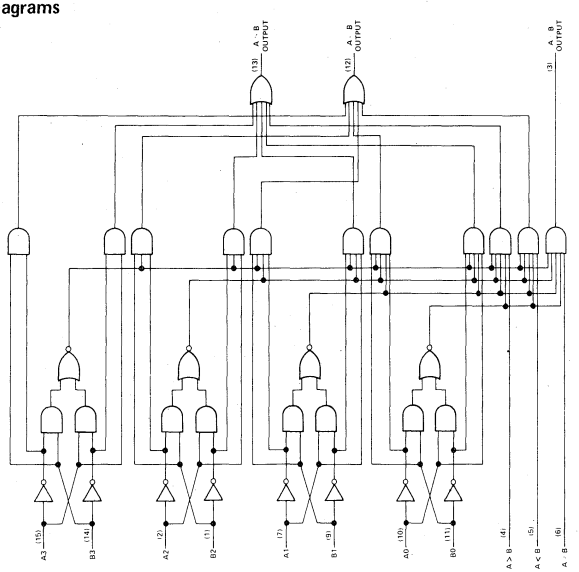
'L85

A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

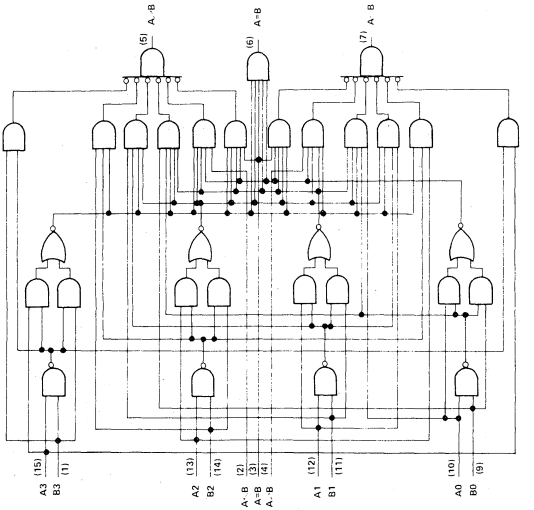
H = high level, L = low level, X = irrelevant

functional block diagrams

'L85

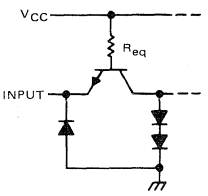


'85, 'S85



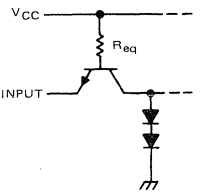
schematics of inputs and outputs

EQUIVALENT OF INPUTS FOR '85



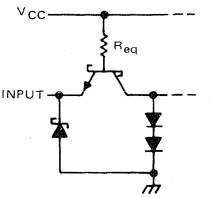
A = B, Any A or B: R_{eq} = 1.67 kΩ NOM
A>B, A<B: R_{eq} = 4 kΩ NOM

EQUIVALENT OF INPUTS FOR 'L85



Any A or B: R_{eq} = 16.7 kΩ NOM
A = B, A>B, A<B: R_{eq} = 40 kΩ NOM

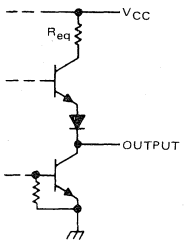
EQUIVALENT OF INPUTS FOR 'S85



A = B, Any A or B: R_{eq} = 933 Ω NOM
A>B, A<B: R_{eq} = 2.8 kΩ NOM

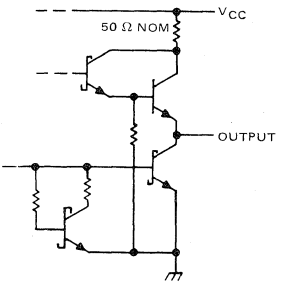
3

TYPICAL OF OUTPUTS FOR '85, 'L85



'85: R_{eq} = 100 Ω NOM
'L85: R_{eq} = 500 Ω NOM

TYPICAL OF OUTPUTS FOR 'S85



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '85, 'S85 . . . . . 7 V
'L85 . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Interemitter voltage (see Note 3) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54L', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. Input voltages for 'L85 must be zero or positive with respect to network ground terminal.
3. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies to each A input in conjunction with its respective B input.

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 2.4 V				40	μA
		all other inputs					120	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		all other inputs					−4.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_O = 0	SN5485	−20		−55	mA
				SN7485	−18		−55	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			55	88	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 400 Ω, See Note 5		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			15		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			7	11	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 5: Load circuit and voltage waveforms are shown on page 148.

recommended operating conditions

	SN54L85			SN74L85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.7	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	SN54L85	2.4	3.3		V
				SN74L85	2.4	3.2		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX	SN54L85		0.15	0.3	V
				SN74L85		0.2	0.4	
I_I	Input current at maximum input voltage	A < B, A > B, or A = B	V_{CC} = MAX, V_I = 5.5 V				100	μA
		A or B inputs					300	
I_{IH}	High-level input current	A < B, A < B, or A = B	V_{CC} = MAX, V_I = 2.4 V				10	μA
		A or B inputs					30	
I_{IL}	Low-level input current	A < B, A > B, or A = B	V_{CC} = MAX, V_I = 0.3 V				−0.18	mA
		A or B inputs					−0.54	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−3		−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 6	Condition A		4.0	7.7	mA
				Condition B		3.2	7.2	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 6: With all outputs open, I_{CC} is measured for Condition A with all inputs at 4.5 V, and for Condition B with all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B	Any	C_L = 50 pF, R_L = 4 kΩ, See Note 7		90	150	ns
t_{PHL}					75	150	
t_{PLH}	A > B, A < B, or A = B	Any			75	150	ns
t_{PHL}					55	100	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 7: Load circuit and voltage waveforms are shown on page 149.

recommended operating conditions

	SN54S85			SN74S85			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S85	2.5	3.4		V
				SN74S85	2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 2.7 V				50	μA
		all other inputs					150	
I_{IL}	Low-level input current	A < B, A > B inputs	V_{CC} = MAX, V_I = 0.5 V				−2	mA
		all other inputs					−6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			73	115	mA
			V_{CC} = MAX, T_A = 125°C, See Note 4	SN54S85N			99	
				SN54S85W			110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 4: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 280 Ω, See Note 5		5		ns
			2			7.5		
			3			10.5	16	
		A = B	4			12	18	
t_{PHL}	Any A or B data input	A < B, A > B	1			5.5		ns
			2			7		
			3			11	16.5	
		A = B	4			11	16.5	
t_{PLH}	A < B or A = B	A > B	1			5	7.5	ns
t_{PHL}	A < B or A = B	A > B	1			5.5	8.5	ns
t_{PLH}	A = B	A = B	2			7	10.5	ns
t_{PHL}	A = B	A = B	2			5	7.5	ns
t_{PLH}	A > B or A = B	A < B	1			5	7.5	ns
t_{PHL}	A > B or A = B	A < B	1			5.5	8.5	ns

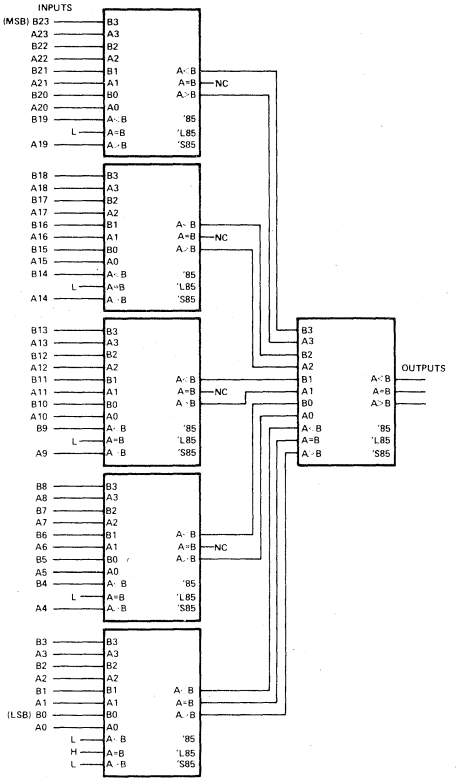
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 5: Load circuit and voltage waveforms are shown on page 148.

TYPICAL APPLICATION DATA

COMPARISON OF TWO N-BIT WORDS

This application demonstrates how these magnitude comparators can be cascaded to compare longer words. The example illustrated shows the comparison of two 24-bit words; however, the scheme is expandable to n-bits. As an example, one comparator can be used with five of the 24-bit comparators illustrated to expand the word length to 120-bits. Typical comparison times for various word lengths using the '85, 'L85, or 'S85 are:

WORD LENGTH	NUMBER OF PKGS	'85	'L85	'S85
1-4 bits	1	23 ns	90 ns	11 ns
5-24 bits	2-6	46 ns	180 ns	22 ns
25-120 bits	8-31	69 ns	270 ns	33 ns



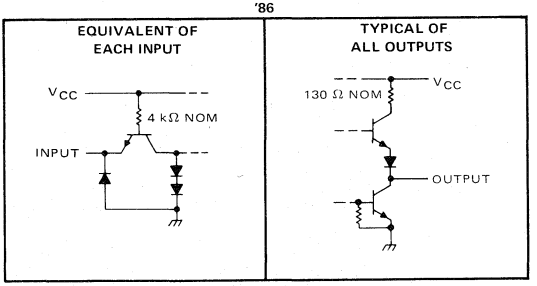
COMPARISON OF TWO 24-BIT WORDS

TYPES SN5486, SN54L86, SN54LS86, SN54S86, SN7486, SN74L86, SN74LS86, SN74S86
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

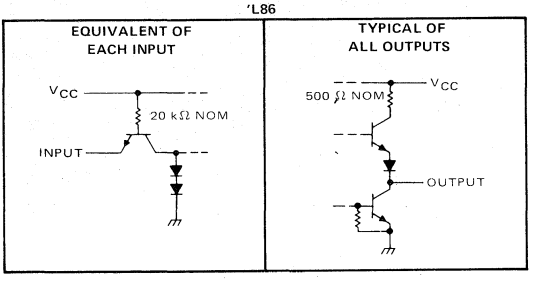
BULLETIN NO. DL-S 7211825, DECEMBER 1972

schematics of inputs and outputs

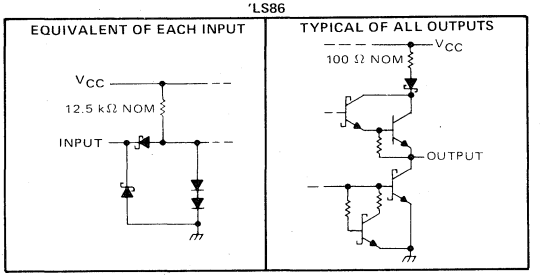
'86



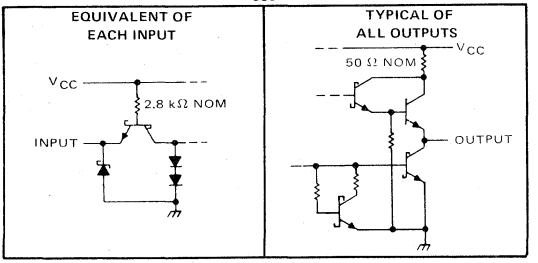
'L86



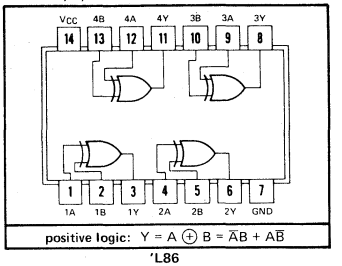
'LS86



'S86

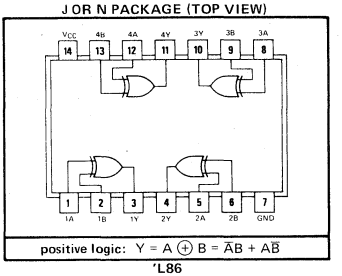


'86, 'LS86, 'S86
J, N, OR W PACKAGE (TOP VIEW)



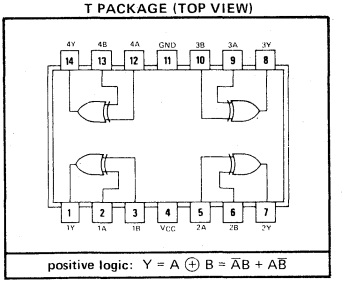
positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

'L86
J OR N PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

'L86
T PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = high level, L = low level

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
'86	14 ns	150 mW
'L86	55 ns	15 mW
'LS86	10 ns	30.5 mW
'S86	7 ns	250 mW

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5486 . . . . . −55°C to 125°C
SN7486 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5486			SN7486			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5486			SN7486			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		30	43		30	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 400 Ω, See Note 3		15	23	ns
t_{PHL}					11	17	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					13	22	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 4) . . . . . 5.5 V
Operating free-air temperature range: SN54L86 . . . . . −55°C to 125°C
SN74L86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
4. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L86			SN74L86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L86			SN74L86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			200			200	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V			−0.36			−0.36	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX, See Note 5		2.2	4.4		2.2	4.4	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 6		3.8	6.68		3.8	6.68	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 5. I_{CCH} is measured with all outputs open, one input of each gate at 4.5 V, and the other inputs grounded.
6. I_{CCL} is measured with all outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 50 pF, R_L = 4 kΩ, See Note 7		75	150	ns
t_{PHL}					60	150	
t_{PLH}	A or B	Other input high			50	90	ns
t_{PHL}					35	60	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 7: Load circuit and voltage waveforms are shown on page 149.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS86 . . . . . −55°C to 125°C
SN74LS86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS86			SN74LS86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS86			SN74LS86			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.6			−0.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 7		10	17	ns
t_{PHL}					10	17	
t_{PLH}	A or B	Other input high			10	17	ns
t_{PHL}					10	17	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 7: Load circuit and voltage waveforms are shown on page 149.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S86 . . . . . −55°C to 125°C
SN74S86 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S86			SN74S86			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54S86			SN74S86			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		50	75		50	75	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

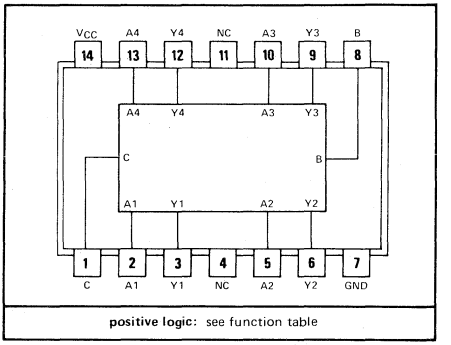
PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 280 Ω, See Note 3		7	10.5	ns
t_{PHL}					6.5	10	
t_{PLH}	A or B	Other input high			7	10.5	ns
t_{PHL}					6.5	10	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54H87, SN74H87
4-BIT TRUE/COMPLEMENT, ZERO/ONE ELEMENT

BULLETIN NO. DL-S 7211837, DECEMBER 1972

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC—No internal connection

description

Operation of these monolithic 4-bit true/complement elements is controlled by the B and C inputs. With the B input low, the 4-bit binary input (A) is transferred to the output (Y) in either complementary form (with C low) or true form (with C high). When the B input is high, the output will be at the complementary level of the C input regardless of the levels of the data inputs.

These circuits are fully compatible for use with other TTL or DTL circuits. Input clamping diodes are provided to minimize transmission line effects and thereby simplify system design. Each input represents only one normalized series 54H/74H load, and full fan-out to 10 series 54H/74H loads is available from each of the outputs in the low-level condition.

Power dissipation is 270 mW typically with an average propagation delay of 14 ns from data inputs to output.

The SN54H87 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H87 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

CONTROL INPUTS		OUTPUTS			
B	C	Y1	Y2	Y3	Y4
L	L	$\overline{A1}$	$\overline{A2}$	$\overline{A3}$	$\overline{A4}$
L	H	A1	A2	A3	A4
H	L	H	H	H	H
H	H	L	L	L	L

H = high level, L = low level
A1, A2, A3, A4 = the level of the respective A input.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54H87 Circuits . . . . . −55°C to 125°C
SN74H87 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54H87			SN74H87			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54H87		54	78	mA
			SN74H87		54	89	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit should not exceed 1 second.
NOTE 2: I_{CC} is measured for the following conditions:
a. All A inputs are at 4.5 V, B and C inputs are grounded, and all outputs are open.
b. B and C inputs are at 4.5 V, all A inputs are grounded, and all outputs are open.

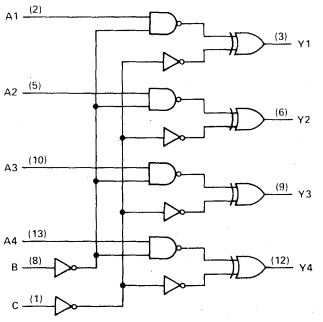
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MAX
t_{PLH}	Propagation delay time, low-to-high-level output from any A input	C_L = 25 pF, R_L = 280 Ω, See Note 3		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from any A input			13	19	ns
t_{PLH}	Propagation delay time, low-to-high-level output from B or C inputs			17	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from B or C inputs			17	25	ns

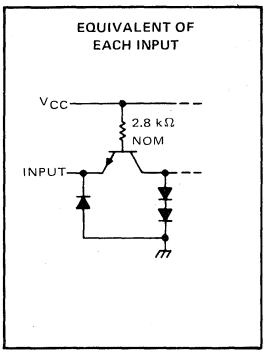
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

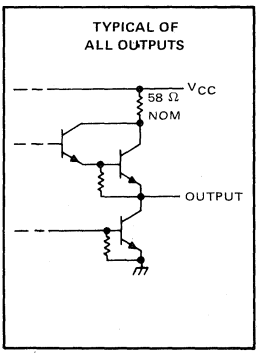
3

functional block diagram



schematics of inputs and outputs



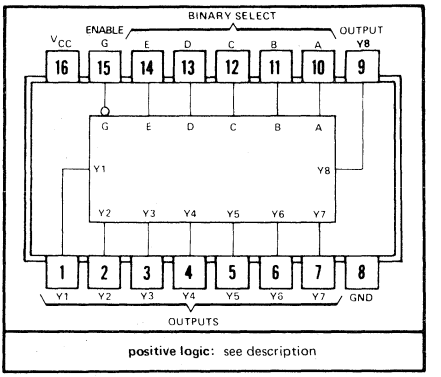


TYPES SN5488A, SN7488A
256-BIT READ-ONLY MEMORIES

BULLETIN NO. DL-S 7211445, JANUARY 1971—REVISED DECEMBER 1972

- Applications in Computer Subroutines
- Useful in Display Systems and Readouts
- Memory Organized as 32 Words of 8 Bits Each
- Input Clamping Diodes Simplify System Design
- Open-Collector Outputs Permit Wire-AND Capability
- Typical Access Time: 25 nanoseconds
- Typical Power Dissipation: 285 milliwatts
- Fully Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



description

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These custom-programmed, 256-bit, read-only memories are organized as 32 words of eight bits each. Each monolithic, high-speed, transistor-transistor logic (TTL), 32-word memory array is addressed in straight 5-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the 32 address gates and cause all eight outputs to remain high (off). Data, as specified by the customer, are permanently programmed into the monolithic structure for the 256 bit locations. This organization is expandable to n-words of N-bit length.

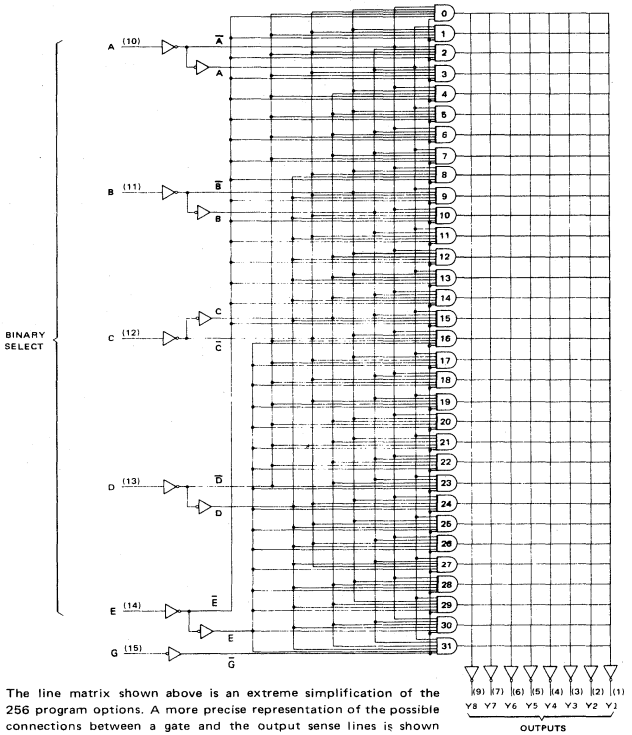
The address of an eight-bit word is accomplished through the buffered, binary select inputs which are decoded by the 32 five-input address gates. When the memory-enable input is high, all 32 gate outputs are low, turning off the eight output buffers.

Data are programmed into the memory at the emitters of 32 eight-emitter transistors. The programming process involves connecting or not connecting each of the 256 emitters. If an emitter is connected, a low-level voltage is read out of that bit location when its decoding gate is addressed. If the emitter is not connected, a high-level voltage is read when addressed. Those decoding-gate output emitters which are used are connected to their repective bit lines to drive the eight output buffers. Since only one decoding gate is addressed at a time, only one of the 32 transistors can supply current to the output buffers at a time.

This memory is fully compatible for use with most TTL or DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and simplify system design. Input buffers lower the fan-in requirement to only one normalized Series 54/74 load for all inputs including enable (G). The open-collector outputs are capable of sinking 12 milliamperes of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor from each output to the supply line (V_{CC}) is required to define the high-level output voltage. Where multiple '88 devices are used in a memory system, the enable input allows easy decoding of additional address bits. Access propagation delay time is typically 25 nanoseconds and power dissipation is typically 285 milliwatts.

The customer can specify the output logic level desired at each of the 256 bit locations by completing the supplementary ordering data and a set of data cards punched in accordance with the data format shown under ordering instructions. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number (not SN5488A or SN7488A). It is important that the customer specify not only the output levels desired at all 256-bit locations, but also the other information requested.

functional block diagram and word selection



The line matrix shown above is an extreme simplification of the 256 program options. A more precise representation of the possible connections between a gate and the output sense lines is shown below.

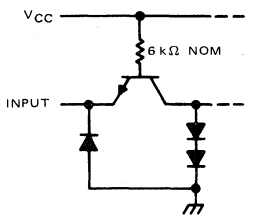
WORD-SELECT TABLE

WORD	INPUTS				
	E	D	C	B	A
0	L	L	L	L	L
1	L	L	L	L	H
2	L	L	L	H	L
3	L	L	L	H	H
4	L	L	H	L	L
5	L	L	H	L	H
6	L	L	H	H	L
7	L	L	H	H	H
8	L	H	L	L	L
9	L	H	L	L	H
10	L	H	L	H	L
11	L	H	L	H	H
12	L	H	H	L	L
13	L	H	H	L	H
14	L	H	H	H	L
15	L	H	H	H	H
16	H	L	L	L	L
17	H	L	L	L	H
18	H	L	L	H	L
19	H	L	L	H	H
20	H	L	H	L	L
21	H	L	H	L	H
22	H	L	H	H	L
23	H	L	H	H	H
24	H	H	L	L	L
25	H	H	L	L	H
26	H	H	L	H	L
27	H	H	L	H	H
28	H	H	H	L	L
29	H	H	H	L	H
30	H	H	H	H	L
31	H	H	H	H	H

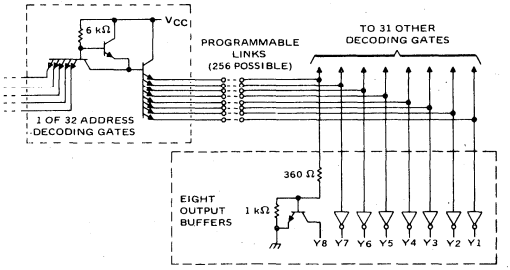
H = high level, L = low level

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



DECODING GATES AND OUTPUT BUFFERS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5488A Circuits . . . . . 55°C to 125°C
SN7488A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN5488A			SN7488A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all outputs low (see Note 2)				64	45	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: All 32 words are addressed separately to ensure that the supply current does not exceed the stated maximum. The typical value shown is for the worst-case condition of all eight outputs driven low at one time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any	C_L = 30 pF,		22	35	ns
t_{PHL}	Enable	Any	R_{L1} = 400 Ω,		22	35	
t_{PLH}	Select	Any	R_{L2} = 600 Ω,		29	45	
t_{PHL}	Select	Any	See Note 3		23	45	

§t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output
NOTE 3: See Load circuit and waveforms shown on page 148.

ORDERING INSTRUCTIONS

Programming instructions for the SN5488A or SN7488A are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 32 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the word specified and describes the levels at the eight outputs for that word. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

DATA CARD FORMAT

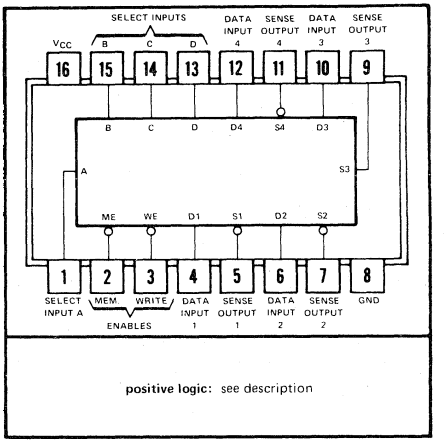
Column	
1-2	Punch a right-justified integer representing the positive-logic binary input address (00-31) for the word described on the card.
3-4	Blank
5	Punch "H" or "L" for output Y8. H = high-voltage-level output, L = low-voltage-level output
6-9	Blank
10	Punch "H" or "L" for output Y7.
11-14	Blank
15	Punch "H" or "L" for output Y6.
16-19	Blank
20	Punch "H" or "L" for output Y5.
21-24	Blank
25	Punch "H" or "L" for output Y4.
26-29	Blank
30	Punch "H" or "L" for output Y3.
31-34	Blank
35	Punch "H" or "L" for output Y2.
36-39	Blank
40	Punch "H" or "L" for output Y1.
41-49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

TYPE SN7489
64-BIT READ/WRITE MEMORY

BULLETIN NO. DL-S 7211386, FEBRUARY 1971–REVISED DECEMBER 1972

- For Application as a "Scratch Pad" Memory with Nondestructive Read-Out
- Fully Decoded Memory Organized as 16 Words of Four Bits Each
- Fast Access Time . . . 33 ns Typical
- Diode-Clamped, Buffered Inputs
- Open-Collector Outputs Provide Wire-AND Capability
- Typical Power Dissipation . . . 375 mW
- Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see description

†Pin assignments for these circuits are the same for all packages.

description

This 64-bit active-element memory is a monolithic, high-speed, transistor-transistor logic (TTL) array of 64 flip-flop memory cells organized in a matrix to provide 16 words of four bits each. Each of the 16 words is addressed in straight binary with full on-chip decoding.

The buffered memory inputs consist of four address lines, four data inputs, a write enable, and a memory enable for controlling the entry and access of data. The memory has open-collector outputs which may be wire-AND connected to permit expansion up to 4704 words of N-bit length without additional output buffering. The open-collector outputs may be utilized to drive external loads directly; however, dynamic reponse of an output can, in most cases, be improved by using an external pull-up resistor in conjunction with a partially loaded output. Access time is typically 33 nanoseconds; power dissipation is typically 375 milliwatts.

FUNCTION TABLE

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	Complement of Data Inputs
L	H	Read	Complement of Selected Word
H	L	Inhibit Storage	Complement of Data Inputs
H	H	Do Nothing	High

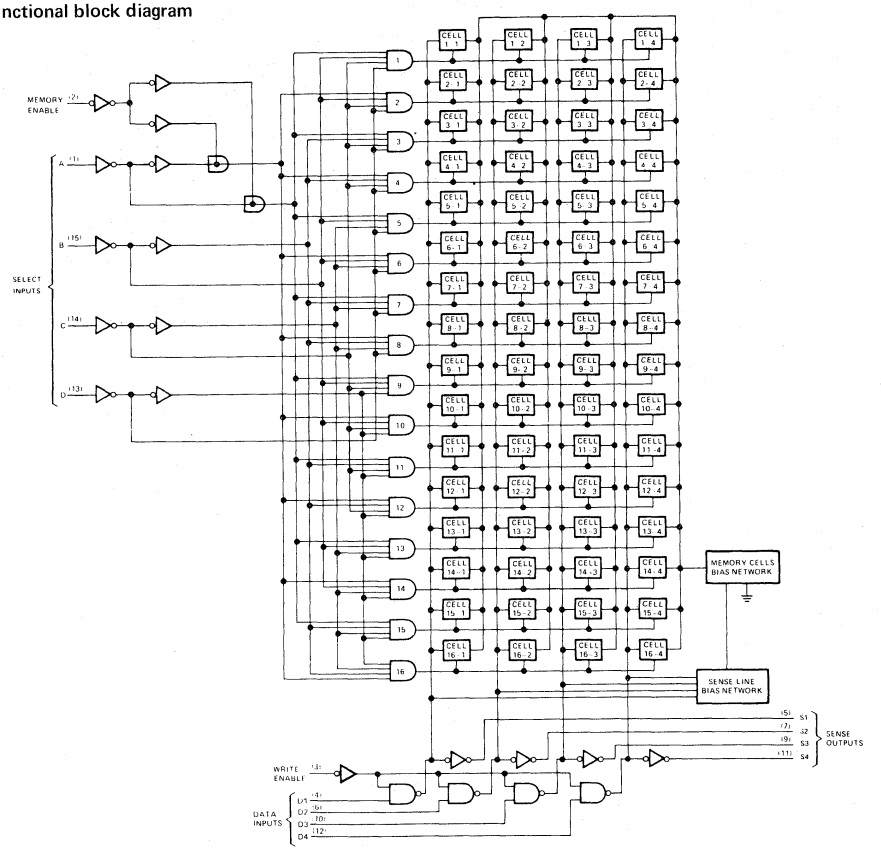
write operation

Information present at the data inputs is written into the memory by addressing the desired word and holding both the memory enable and write enable low. Since the internal output of the data input gate is common to the input of the sense amplifier, the sense output will assume the opposite state of the information at the data inputs when the write enable is low.

read operation

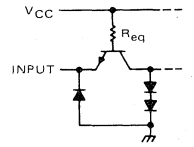
The complement of the information which has been written into the memory is nondestructively read out at the four sense outputs. This is accomplished by holding the memory enable low, the write enable high, and selecting the desired address.

functional block diagram



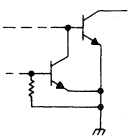
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



D1, D2, D3, D4: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
High-level output voltage, V_{OH} (see Notes 1 and 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Width of write-enable pulse, t_w	40			ns
Setup time, data input with respect to write enable, t_{setup} (see Figure 1)	40			ns
Hold time, data input with respect to write enable (see Figure 1)	5			ns
Select input setup time with respect to write enable, t_{setup}	0			ns
Select input hold time after writing, t_{hold} (see Figure 1)	5			ns
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,		I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,		V_{IH} = 2 V, V_{OH} = 5.5 V			20	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 12 mA			0.4	V
				I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,		V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,		V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,		V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX,		See Note 3		75	105	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz		V_O = 2.4 V,		4		pF

NOTE 3: I_{CC} is measured with the memory enable grounded, all other inputs at 4.5 V, and all outputs open.

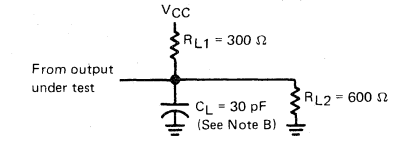
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

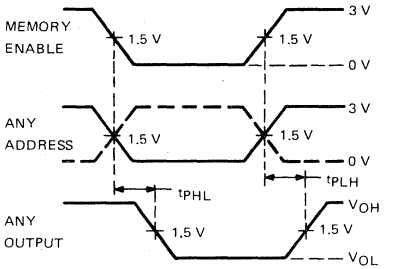
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from memory enable		C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1		26	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from memory enable				33	50	
t_{PLH}	Propagation delay time, low-to-high-level output from select				30	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select				35	60	
t_{SR}	Sense recovery time after writing	output initially high			39	70	ns
		output initially low			48	70	

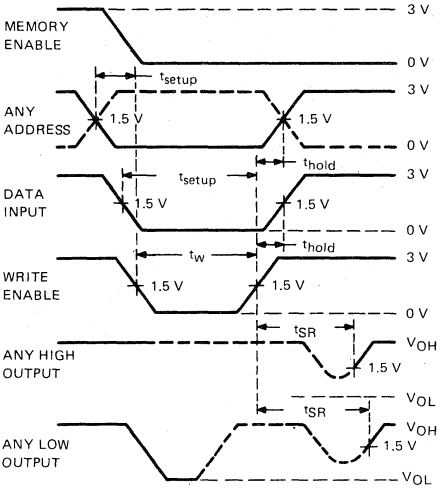
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



READ CYCLE



WRITE CYCLE FROM WRITE ENABLE

NOTES: A. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

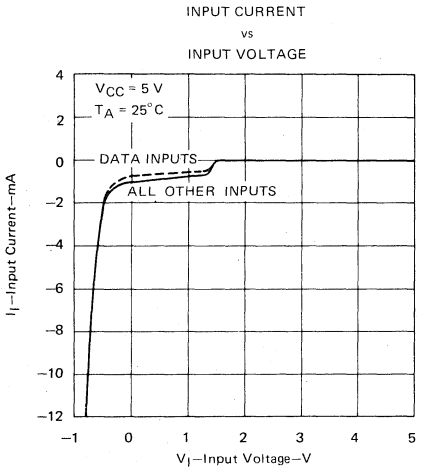


FIGURE 2

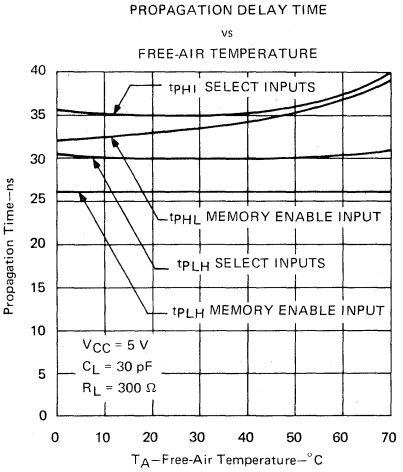


FIGURE 3

TYPES SN5490A, SN5492A, SN5493A, SN54L90, SN54L93, SN7490A, SN7492A, SN7493A, SN74L90, SN74L93 DECADE, DIVIDE-BY-TWELVE, AND BINARY COUNTERS

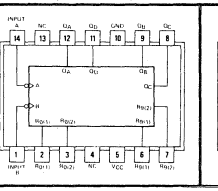
BULLETIN NO. DL-S 7211807, DECEMBER 1972

'90A, 'L90 . . . DECADE COUNTERS

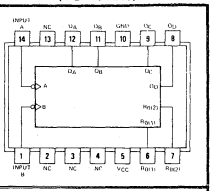
'92A . . . DIVIDE-BY-TWELVE COUNTER

'93A, 'L93 . . . 4-BIT BINARY COUNTERS

'90A . . . J, N, OR W PACKAGE
'L90 . . . J, N, OR T PACKAGE (TOP VIEW)

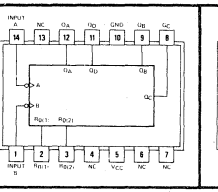


'92A . . . J, N, OR W PACKAGE (TOP VIEW)

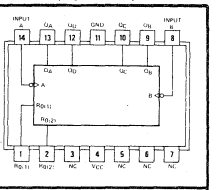


positive logic: see function tables

'93A . . . J, N, OR W PACKAGE (TOP VIEW)



'L93 . . . J, N, OR T PACKAGE (TOP VIEW)



positive logic: see function tables

NC—No internal connection

description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '90A and 'L90, divide-by-six for the '92A, and divide-by-eight for the '93A and 'L93.

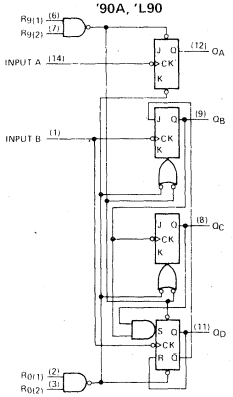
All of these counters have a gated zero reset and the '90A and 'L90 also have gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade, divide-by-twelve, or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '90A or 'L90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

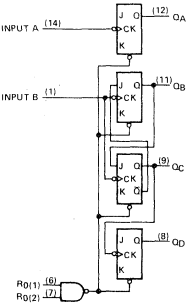
TYPES	TYPICAL POWER DISSIPATION
'90A	145 mW
'L90	20 mW
'92A, '93A	130 mW
'L93	16 mW

functional block diagrams

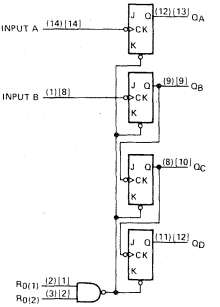
'90A, 'L90



'92A



'93A, 'L93



⊲ . . . dynamic input activated by transition from a high level to a low level.

The J and K inputs shown without connection are for reference only and are functionally at a high level.

'90A, 'L90
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'90A, 'L90
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'90A, 'L90
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'92A
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

'93A, 'L93
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

'92A, '93A, 'L93
RESET/COUNT FUNCTION TABLE

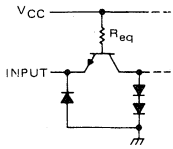
RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

'90A, '92A, '93A

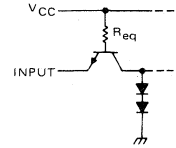
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
A	2.5 kΩ
B ('90A, '92A)	1.25 kΩ
B ('93A)	2.5 kΩ
All resets	6 kΩ

'L90, 'L93

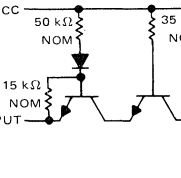
EQUIVALENT OF EACH INPUT
EXCEPT A AND B OF 'L93



INPUT	R_{eq} NOM
A ('L90)	13.3 kΩ
B ('L90)	6.67 kΩ
All resets	40 kΩ

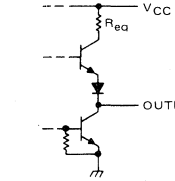
'L93

EQUIVALENT OF A OR B
INPUT



'90A, '92A, '93A, 'L90, 'L93

TYPICAL OF ALL
OUTPUTS



'90A, '92A, '93A: R = 100 Ω NOM
'L90, 'L93: R = 500 Ω NOM

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5490A, SN5492A, SN5493A . . . . . −55°C to 125°C
SN7490A, SN7492A, SN7493A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '90A circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN5490A, SN5492A, SN5493A			SN7490A, SN7492A, SN7493A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count} (see Figure 1)	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup, t_{setup}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'90A MIN	'90A TYP‡	'90A MAX	'92A MIN	'92A TYP‡	'92A MAX	'93A MIN	'93A TYP‡	'93A MAX	UNIT
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	Any reset	V_{CC} = MAX, V_I = 2.4 V			40			40			40	μA
		A input				80			80			80	
		B input				120			120			80	
I_{IL}	Low-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6			−1.6	mA
		A input				−3.2			−3.2			−3.2	
		B input				−4.8			−4.8			−3.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	−20		−57	−20		−57	mA
			SN74'	−18		−57	−18		−57	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3			29	42		26	39		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'90A			'92A			'93A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Figure 1	32	42		32	42		32	42		MHz
	B	Q_B		16			16			16			
t_{PLH}	A	Q_A			10	16		10	16		10	16	ns
t_{PHL}					12	18		12	18		12	18	
t_{PLH}	A	Q_D			32	48		32	48		46	70	ns
t_{PHL}					34	50		34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16		10	16	ns
t_{PHL}					14	21		14	21		14	21	
t_{PLH}	B	Q_C			21	32		10	16		21	32	ns
t_{PHL}					23	35		14	21		23	35	
t_{PLH}	B	Q_D			21	32		21	32		34	51	ns
t_{PHL}					23	35		23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30							ns
t_{PHL}		Q_B, Q_C			26	24							

¶ f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 8 V
Input voltage (see Note 5) . . . . . 5.5 V
Operating free-air temperature range: SN54L90, SN54L93 Circuits . . . . . −55°C to 125°C
SN74L90, SN74L93 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 4. Voltage values are with respect to network ground terminal.
5. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L90, SN54L93			SN74L90, SN74L93			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Input count frequency, f_{count}	0		3	0		3	MHz
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Width of input count pulse, $t_{w(count)}$	200			200			ns
Width of reset pulse, $t_{w(reset)}$	200			200			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	'L90			'L93			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_{OH}	High-level output voltage	SN54L'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.3		V
		SN74L'		2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage	SN54L'	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX¶		0.15	0.3		0.15	0.3	V
		SN74L'			0.2	0.4		0.2	0.4	
I_I	Input current at maximum input voltage	Any reset input	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		A input				300			200	
		B input				600			200	
I_{IH}	High-level input current	Any reset input	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		A input				30			20	
		B input				60			20	
I_{IL}	Low-level input current	Any reset input	V_{CC} = MAX, V_I = 0.3 V			−0.18			0.18	mA
		A input				−0.54			0.36	
		B input				−1.08			0.36	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		4	7.2		3.2	6.6	mA

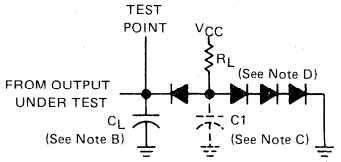
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Outputs are tested at I_{OL} = MAX plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

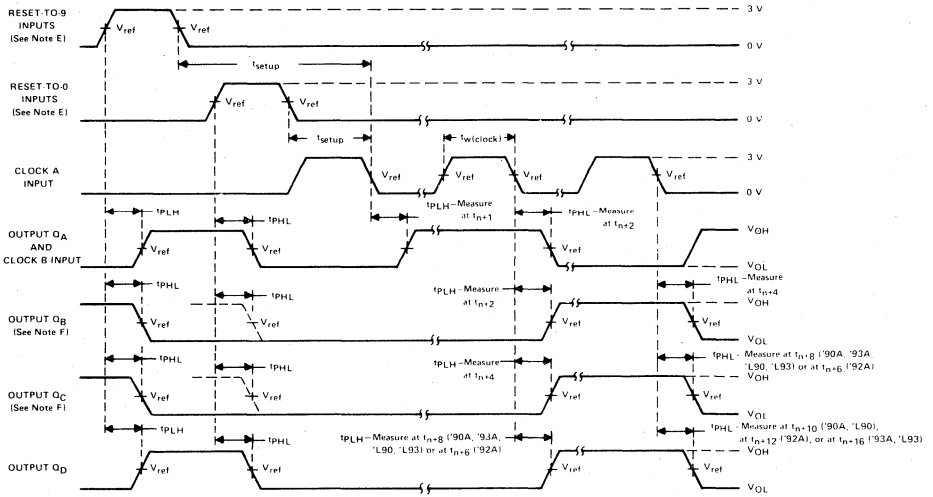
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'L90			'L93			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Maximum count frequency		3	6		3	6		MHz
t_{PLH}	Propagation delay time, low-to-high-level Q_D output from input A	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		230	340		280	450	ns
t_{PHL}	Propagation delay time, high-to-low-level Q_D output from input A			230	340		280	450	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics:
for '90A, '92A, '93A, $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'L90, $t_r \leq 15$ ns, $t_f \leq 15$ ns, PRR = 500 kHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms;
for 'L93, $t_r \leq 15$ ns, $t_f \leq 15$ ns, PRR = 500 kHz, duty cycle = 50%, $Z_{out} \approx 50$ ohms.

B. C_L includes probe and jig capacitance.

C. C1 (30 pF) is applicable for testing 'L90 and 'L93.

D. All diodes are 1N916 or 1N3064.

E. Each reset input is tested separately with the other reset at 4.5 V.

F. Reference waveforms are shown with dashed lines.

G. For '90A, '92A, and '93A; V_{ref} = 1.5 V. For 'L90 and 'L93; V_{ref} = 1.3 V.

FIGURE 1

TYPES SN5491A, SN54L91, SN7491A, SN74L91
8-BIT SHIFT REGISTERS

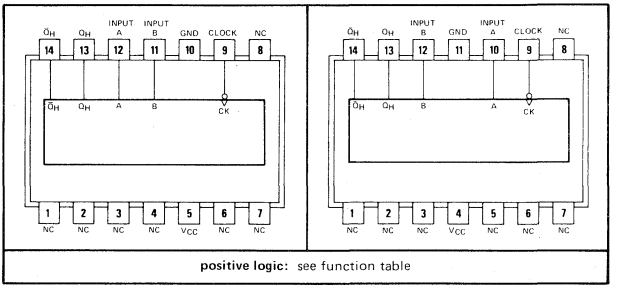
BULLETIN NO. DL-S 7211854, DECEMBER 1972

MSI TTL SHIFT REGISTERS
for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

'91A, 'L91 . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

'91A . . . W
'L91 . . . T
FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC—No internal connection

logic

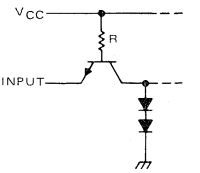
FUNCTION TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+8}	
A	B	Q	$\overline{Q}_H$
H	H	H	L
L	X	L	H
X	L	L	H

H = high, L = low, X = irrelevant
t_n = Reference bit time, clock low
t_{n+8} = Bit time after 8 low-to-high clock transitions.

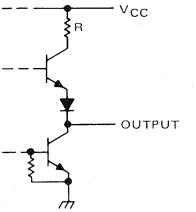
schematics of inputs and outputs

EQUIVALENT OF ALL INPUTS



'91A: R = 4 kΩ NOM
'L91: R = 40 kΩ NOM

TYPICAL OF BOTH OUTPUTS



'91A: R = 130 Ω NOM
'L91: R = 500 Ω NOM

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'91A	18 MHz	175 mW
'L91	6.5 MHz	17.5 mW

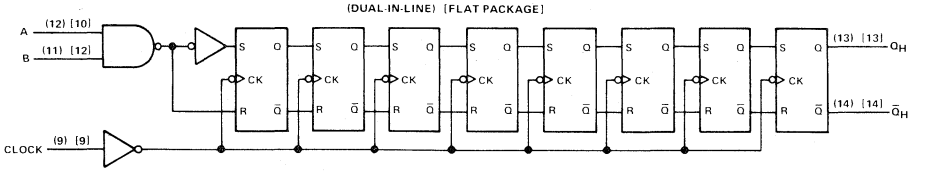
description

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

Series 54 and 54L devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74L devices are characterized for operation from 0°C to 70°C.

functional block diagram

(DUAL-IN-LINE) (FLAT PACKAGE)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5491A Circuits . . . . . −55°C to 125°C
SN7491A Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5491A			SN7491A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Width of clock input pulse, t_w	25			25			ns
Setup time, t_{setup} (see Figure 1)	25			25			ns
Hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5491A			SN7491A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3		35	50		35	58	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	10	18		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			24	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output			27	40	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L91 Circuits . . . . . −55°C to 125°C
SN74L91 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L91			SN74L91			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−100			−200	μA
Low-level output current, I_{OL}				2			3.6	mA
Width of clock input pulse, $t_{w(clock)}$	High logic level	100			100			ns
	Low logic level	150			150			ns
Setup time, t_{setup} (see Figure 1)		120			120			ns
Hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

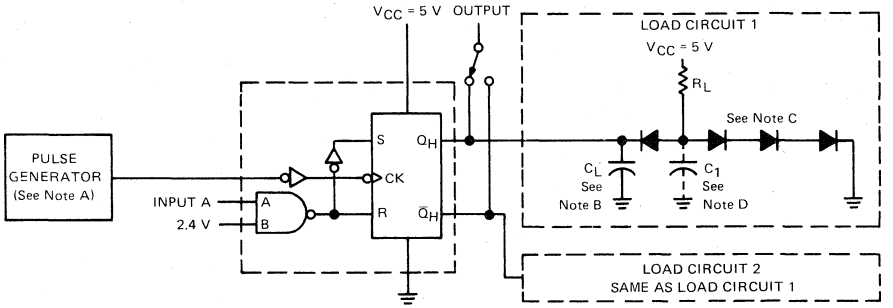
PARAMETER		TEST CONDITIONS†	SN54L91			SN74L91			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3		3.5	6.6		3.5	6.6	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 3: I_{CC} is measured after the eighth clock pulse with the outputs open and A and B inputs grounded.

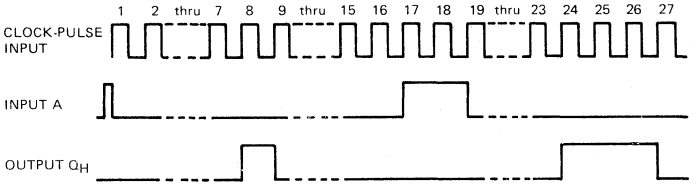
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L 50 pF, R_L = 4 kΩ, See Figure 1	3	6.5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			55	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	150	ns

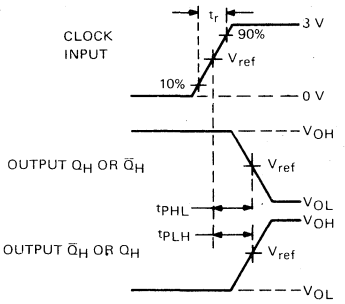
PARAMETER MEASUREMENT INFORMATION



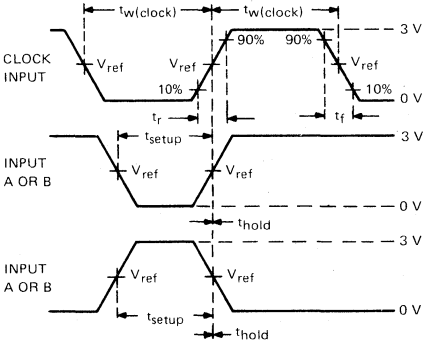
TEST CIRCUIT



TYPICAL INPUT/OUTPUT WAVEFORMS



PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



SWITCHING TIMES VOLTAGE WAVEFORMS

NOTES: A. The generator has the following characteristics: $t_{w(clock)} \approx 500\ \mu s$, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$. For SN5491A/SN7491A, $t_r \leq 10$ ns and $t_f \leq 10$ ns; for SN54L91/SN74L91, $t_r \leq 15$ ns and $t_f \leq 15$ ns.

B. C_L includes probe and jig capacitance.

C. For testing Series 54/74 deivces, all diodes are 1N3064; for testing Series 54L/74L deivces, all diodes are 1N916.

D. C_1 = 30 pF and is used for SN54L91/SN74L91 only.

E. For SN5491A/SN7491A, V_{ref} = 1.5 V; for SN54L91/SN74L91, V_{ref} = 1.3 V.

FIGURE 1–SWITCHING TIMES

TYPES SN5494, SN7494
4-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7211812, DECEMBER 1972

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS
for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

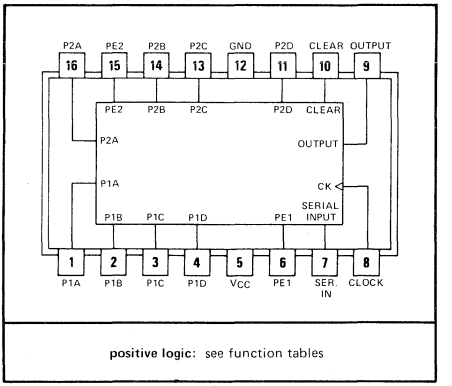
description

These monolithic shift registers which utilize transistor-transistor logic (TTL) circuits in the familiar Series 54/74 configuration, are composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to a low output level by applying a high-level voltage to the clear input while the internal presets are inactive (high). See the preset function table below. Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to either the P1 or P2 inputs of each register stage (A, B, C, and D) with the corresponding preset enable input, PE1 or PE2, high. Presetting, like clearing, is independent of the level of the clock input.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function tables

Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be setup at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a low level and the internal presets must be inactive (high) when clocking occurs.

PRESET FUNCTION TABLE
(BIT A, TYPICAL OF ALL)

PRESET INPUTS				INTERNAL
PE1	P1A	PE2	P2A	PRESET A
L	X	L	X	H (inactive)
L	X	X	L	H (inactive)
X	L	L	X	H (inactive)
X	L	X	L	H (inactive)
H	H	X	X	L (active)
X	X	H	H	L (active)

REGISTER FUNCTION TABLE

INTERNAL PRESETS				INPUTS			INTERNAL OUTPUTS			OUTPUT
A	B	C	D	CLEAR	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D
H	H	H	H	H	X	X	L	L	L	L
L	L	L	L	L	X	X	H	H	H	H
H	H	H	H	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	L	H	L	L	X	H	Q_{B0}	H	Q_{D0}
H	H	H	H	L	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	H	H	L	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}

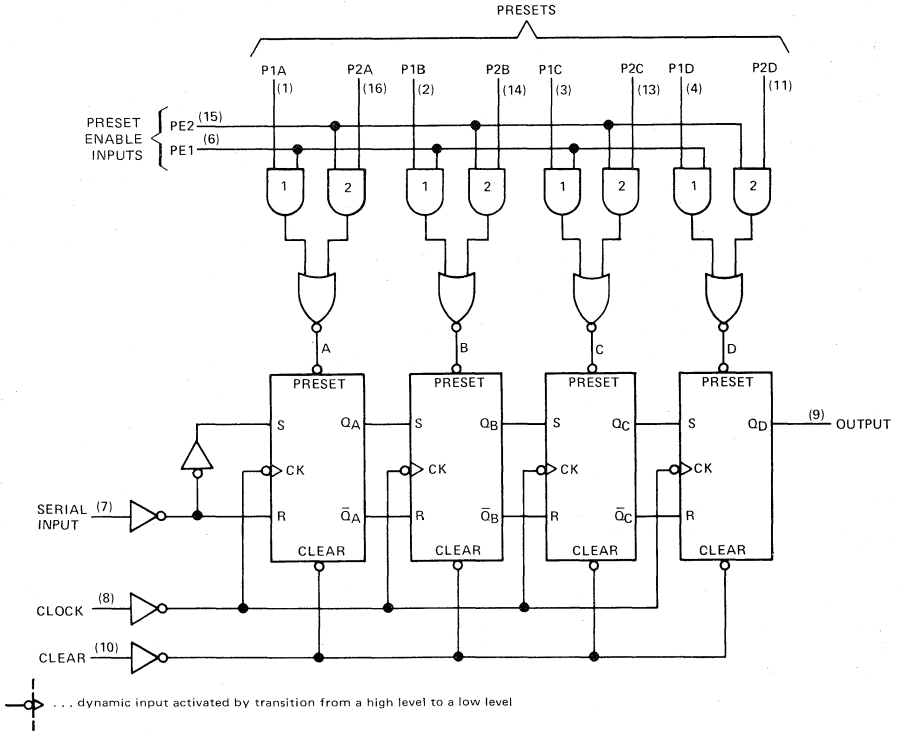
H = high level (steady state), L = low level (steady state), X = irrelevant, ↑ = transition from low to high level
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5494 Circuits . . . . . −55°C to 125°C
SN7494 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

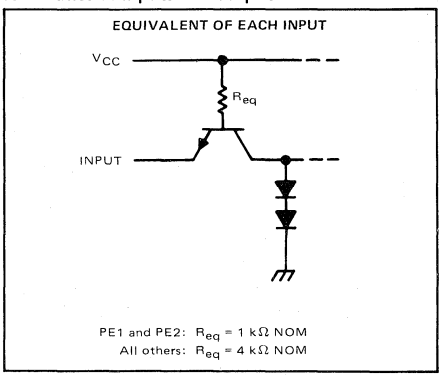
NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

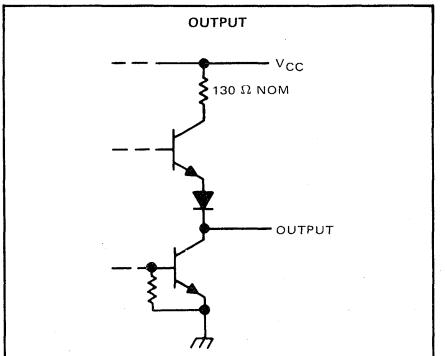
functional block diagram



. . . dynamic input activated by transition from a high level to a low level

schematics of inputs and output





recommended operating conditions

		SN5494			SN7494			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, $t_{w(clock)}$		35			35			ns
Width of clear pulse, $t_{w(clear)}$		30			30			ns
Width of preset pulse, $t_{w(preset)}$		30			30			ns
Setup time, t_{setup}	High-level data	35			35			ns
	Low-level data	25			25			
Hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5494			SN7494			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 2.4 V			160			160	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Presets 1 and 2	V_{CC} = MAX, V_I = 0.4 V			−6.4			−6.4	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		35	50		35	58	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the outputs open, clear grounded following momentary application of 4.5 V, both preset-enable inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 4	10			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			25	40	ns
t_{PHL}	Propgaation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset				35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				40	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 148.

TYPES SN5495A, SN54L95, SN54LS95A, SN7495A, SN74L95, SN74LS95A 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7211872, DECEMBER 1972

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
'L95	5 MHz	19 mW
'LS95A	28 MHz	50 mW

description

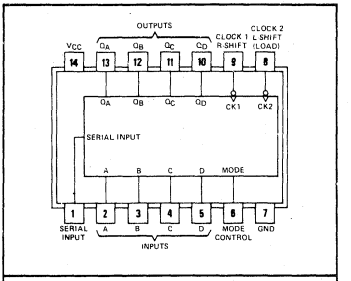
These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (Broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

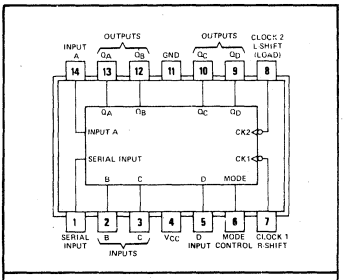
Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

'95A and 'LS95A
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

'L95
J OR N DUAL-IN-LINE
OR T FLAT PACKAGE (TOP VIEW)



positive logic: see function table

FUNCTION TABLE

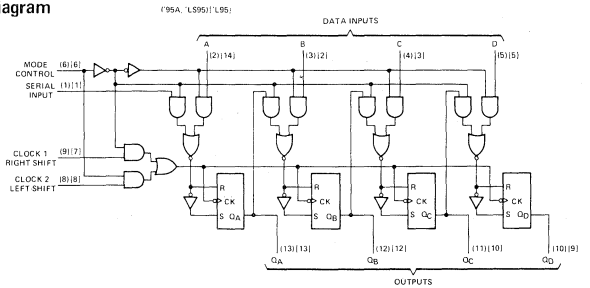
MODE CONTROL	CLOCKS 2 (L)	CLOCKS 1 (R)	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	OUTPUTS Q_A	OUTPUTS Q_B	OUTPUTS Q_C	OUTPUTS Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

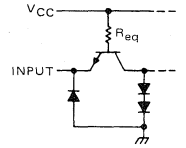
functional block diagram

('95A, 'LS95)/('L95)



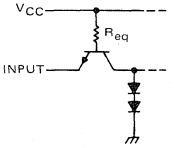
schematics of inputs and outputs

EQUIVALENT OF INPUTS OF '95A



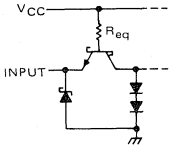
Mode control: R_{eq} = 3 kΩ NOM
Clock inputs: R_{eq} = 4 kΩ NOM
All other inputs: R_{eq} = 6 kΩ NOM

EQUIVALENT OF INPUTS OF 'L95



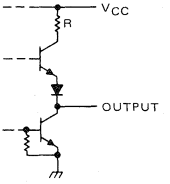
Mode control: R_{eq} = 20 kΩ NOM
All other inputs: R_{eq} = 40 kΩ NOM

EQUIVALENT OF INPUTS OF 'LS95A



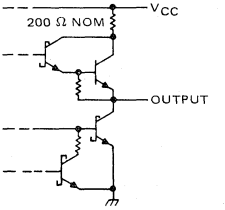
Mode control: R_{eq} = 8.57 kΩ NOM
Clock inputs: R_{eq} = 15 kΩ NOM
All other inputs: R_{eq} = 20 kΩ NOM

TYPICAL OF OUTPUTS OF '95A, 'L95



'95A: R = 100 Ω
'L95: R = 500 Ω

TYPICAL OF OUTPUTS OF 'LS95A



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1): '95A, 'LS95A . . . . . 7 V
'L95 . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Interemitter voltage (see Note 3) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54L', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. For the 'L95, input voltages must be zero or positive with respect to network ground terminal.
3. This is the voltage between two emitters of a multiple-emitter input transistor. For these devices, this ratings applies between the clock-2 input and the mode control input.

recommended operating conditions

	SN5495A			SN7495A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	20	10		15	10		ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1)	10			10			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	15			15			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	15			15			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	5			5			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5495A			SN7495A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Mode control				80			80	
I_{IL}	Low-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Mode control				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		39	63		39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32	ns

recommended operating conditions

	SN54L95			SN74L95			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Clock frequency, f_{clock}	0		3	0		3	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	200			200			ns
Setup time, high-level data, t_{setup} (see Figure 1)	100			100			ns
Setup time, low-level data, t_{setup} (see Figure 1)	120			120			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	225			225			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	200			200			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	100			100			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54L95			SN74L95			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		Mode control				200			200	
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		Mode control				20			20	
I_{IL}	Low-level input current	Serial, A, B, C, D, clock 1 or 2	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
		Mode control				−0.36			−0.36	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 4		3.8	9		3.8	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 4 kΩ, See Figure 1	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			125	200	ns

recommended operating conditions

	SN54LS95A			SN74LS95A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	25			25			ns
Setup time, high-level or low-level data, t_{setup} (see Figure 1)	20			20			ns
Hold time, high-level or low-level data, t_{hold} (see Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 2)	20			20			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 2)	20			20			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 2)	20			20			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 2)	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

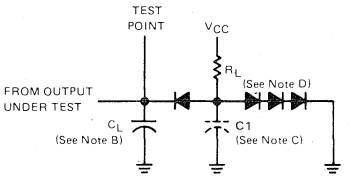
PARAMETER			TEST CONDITIONS†		SN54LS95A			SN74LS95A			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA			0.4				V
				I_{OL} = 8 mA						0.5	
I_I	Input current at maximum input voltage	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
		Mode control					0.2			0.2	
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Mode control					40			40	
I_{IL}	Low-level input current	Serial, A, B, C, D	V_{CC} = MAX,	V_I = 0.4 V			−0.36			−0.36	mA
		Clock 1 or 2					−0.44			−0.44	
		Mode Control					−0.72			−0.72	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX,	See Note 4		10	17		10	17	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 4: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

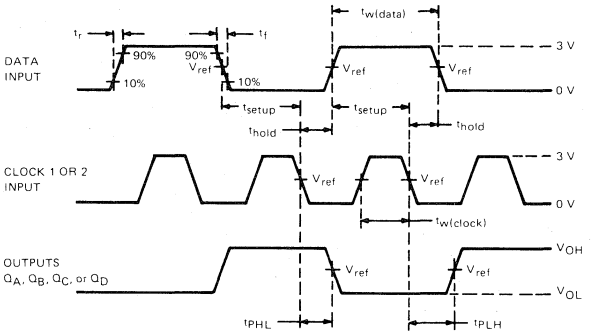
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	20	28		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			30	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			35	48	ns

PARAMETER MEASUREMENT INFORMATION

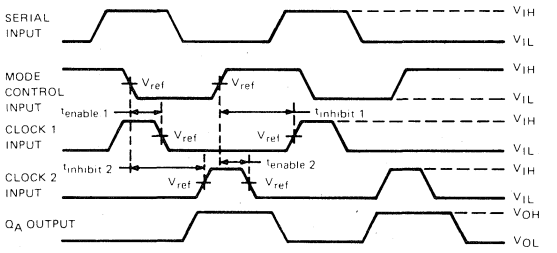


LOAD CIRCUIT



NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \approx 50\ \Omega$. For the data pulse generator, PRR = 500 kHz; for the clock pulse generator, PRR = 1 MHz. When testing f_{max}, vary PRR. For '95A, $t_{w(data)} \geq 20$ ns; $t_{w(clock)} \geq 15$ ns. For 'L95, $t_{w(data)} \geq 150$ ns; $t_{w(clock)} \geq 200$ ns. For 'LS95A, $t_{w(data)} \geq 20$ ns, $t_{w(clock)} \geq 15$ ns.
B. C_L includes probe and jig capacitance.
C. C1 (30 pF) is applicable for testing 'L95.
D. All diodes are 1N916 or 1N3064.
E. For '95A, $V_{ref} = 1.5$ V; for 'L95 and 'LS95A, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 1–SWITCHING TIMES



NOTES: A. Input A is at a low level.
B. For '95A, $V_{ref} = 1.5$ V; for 'L95 and 'LS95A, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 2–CLOCK ENABLE/INHIBIT TIMES

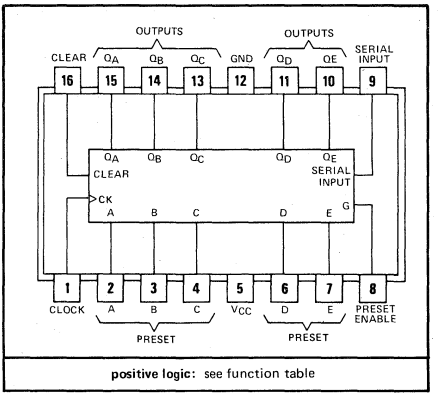
TYPES SN5496, SN54L96, SN7496, SN74L96
5-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7211821, DECEMBER 1972

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

TYPE	PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'96	25 ns	240 mW
'L96	50 ns	120 mW

'96 . . . J, N, OR W PACKAGE
'L96 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

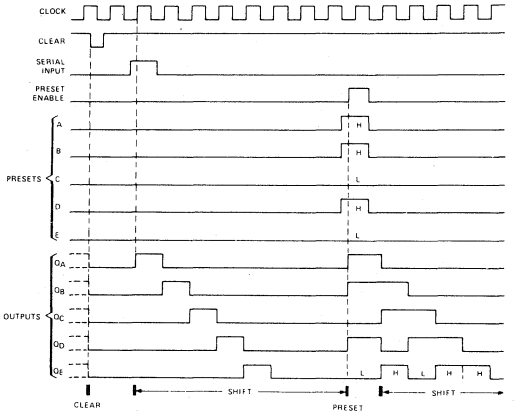
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	PRESET ENABLE	PRESET A	B	C	D	E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

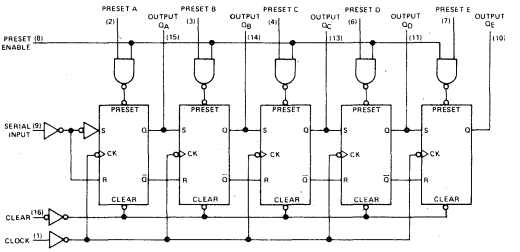
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most-recent ↑ transition of the clock.

typical clear, shift, preset, and shift sequences



3

functional block diagram

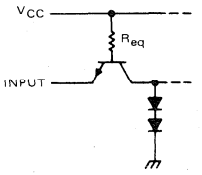


. . . dynamic input activated by transition from a high level to a low level.

schematics of inputs and outputs

'96

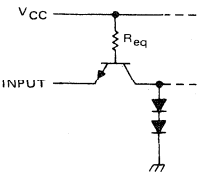
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Preset enable	800 Ω
All others	4 kΩ

'L96

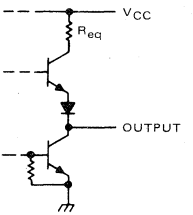
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Preset enable	1.6 kΩ
All others	8 kΩ

'96, 'L96

TYPICAL OF ALL OUTPUTS



'96: R_{eq} = 130 Ω NOM
'L96: R_{eq} = 260 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input Voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN5496 . . . . . −55°C to 125°C
SN7496 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_{w(clock)}$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5496			SN7496			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	any input except preset enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		preset enable				200			200	
I_{IL}	Low-level input current	any input except preset enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		preset enable				−8			−8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		48	68		48	79	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 400 Ω, See Figure 1		25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				55	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 5) . . . . . 8 V
Input voltage (see Note 6) . . . . . 5.5 V
Operating free-air temperature range: SN54L96 . . . . . −55°C to 125°C
SN74L96 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 5. Voltage values are with respect to network ground terminal.
6. Input voltage must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L96			SN74L96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−200	μA
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		5	0		5	MHz
Width of clock, preset, or clear input pulse, t_w	100			100			ns
Serial input setup time, t_{setup} (see Figure 1)	100			100			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

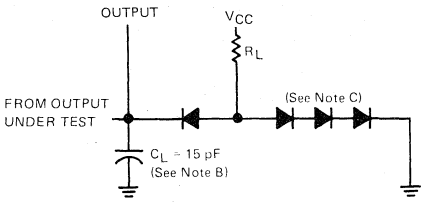
PARAMETER			TEST CONDITIONS†	SN54L96			SN74L96			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA	2.4	3.2		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	any input except preset enable	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
		preset enable				100			100	
I_{IL}	Low-level input current	any input except preset enable	V_{CC} = MAX, V_I = 0.4 V			−0.8			−0.8	mA
		preset enable				−4			−4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−10		−29	−9		−29	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		24	34		24	40	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

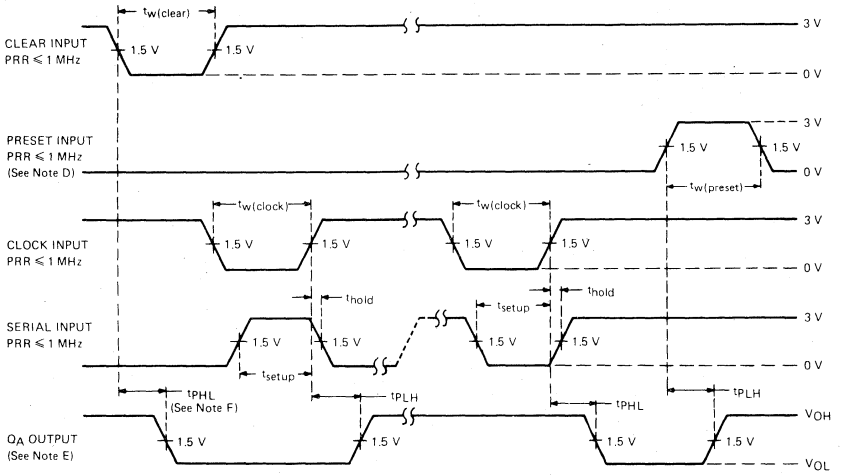
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 800 Ω, See Figure 1		50	80	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			50	80	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable			56	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				110	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by pulse generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
E. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.
F. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

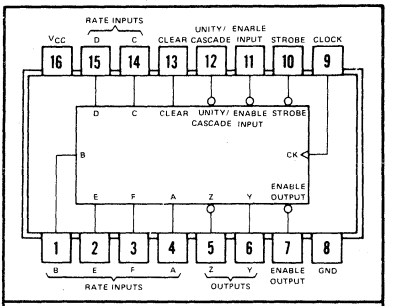
FIGURE 1–SWITCHING TIMES

TYPES SN5497, SN7497
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS

BULLETIN NO. DL-S 7211802, DECEMBER 1972

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

SN5497 . . . J OR W PACKAGE
SN7497 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic: see description

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These six-bit serial binary counters feature buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

3

The counter is enabled when the clear, strobe, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 64, ie.:

$$f_{out} = \frac{M \cdot f_{in}}{64}$$

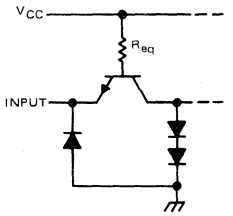
where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

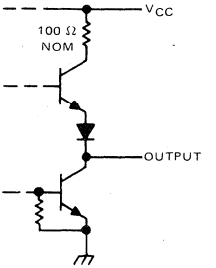
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Clock input: R_{eq} = 2 kΩ NOM
Other inputs: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



description (continued)

STATE AND/OR RATE FUNCTION TABLE (See Note A)

INPUTS										OUTPUTS			
			BINARY RATE							LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	F	E	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	L	L	64	H	L	H	1	C
L	L	L	L	L	L	L	L	H	64	H	1	1	1	C
L	L	L	L	L	L	L	H	L	64	H	2	2	1	C
L	L	L	L	L	L	H	L	L	64	H	4	4	1	C
L	L	L	L	L	H	L	L	L	64	H	8	8	1	C
L	L	L	L	H	L	L	L	L	64	H	16	16	1	C
L	L	L	H	L	L	L	L	L	64	H	32	32	1	C
L	L	L	H	H	H	H	H	H	64	H	63	63	1	C
L	L	L	H	H	H	H	H	H	64	L	H	63	1	D
L	L	L	H	L	H	L	L	L	64	H	40	40	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.

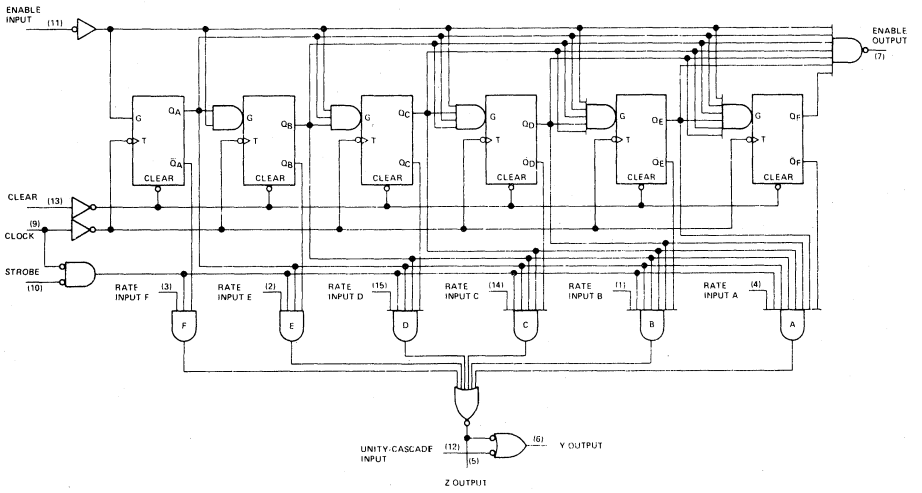
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.

C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.

D. Unity/cascade is used to inhibit output Y.

E. $f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5497 (see Note 2) . . . . . −55°C to 125°C
SN7497 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN5497			SN7494			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Setup time, t_{setup}: (See Figure 1)							
Before positive-going transition of clock pulse	25			25			ns
Before negative-going transition of previous clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	
Hold time, t_{hold}: (See Figure 1)							
After positive-going transition of clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	ns
After negative-going transition of previous clock pulse	20		$t_{cp}-10$	20		$t_{cp}-10$	
Operating free-air temperature, T_A (See Note 2)	−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock input	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
		other inputs					−1.6	
I_{OS}	Short circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, outputs high		V_{CC} = MAX,	See Note 3		58		mA
I_{CCL}	Supply current, outputs low		V_{CC} = MAX,	See Note 4		80	120	mA

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 1. Voltage values are with respet to network ground terminal.
2. An SN5497 in the W package operating at free-air temperatures above 118°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 55°C/W.
3. I_{CCH} is measured with outputs open and all inputs grounded.
4. I_{CCL} is measured with outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETERS¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36*	ns
t_{PHL}		Z			15	23	
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

¶ f_{max} = maximum input clock frequency.
t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

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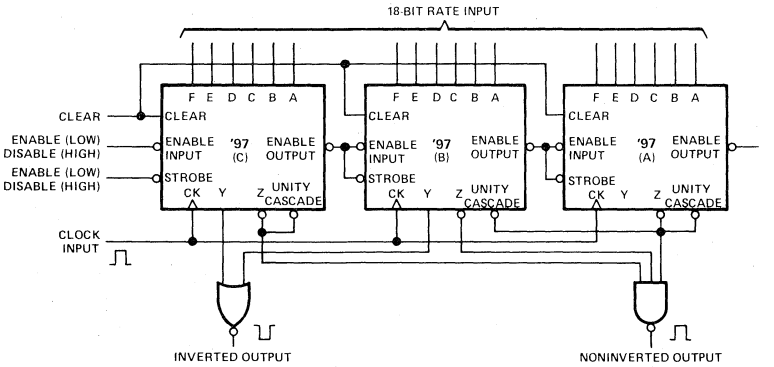
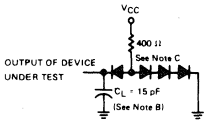
TYPICAL APPLICATION DATA

This application demonstrates how the '97 can be cascaded to perform 18-bit rate multiplication. This scheme is expandable to n-bits by extending the pattern illustrated.



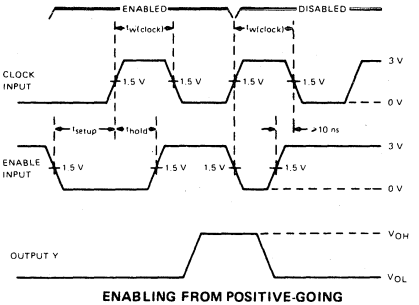
As illustrated, two of the 6-bit multipliers can be cascaded by connecting the Z output of unit A to the unity cascade input of unit B, in which case, a two-input NOR gate is used to cascade the remaining multipliers. Alternatively, all three Y outputs can be cascaded with a 3-input NOR gate. The three unused unity cascade inputs can be conveniently terminated by connecting each to its Z output.

PARAMETER MEASUREMENT INFORMATION

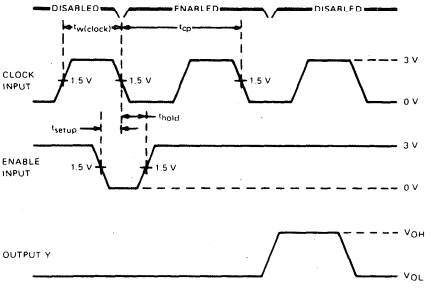


All three outputs are loaded during testing

LOAD CIRCUIT

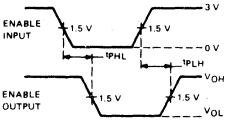


ENABLING FROM POSITIVE-GOING TRANSITION OF CLOCK PULSE



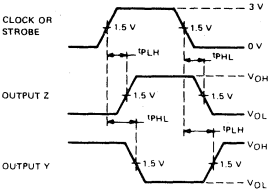
ENABLING FROM NEGATIVE-GOING TRANSITION OF PREVIOUS CLOCK PULSE

1. Unity/Cascade and pin 2 (rate input) are high, other inputs are low. Clear the counter and apply clock and enable pulse as illustrated.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulse (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transition enabled.



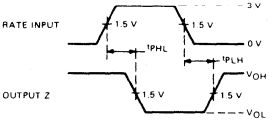
Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT



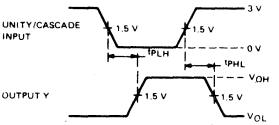
Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y



Flip-flops are at a count so that all other inputs to the gate under test are high and all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y

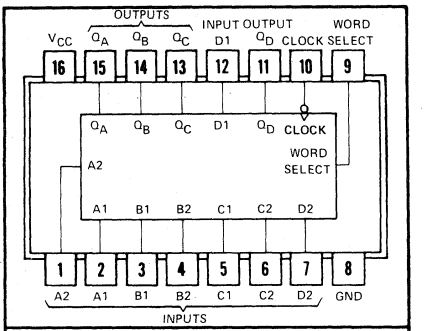
NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)}$ = 20 ns, $t_{TLH} \leq$ 10 ns, $t_{THL} \leq$ 10 ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–SWITCHING TIMES

TYPES SN54L98, SN74L98
4-BIT DATA SELECTORS/STORAGE REGISTERS

BULLETIN NO. DL-S 7211822, DECEMBER 1972

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: word select low for word 1, word select high for word 2, see description

description

These monolithic data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR-INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical power dissipation is 25 mW. The SN54L98 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74L98 is characterized for operation from 0°C to 70°C.

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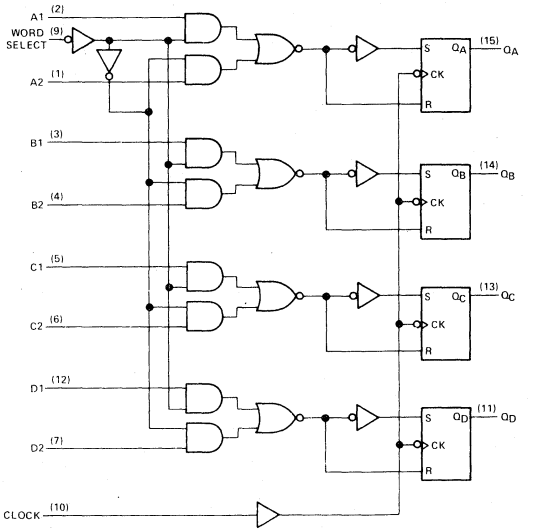
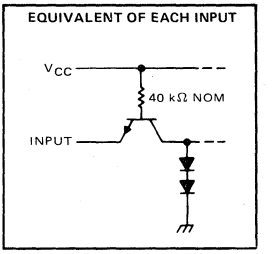
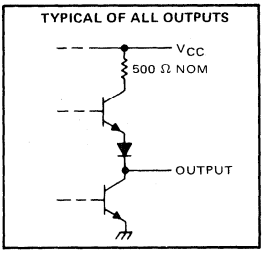
functional block diagram and schematics of inputs and outputs







. . . dynamic input activated by transition from a high level to a low level.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L98 . . . . . −55°C to 125°C
SN74L98 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

		SN54L98			SN74L98			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−100			−200	μA
Low-level output current, I_{OL}				2			3.6	mA
Width of clock pulse, $t_{w(clock)}$		200			200			ns
Setup time for high-level data, $t_{setup(H)}$	at A, B, C, or D	100			100			ns
	at word select	150			150			
Setup time for low-level data, $t_{setup(L)}$	at A, B, C, or D	120			120			ns
	at word select	100			100			
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54L98			SN74L98			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.7 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.7 V,	V_{IH} = 2 V I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			10			10	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.3 V			−0.18			−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−3		−15	−3		−15	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		5	9		5	9	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 4 kΩ, See Note 4	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			125	200	ns

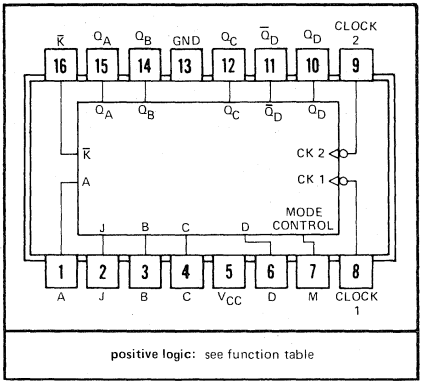
NOTE 4: Load circuit and voltage waveforms are shown on page 149.

TYPES SN54L99, SN74L99
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS

BULLETIN NO. DL-S 7211871, DECEMBER 1972

- N-Bit Serial-to-Parallel Converter
- N-Bit Parallel-to-Serial Converter
- N-Bit Storage Register
- J-$\overline{K}$ Serial Input

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function table

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, mode control, and two clock inputs. The registers have three modes of operation:

Parallel (Broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flop and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on a high-to-low transition of clock 1 when the mode control is low. Serial data for the right-shift mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, a D-type, or T-type flip-flop as shown in the function table. Shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.). Serial data for this mode is entered at the D input. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.

3

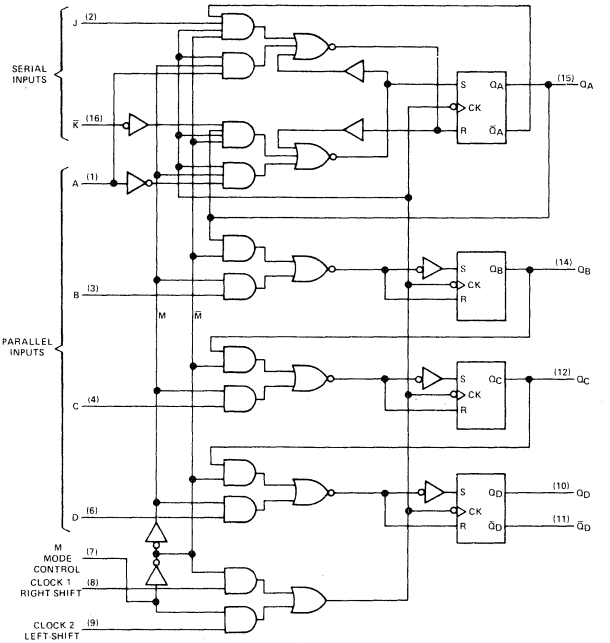
FUNCTION TABLE

INPUTS									OUTPUTS				
MODE	CLOCKS		SERIAL		PARALLEL								
CONTROL	2 (L)	1 (R)	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
H	H	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	↓	X	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	↓	X	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d	$\overline{d}$
L	L	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
L	X	↓	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	X	↓	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	X	↓	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	X	↓	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
↑	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↓	L	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↓	L	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↑	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
↑	H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

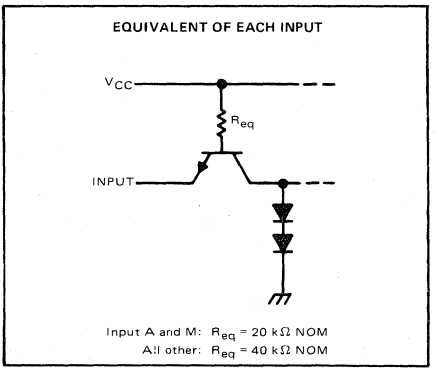
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

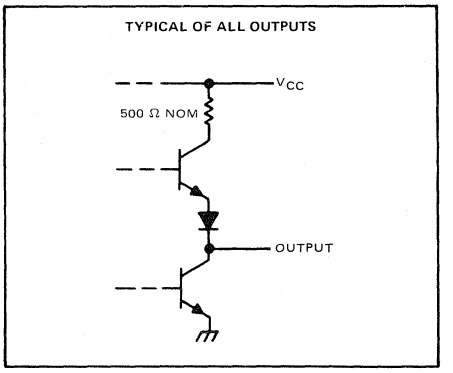
functional block diagram



. . . dynamic input activated by transition from a high level to a low level.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54L99 Circuits . . . . . −55°C to 125°C
SN74L99 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54L99			SN74L99			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Width of clock pulse, $t_{w(clock)}$	200			200			ns
Setup time for high-level data at J, $\overline{K}$, A, B, C, or D inputs, $t_{setup(H)}$	100			100			ns
Setup time for low-level data at J, $\overline{K}$, A, B, C, or D inputs, $t_{setup(L)}$	120			120			ns
Hold time at J, $\overline{K}$, A, B, C, or D inputs, t_{hold}	0			0			ns
Time to enable clock 1, $t_{enable\ 1}$ (see Figure 1)	225			225			ns
Time to enable clock 2, $t_{enable\ 2}$ (see Figure 1)	200			200			ns
Time to inhibit clock 1, $t_{inhibit\ 1}$ (see Figure 1)	100			100			ns
Time to inhibit clock 2, $t_{inhibit\ 2}$ (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54L99			SN74L99			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	J, $\overline{K}$, B, C, or D	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		M or A				200			200	
I_{IH}	High-level input current	J, $\overline{K}$, B, C, or D	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		M or A				20			20	
I_{IL}	Low-level input current	J, $\overline{K}$, B, C, or D	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
		M or A				−0.36			−0.36	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		3.8	9		3.8	9	mA

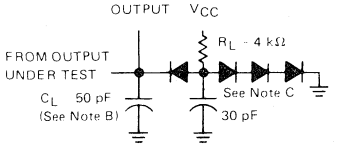
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: With all outputs and J and $\overline{K}$ inputs open, mode control at 4.5 V, inputs A through D grounded, I_{CC} is measured after a momentary 3 V, then ground, is applied to both clock inputs.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

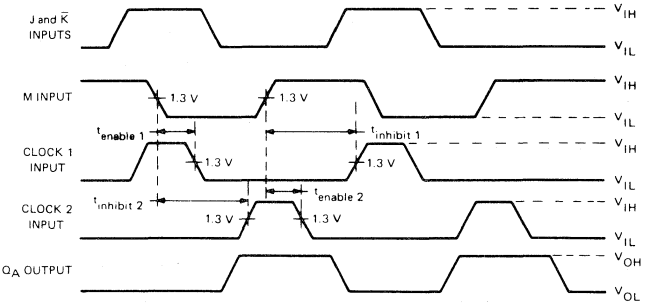
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 4 kΩ, See Figure 2	3	5		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from either clock			115	200	ns
t_{PHL}	Propagation delay time, high-to-low-level output from either clock			125	200	ns

2

PARAMETER MEASUREMENT INFORMATION

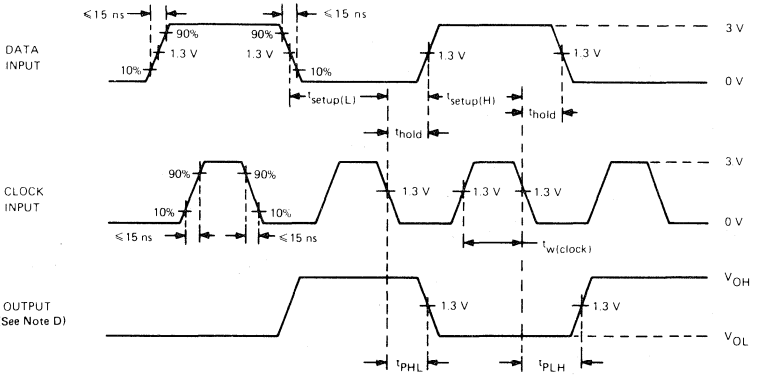


LOAD CIRCUIT



NOTE: A input is at the low level.

VOLTAGE WAVEFORMS
FIGURE 1–CLOCK ENABLE/INHIBIT TIMES



VOLTAGE WAVEFORMS
FIGURE 2–SWITCHING TIMES

NOTES: A. The input waveforms are supplied by pulse generators having the following characteristics: $Z_{out} \approx 50\ \Omega$. For data pulse generator: $t_w \geq 150$ ns, PRR ≤ 500 kHz, $t_{setup(L)} = 120$ ns, and $t_{setup(H)} = 100$ ns. For clock pulse generator: $t_w \geq 200$ ns and PRR ≤ 1 MHz. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916.
D. When data input is applied to J and $\overline{K}$ inputs, the output waveform applies only to output Q_A.

TEXAS INSTRUMENTS

TYPES SN54100, SN74100
8-BIT BISTABLE LATCHES

BULLETIN NO. DL-S 7211830, DECEMBER 1972

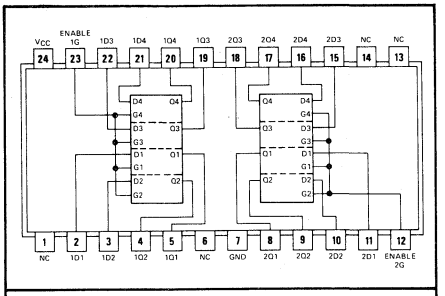
logic

FUNCTION TABLE
(Each Latch)

INPUTS		OUTPUTS	
D	G	Q	$\bar{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level, X = irrelevant
Q_0 = the level of Q before the high-to-low transition of G

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

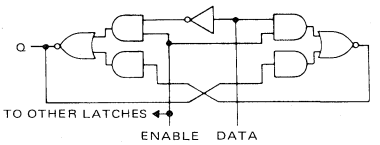
NC—No internal connection

description

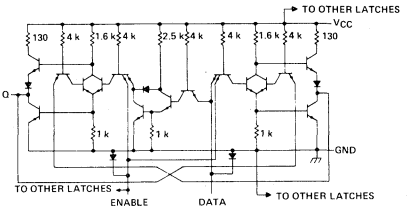
These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable (G) is high and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was setup at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These circuits are completely compatible with all popular TTL or DTL families. All inputs are diode-clamped to minimize transmission-line effects and simplify system design. Typical power dissipation is 40 milliwatts per latch. The SN54100 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74100 is characterized for operation from 0°C to 70°C.

functional block diagram (each latch)



schematic (each latch)



Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Intermitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54100	−55°C to 125°C
SN74100	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For this circuit, this rating applies between the enable and D inputs of any latch.

recommended operating conditions

	SN54100			SN74100			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Width of enabling pulse, t_w	20			20			ns
Setup time, t_{setup}	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		G input					320	
I_{IL}	Low-level input current	D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		G input					−12.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54100	−20		−57	mA
				SN74100	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	SN54100		64	92	mA
				SN74100		64	106	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	D	Q	C_L = 15 pF, R_L = 400 Ω, See Note 4		16	30	ns
t_{PHL}					14	25	
t_{PLH}	G	Q			16	30	ns
t_{PHL}					7	15	

¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

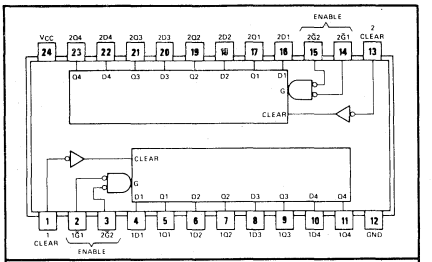
NOTE 4: Test circuit and voltage waveforms are the same as those shown for the '75, '77, 'L75, and 'L77 on page 186.

TYPES SN54116, SN74116
DUAL 4-BIT LATCHES WITH CLEAR

BULLETIN NO. DL-S 7211849, DECEMBER 1972

- Two Independent 4-Bit Latches in a Single Package
- Separate Clear Inputs Provide One-Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading and Register Implementations
- Compatible for Use with TTL and DTL Circuits
- Input Clamping Diodes Simplify System Design

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These monolithic TTL circuits utilize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

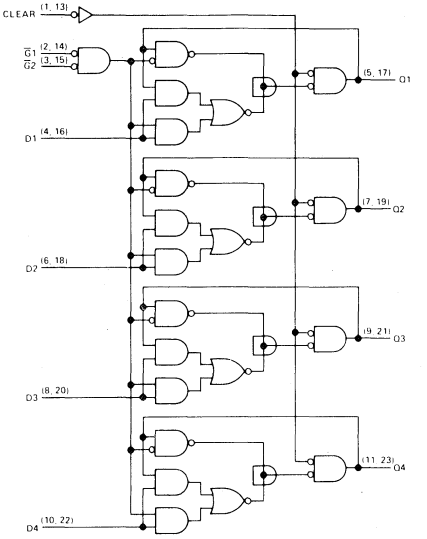
The SN54116 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74116 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS				OUTPUT
CLEAR	ENABLE $\overline{G1}$	ENABLE $\overline{G2}$	DATA	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before these input conditions were established.

functional block diagram (each 4-bit latch)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54116 Circuits . . . . . −55°C to 125°C
SN74116 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54116			SN74116			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Input pulse width, t_w	Enable	18			18			ns
	Clear	18			18			
Data setup time, t_{setup}	High logic level	8			8			ns
	Low logic level	14			14			
Clear inactive-state setup time, t_{setup}		8			8			ns
Data release time, high-level data, $t_{release}$				2			2	ns
Data hold time, low-level data, t_{hold}		8			8			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Any D					60	
I_{IL}	Low-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Any D, initial peak					−2.4	
		Any D, steady-state					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54116	−20		−57	mA
				SN74116	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition A		60	100	mA
				Condition B		40	70	

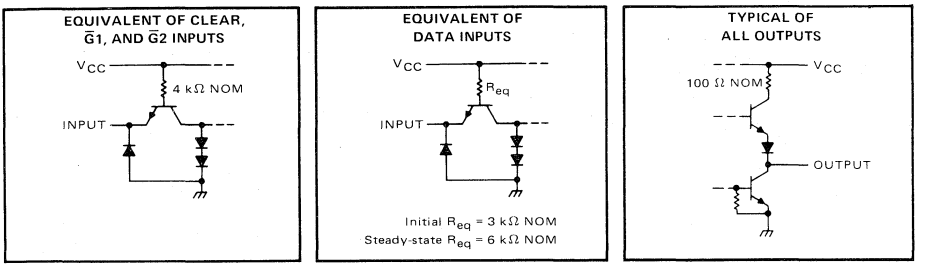
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With outputs open, I_{CC} is measured for the following conditions:
A. All inputs grounded.
B. All $\overline{G}$ inputs are grounded and all other inputs are at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

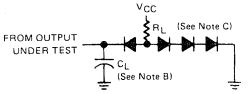
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		19	30	ns
t_{PHL}					15	22	
t_{PLH}	Data	Q			10	15	ns
t_{PHL}					12	18	
t_{PHL}	Clear	Any Q			15	22	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

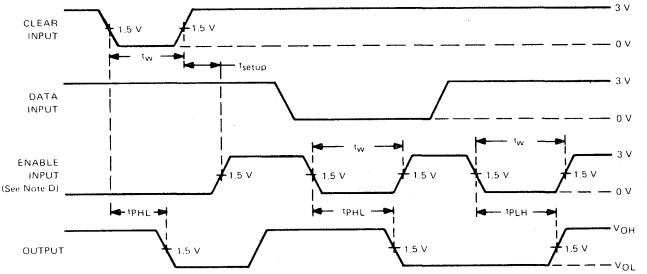
schematics of inputs and outputs



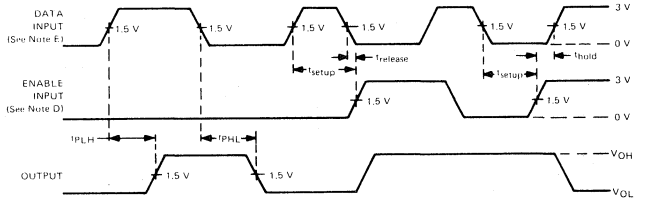
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



SWITCHING TIMES FROM CLEAR AND ENABLE INPUTS



SWITCHING TIMES FROM DATA INPUTS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR = 1 MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. The other enable input is low.
E. Clear input is high.

FIGURE 1

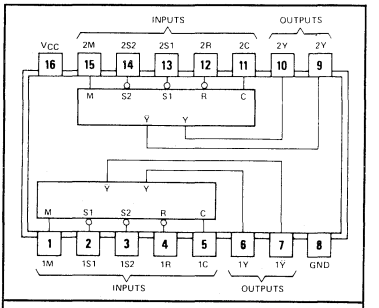
TYPES SN54120, SN74120
DUAL PULSE SYNCHRONIZERS/DRIVERS

BULLETIN NO. DL-S 7211537, SEPTEMBER 1971—REVISED DECEMBER 1972

- Generates Either a Single Pulse or Train of Pulses Synchronized with Control Functions
- Ideal for Implementing Sync-Control Circuits Similar to those Used in Oscilloscopes
- Latched Operation Ensures that Output Pulses Are Not Clipped
- High-Fan-Out Complementary Outputs Drive System Clock Lines Directly
- Internal Input Pull-Up Resistors Eliminate Need for External Components
- Diode-Clamped Inputs Simplify System Design
- Typical Propagation Delays:

  9 Nanoseconds through One Level
  16 Nanoseconds through Two Levels

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



logic: see description and function table

description

These monolithic pulse synchronizers are designed to synchronize an asynchronous or manual signal with a system clock. Reliable response is ensured as the input signals are latched up; therefore duration of logic input is not critical and the adverse effects of contact-bounce of a manual input are eliminated. The ability to pass output pulses is started and stopped by the levels or pulses applied to the latch inputs S1, S2, or R in accordance with the function table. High-speed circuitry is utilized throughout the clock paths to minimize skew with respect to the system clock.

After initiation, the mode control (M) input determines whether a series of pulses or only one pulse is passed. In the absence of a stop command, the clock driver will continue to pass clock pulses as long as the mode control input is low (see Figures 2 through 4). If the mode control input is high only a single clock pulse will be passed (see Figure 5).

When the mode control is set to pass a series of pulses, the last pulse out is determined by two general rules:

a. When pulses are terminated by the S or R inputs, conditions meeting the setup times (specified under recommended operating conditions) will dominate.

FUNCTION TABLE

INPUTS			FUNCTION
R	S1	S2	
X	L	X	Pass Output Pulses
X	X	L	Pass Output Pulses
L	H	H	Inhibit Output Pulses
H	↓	H	Start Output Pulses
H	H	↓	Start Output Pulses
↓	H	H	Stop Output Pulses
H	H	H	Continue†

H = high level (steady state)
L = low level (steady state)
↓ = transition from H to L
X = irrelevant
†Operation initiated by last ↓ transition continues.

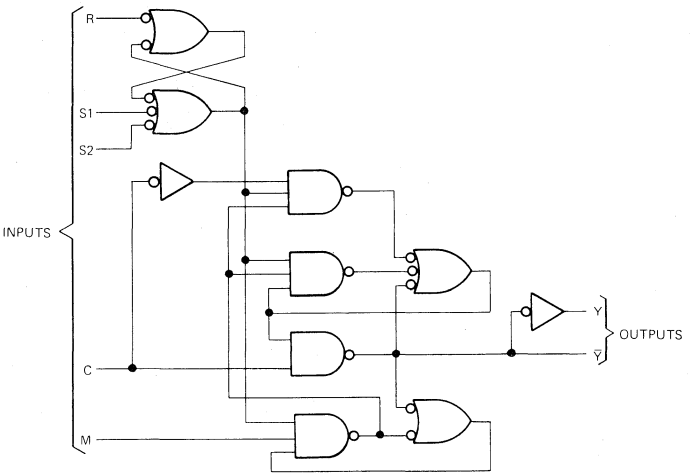
b. Low-to-high-level transitions at the mode control input should be avoided during the 20-nanosecond period immediately following the negative transition of the input clock pulse as transitions during this time period may or may not allow the next pulse to pass (see Figures 4 and 5). When pulses are terminated by the mode control input, a positive transition at the mode control input meeting the high-level setup time, $t_{setup(H)}$, (specified under recommended operating conditions) will pass that positive clock pulse then inhibit remaining clock pulses. The clock input (C) is latch-controlled ensuring that once initiated the output pulse will not be terminated until the full pulse has been passed.

description (continued)

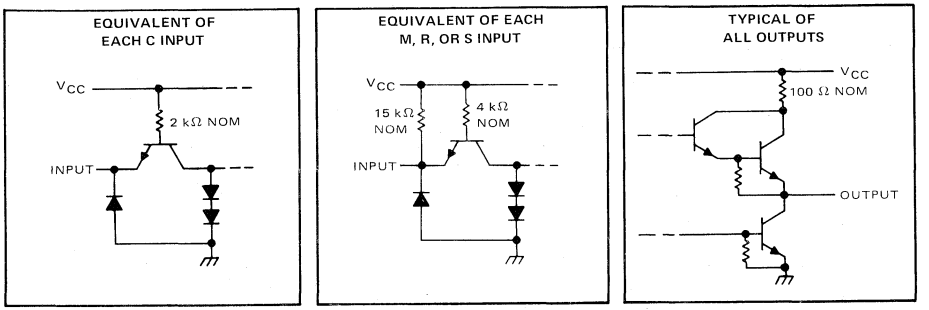
This clock driver circuit is entirely compatible for use with either digital logic circuits or mechanical switches for input controls since all inputs, except the clock, have internal pull-up resistors. This eliminates the requirement to supply an external resistor to prevent the input from floating when the control switch is open. The internal resistor also means that these inputs may be left disconnected if unused.

Typical propagation delay time is 9 nanoseconds to the $\overline{Y}$ output and 16 nanoseconds to the Y output from the clock input. The outputs will drive 60 Series 54/74 loads at a high logic level and 30 loads at a low logic level. Typical power dissipation is 127 milliwatts per driver. The SN54120 is characterized for operation from −55°C to 125°C; the SN74120 is characterized for operation from 0°C to 70°C.

functional block diagram (each driver)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54120 Circuits . . . . . −55°C to 125°C
SN74120 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the S1 and S2 inputs.

recommended operating conditions

			SN54120			SN74120			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}					−2.4			−2.4	mA
Low-level output current, I_{OL}					48			48	mA
Setup time (see Figures 2 thru 5)	Any input except mode control, $t_{setup(H\text{ or }L)}$		12			12			ns
	Mode control	$t_{setup(H)}$	0			0			
		$t_{setup(L)}$	12			12			
Hold time (see Figures 3 and 5)	Any input except mode control, $t_{hold(H\text{ or }L)}$		3			3			ns
	Mode control, $t_{hold(H\text{ or }L)}$		20			20			
Operating free-air temperature, T_A			−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −2.4 mA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 48 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	Clock input	V_{CC} = MAX, V_I = 2.4 V			80	μA
		Other inputs		−0.12	−0.2	−0.36	mA
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX, V_I = 0.4 V			−3.2	mA
		Other inputs				−2.1	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−35		−90	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		51	90	mA

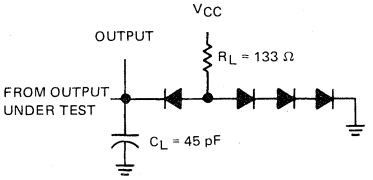
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with ground applied to all inputs except R which is at 4.5 V and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C	Y	C_L = 45 pF, R_L = 133 Ω, See Figure 1		14	22	ns
t_{PHL}					17	25	
t_{PLH}	C	$\overline{Y}$			10	16	ns
t_{PHL}					8	13	

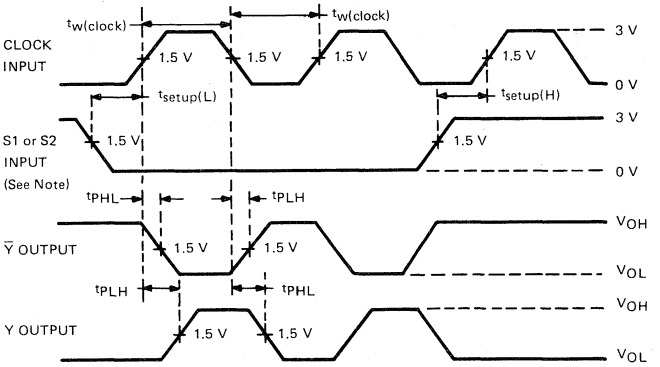
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



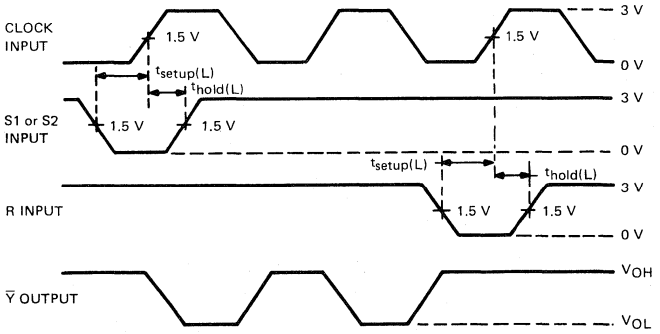
NOTES: A. The clock input pulse in figures 2 through 5 is supplied by a generator having the following characteristics: $t_{w(clock)} \geq 15$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1–LOAD CIRCUIT FOR SWITCHING TESTS



NOTE: Mode control and R inputs are low unused S input is high.

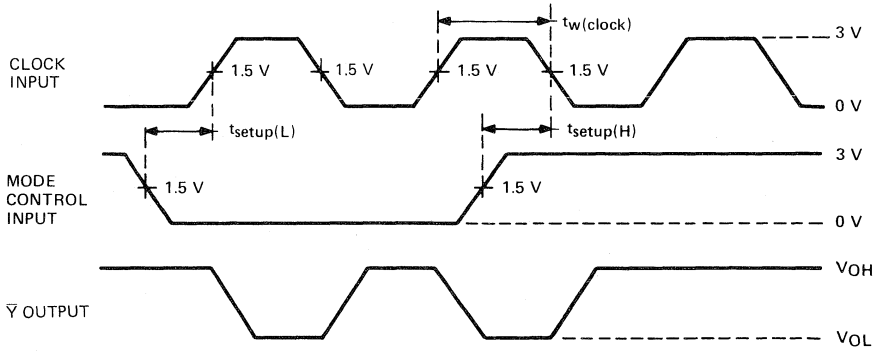
FIGURE 2–INITIATING AND TERMINATING PULSE TRAIN FROM S INPUTS



NOTE: Mode control input is low and unused S input is high.

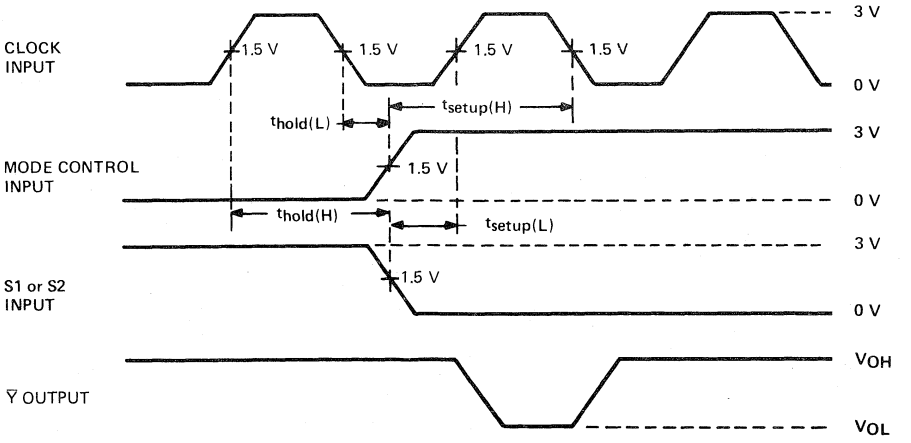
FIGURE 3–INITIATING PULSE TRAIN FROM S AND TERMINATING WITH R INPUTS

PARAMETER MEASUREMENT INFORMATION



NOTE: At least one of the S inputs is low.

FIGURE 4–INITIATING AND TERMINATING PULSE TRAIN WITH MODE CONTROL INPUT



NOTE: Input R and the unused S are high.

FIGURE 5–ENABLING SINGLE PULSE

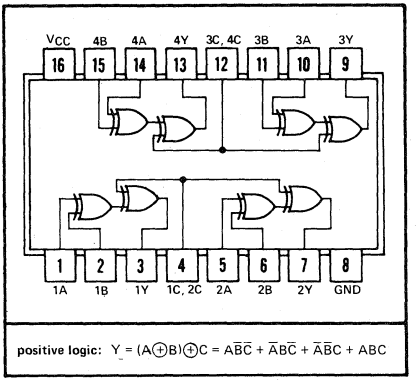
TEXAS INSTRUMENTS

TYPES SN54S135, SN74S135
QUADRUPLE EXCLUSIVE-OR/NOR GATES

BULLETIN NO. DL-S 7211826, DECEMBER 1972

- Fully Compatible with Most TTL and TTL MSI Circuits
- Fully Schottky Clamping Reduces Delay Times . . . 8 ns Typical
- Can Operate as Exclusive-OR Gate (C Input Low) or as Exclusive-NOR Gate (C Input High)

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $Y = (A \oplus B) \oplus C = A\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + ABC$

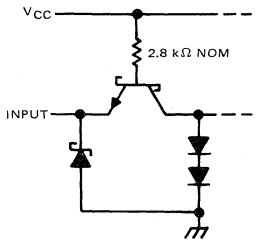
FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

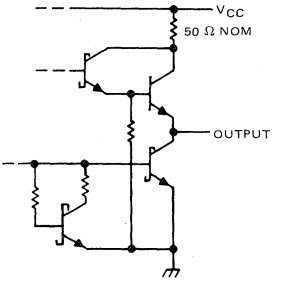
H = high level, L = low level

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S135 . . . . . −55°C to 125°C
SN74S135 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S135			SN74S135			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			65	99	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the inputs grounded and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

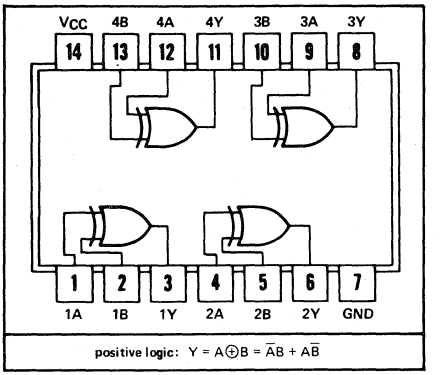
PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	B or A = L, C = L	C_L = 15 pF, R_L = 280 Ω, See Note 3		8.5	13	ns
t_{PHL}					11	15	
t_{PLH}	A or B	B or A = H, C = L			8	12	ns
t_{PHL}					9	13.5	
t_{PLH}	A or B	B or A = L, C = H			10	15	ns
t_{PHL}					6.5	10	
t_{PLH}	A or B	B or A = H, C = H			8.5	12	ns
t_{PHL}					7	11	
t_{PLH}	C	A = B			8	12	ns
t_{PHL}					9.5	14.5	
t_{PLH}	C	A ≠ B			7.5	11.5	ns
t_{PHL}					8	12	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54136, SN54LS136, SN74136, SN74LS136
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES
WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7211827, DECEMBER 1972

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $Y = A \oplus B = \overline{A}B + A\overline{B}$

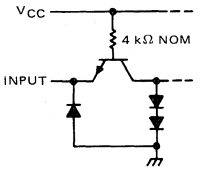
FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

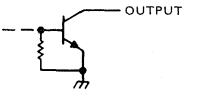
H = high level, L = low level

schematics of inputs and outputs

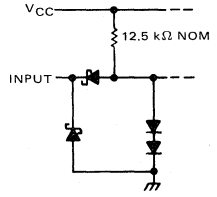
EQUIVALENT OF EACH INPUT
OF '136



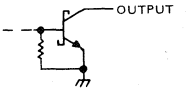
TYPICAL OF ALL OUTPUTS
OF '136



EQUIVALENT OF EACH INPUT
OF 'LS136



TYPICAL OF ALL OUTPUTS
OF 'LS136



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54136 . . . . . −55°C to 125°C
SN74136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54136			SN74136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −8 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current, high-level output	V_{CC} = MAX, See Note 2		SN54136		30	43	mA
				SN74136		30	50	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 400 Ω, See Note 3		12	18	ns
t_{PHL}					39	50	
t_{PLH}	A or B	Other input high			14	22	ns
t_{PHL}					42	55	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS136 . . . . . −55°C to 125°C
SN74LS136 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS136			SN74LS136			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS136			SN74LS136			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.6			−0.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		6.1	10		6.1	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 3		18	30	ns
t_{PHL}					18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 149.

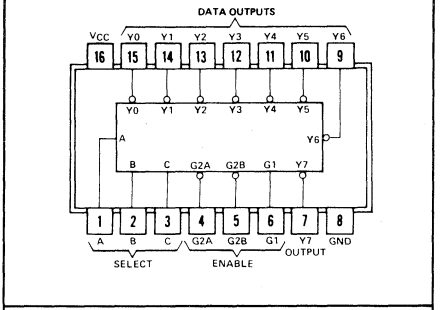
TYPES SN54LS138, SN54LS139, SN54S138, SN54S139, SN74LS138, SN74LS139, SN74S138, SN74S139 DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7211804, DECEMBER 1972

- Designed Specifically for High-Speed:
  Memory Decoders
  Data Transmission Systems
- 'S138 and 'LS138 3-to-8-Line Decoders Incorporate 3 Enable Inputs to Simplify Cascading and/or Data Reception
- 'S139 and 'LS139 Contain Two Fully Independent 2-to-4-Line Decoders/ Demultiplexers
- Schottky Calmped for High Performance

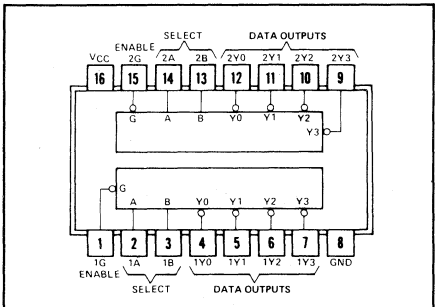
TYPE	TYPICAL PROPAGATION DELAY (3 LEVELS OF LOGIC)	TYPICAL POWER DISSIPATION
'LS138	22 ns	32 mW
'S138	8 ns	245 mW
'LS139	22 ns	34 mW
'S139	7.5 ns	300 mW

'LS138, 'S138
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

'LS139, 'S139
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These Schottky-clamped TTL MSI circuits are designed to be used in high-performance memory-decoding or data-routing applications requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When employed with high-speed memories utilizing a fast-enable circuit the delay times of these decoders and the enable time of the memory are usually less than the typical access time of the memory. This means that the effective system delay introduced by the Schottky-clamped system decoder is negligible.

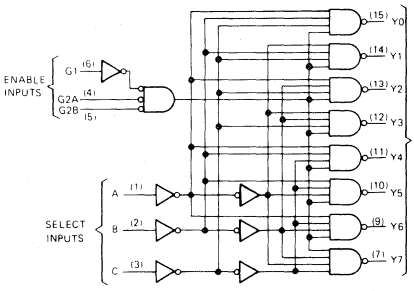
The 'LS138 and 'S138 decode one-of-eight lines dependent on the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented without external inverters and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The 'LS139 and 'S139 comprise two individual two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs each of which represents only one normalized Series 54LS/74LS load ('LS138, 'LS139) or one normalized Series 54S/74S load ('S138, 'S139) to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design. Series 54LS and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74LS and 74S devices are characterized for 0°C to 70°C industrial systems.

functional block diagrams and logic

'LS138, 'S138

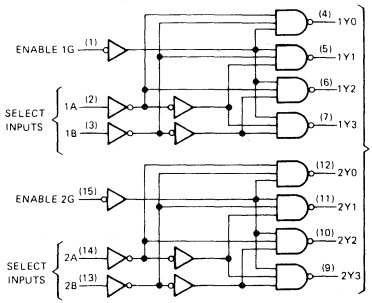


'LS138, 'S138
FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

'LS139, 'S139



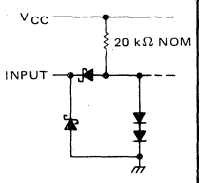
'LS139, 'S139
(EACH DECODER/DEMULTIPLEXER)
FUNCTION TABLE

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

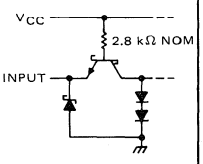
H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

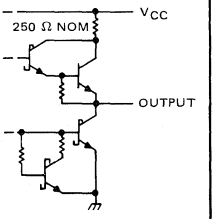
EQUIVALENT OF EACH INPUT OF 'LS138, 'LS139



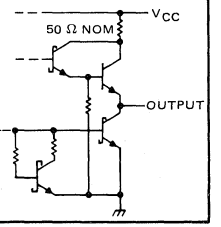
EQUIVALENT OF EACH INPUT OF 'S138, 'S139



TYPICAL OF OUTPUTS OF 'LS138, 'LS139



TYPICAL OF OUTPUTS OF 'S138, 'S139



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS138, SN54LS139 Circuits . . . . . −55°C to 125°C
SN74LS138, SN74LS139 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS138 SN54LS139			SN74LS138 SN74LS139			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS138 SN54LS139			SN74LS138 SN74LS139			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.36			−0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs enabled and open	'LS138		6.3	10		6.3	10	mA
			'LS139		6.8	11		6.8	11	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54LS138 SN74LS138			SN54LS139 SN74LS139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary Select	Any	2	C_L = 15 pF, R_L = 2 kΩ, See Note 2		13	20		13	20	ns
t_{PHL}						27	41		22	33	ns
t_{PLH}			3			18	27		18	29	ns
t_{PHL}						26	39		25	38	ns
t_{PLH}	Enable	Any	2			12	18		16	24	ns
t_{PHL}						21	32		21	32	ns
t_{PLH}			3			17	26				ns
t_{PHL}						25	38				ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 2: Load circuits and waveforms are shown on page 149.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S138, SN54S139 Circuits . . . . . −55°C to 125°C
SN74S138, SN74S139 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S138 SN74S139			SN74S138 SN74S139			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		SN54S138 SN74S138			SN54S139 SN74S139			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_I Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH} High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		2.5	3.4		V
		SN74S'	2.7	3.4		2.7	3.4		
V_{OL} Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH} High-level input current	V_{CC} = MAX, V_I = 2.7 V				50			50	μA
I_{IL} Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2			−2	mA
I_{OS} Short-circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC} Supply current	V_{CC} = MAX, Outputs enabled and open			49	74		60	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF DELAY	TEST CONDITIONS	SN54S138, SN74S138			SN54S139 SN74S139			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Binary select	Any	2	C_L = 15 pF, R_L = 280 Ω, See Note 3		4.5	7		5	7.5	ns
t_{PHL}						7	10.5		6.5	10	
t_{PLH}			3			7.5	12		7	12	ns
t_{PHL}						8	12		8	12	
t_{PLH}	Enable	Any	2			5	8		5	8	ns
t_{PHL}						7	11		6.5	10	
t_{PLH}			3			7	11				ns
t_{PHL}						7	11				

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

NOTE 3: Load circuits and waveforms are shown on page 148.

TYPE SN74141
BCD-TO-DECIMAL DECODER/DRIVER

BULLETIN NO. DL-S 7211801, DECEMBER 1972

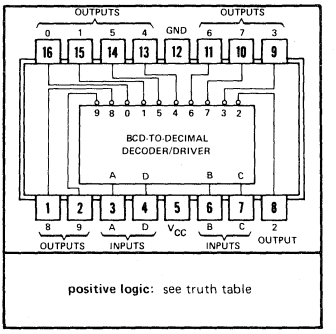
- Drives gas-filled cold-cathode indicator tubes directly
- Fully decoded inputs ensure all outputs are off for invalid codes
- Input clamping diodes minimize transmission-line effects

FUNCTION TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level
† All other outputs are off

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



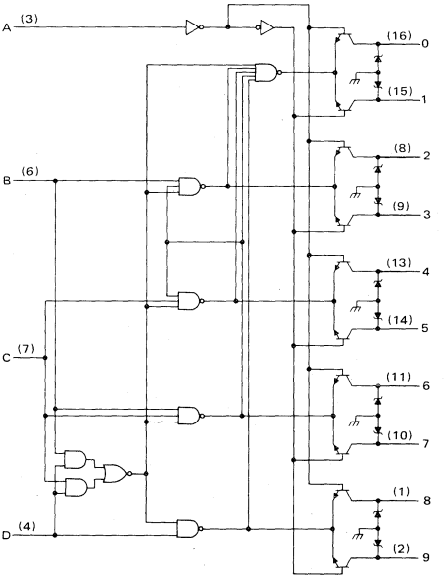
description

The SN74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 80 milliwatts. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Current into any output (off-state) . . . . . 2 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Off-state output voltage			60	V
Operating free-air temperature, T_A	0		70	°C

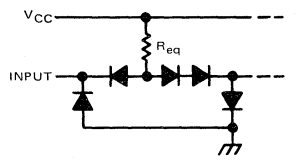
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −5 mA			−1.5	V
$V_{O(on)}$	On-state output voltage		V_{CC} = MIN,	I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9		V_{CC} = MAX,	I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state reverse current		V_{CC} = MAX,	V_O = 55 V			50	µA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15		V_{CC} = MAX, V_O = 30 V	T_A = 55°C			5	µA
				T_A = 70°C			15	
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	A input	V_{CC} = MAX,	V_I = 2.4 V			40	µA
		B, C, or D input					80	
I_{IL}	Low-level input current	A input	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		B, C, or D input					−3.2	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 2		16	25	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This typical value is at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

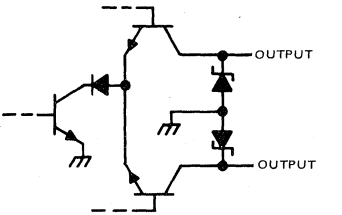
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Input A: R_{eq} = 6 kΩ NOM
Inputs B, C, D: R_{eq} = 2 kΩ NOM

TYPICAL OF ALL OUTPUTS



TYPE SN74142
BCD COUNTER/4-BIT LATCH/BCD DECODER/DRIVER

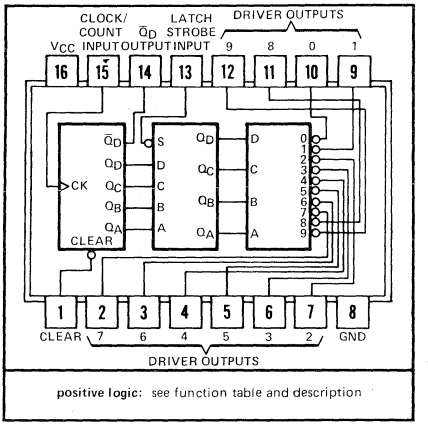
BULLETIN NO. DL-S 7211719, MAY 1972—REVISED DECEMBER 1972

FUNCTION TABLE

INPUTS			OUTPUTS	
COUNT PULSE (CLOCK)	CLEAR	LATCH STROBE	ON†	$\overline{Q}_D$
X	L	L	0	H
1	H	L	1	H
2	H	L	2	H
3	H	L	3	H
4	H	L	4	H
5	H	L	5	H
6	H	L	6	H
7	H	L	7	H
8	H	L	8	L
9	H	L	9	L
10	H	L	0	H
11	H	H	0	H

†All other outputs are off.
H = high level, L = low level, X = irrelevant

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see function table and description

description

The SN74142 contains a divide-by-ten (BCD) counter, a four-bit latch, and a decoder/*Nixie*‡ tube driver on a monolithic chip and is packaged in popular 16-pin packages. This single MSI function can replace the equivalent of three separately packaged MSI circuits to reduce printed-circuit board area and the number of system interconnections, resulting in reduced costs and improved reliability.

Four master-slave flip-flops are fully decoded to provide a divide-by-ten counter. A direct clear input will, when taken low, reset and hold the counter at zero (all Q outputs low, $\overline{Q}_D$ output high). While the clear input is inactive (high), each positive-going transition of the clock will increment the counter. The $\overline{Q}_D$ output is made available externally for cascading to n-bit counters.

The Q outputs of the counter are routed to the data inputs of the four-bit latch. While the latch strobe input is low, the internal latch outputs will follow the respective Q outputs of the counter. When the latch strobe input is taken high, the latch stores the data which has been setup by the counter outputs prior to the low-to-high level transition of the latch strobe input. The $\overline{Q}_D$ output from the counter is not stored by the latch since it is intended for clocking the next counter stage. This means that the system counter can continuously acquire new data. Since all outputs of the latch and Q outputs of the counter drive low-capacitance on-chip loads, the circuitry is considerably simplified with respect to the number of components required. This results in a highly efficient function which typically reduces power requirements 15% when compared to systems using the three separate packages.

The SN74142 counter/latch/driver features fully buffered inputs to reduce drive requirements to one normalized Series 74 load per input, and diode-clamping of all inputs to minimize transmission line effects. The counter will accept input clock frequencies up to 20 MHz and is entirely compatible for use with all popular TTL and DTL logic circuits. The high-performance n-p-n driver outputs are identical to the SN74141 and have a maximum off-state reverse current of 50 microamperes at 55 volts.

‡*Nixie* is a registered trademark of the Burroughs Corporation.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state current into outputs 0 thru 9 . . . . . 1 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: All voltage values are with respect to the network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current from $\overline{Q}_D$, I_{OH}				−400	μA
Low-level output current from $\overline{Q}_D$, I_{OL}				8	mA
Input clock frequency, f_{clock}		0		20	MHz
Clock pulse width, $t_{w(clock)}$ (see Figure 1)	High logic level	15			ns
	Low logic level	35			
Clear pulse width, $t_{w(clear)}$ (see Figure 1)		25			ns
Strobe pulse width, $t_{w(strobe)}$ (see Figure 1)		20			ns
Clear inactive-state setup time, t_{setup} (see Figure 1)		15			ns
Strobe time, t_{strobe} (see Figure 1)		45		$t_{w(clock)}$ +10	ns
Operating free-air temperature, T_A		0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

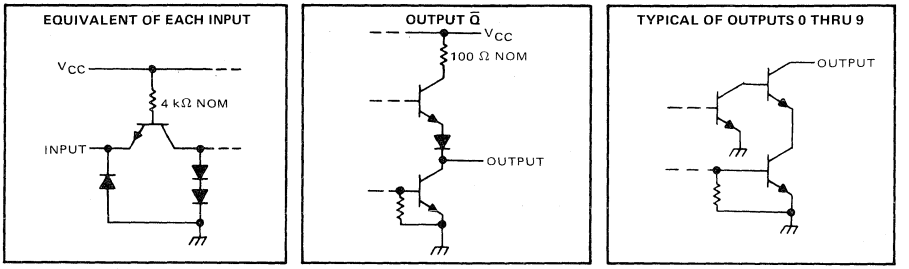
PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level $\overline{Q}_D$ output voltage	V_{CC} = MIN, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level $\overline{Q}_D$ output voltage	V_{CC} = MIN, I_{OL} = 8 mA		0.2	0.4	V
$V_{O(on)}$	On-state voltage, outputs 0 thru 9	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state voltage, outputs 0 thru 9	V_{CC} = MAX, I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state current, outputs 0 thru 9	V_{CC} = MAX, V_O = 55 V			50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit $\overline{Q}_D$ output current	V_{CC} = MAX	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open		68	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

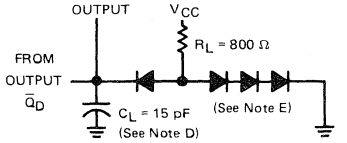
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}_D$ output from clock	C_L = 15 pF, R_L = 800 Ω, See Figure 1		35	55	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}_D$ output from clock			30	45	
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}_D$ output from clear			30	45	ns

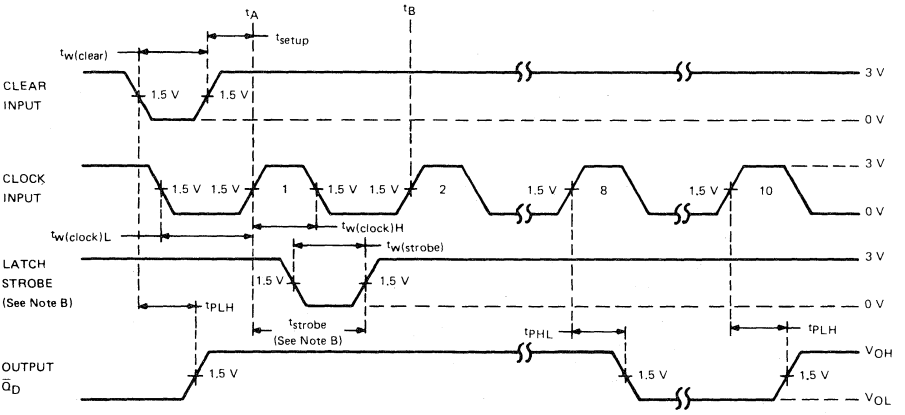
schematics of inputs and outputs



PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. This typical abbreviated sequence illustrates clearing from count 8 or 9 and counting through ten clock pulses. Clock pulses 3 through 7 and 9 are omitted for brevity.

B. Strobe input can go low at any time; however, the positive transition to store data from any given clock transition (t_A) must occur a minimum of 45 ns after t_A and prior to 10 ns after the next positive-going clock transition (t_B + 10 ns).

C. Input pulses are supplied by generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.

D. C_L includes probe and jig capacitance.

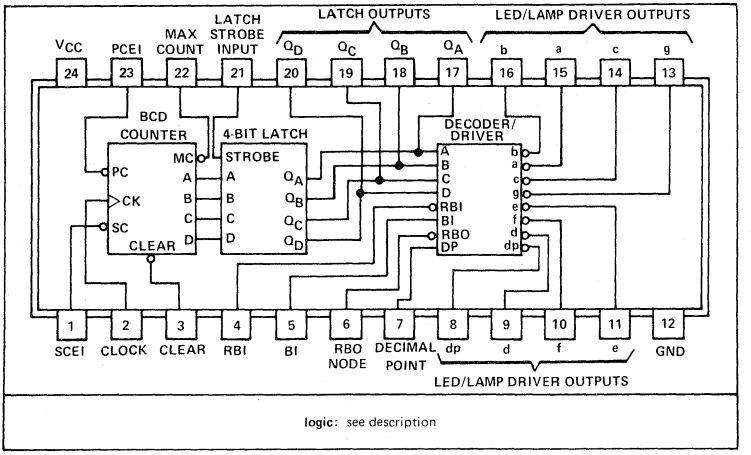
E. All diodes are 1N3064.

FIGURE 1

TYPES SN54143, SN54144, SN74143, SN74144
4-BIT COUNTER/LATCH, SEVEN-SEGMENT LED/LAMP DRIVERS

BULLETIN NO. DL-S 7211538, NOVEMBER 1971–REVISED DECEMBER 1972

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



logic: see description

- **Choice of Driver Outputs:**

  SN54143 and SN74143 have 15-mA Constant-Current Outputs for Driving Common-Anode LED's such as TIL302 or TIL303 without Series Resistors

  SN54144 and SN74144 Drive High-Current Lamps, Numitrons†, or LED's from Saturated Open-Collector Outputs

- **Universal Logic Capabilities**

  Ripple Blanking of Extraneous Zeros
  Latch Outputs Can Drive Logic Processors Simultaneously
  Decimal Point Driver Is Included

- **Synchronous BCD Counter Capability Includes:**

  Cascadable to N-Bits
  Look-Ahead-Enable Techniques Minimize Speed Degradation When Cascaded for Large-Word Display
  Direct Clear Input

description

These TTL MSI circuits contain the equivalent of 86 gates on a single chip. Logic inputs and outputs are completely TTL/DTL compatible. The buffered inputs are implemented with relatively large resistors in series with the bases of the input transistors to lower drive-current requirements to one-half of that required for a standard Series 54/74 TTL input. The serial-count-enable, actually two internal emitters, is rated as one standard series 54/74 load. The logic outputs, except RBO, have active pull-ups.

The SN54143 and SN74143 driver outputs are designed specifically to maintain a relatively constant on-level sink current of approximately 15 milliamperes from outputs "a" through "g" and seven milliamperes from output "dp" over a voltage range from one to five volts. Any number of LED's in series may be driven as long as the output voltage rating is not exceeded.

†Trademark of RCA

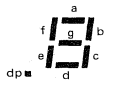
description (continued)

The SN54144 and SN74144 drivers have high-sink-current saturated outputs for driving indicators having voltage ratings up to 15 volts or requiring up to 25 milliamperes drive. The SN54144 sinks 20 milliamperes and the SN74144 sinks 25 milliamperes at an on-level voltage of 0.6 volts across their respective operating temperature ranges.

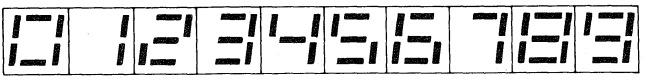
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Maximum clock frequency is typically 18 megahertz and power dissipation is typically 280 milliwatts. The SN54143 and SN54144 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74143 and SN74144 are characterized for operation from 0°C to 70°C.

Functions of the inputs and outputs of these devices are as follows:

FUNCTION	PIN NO	DESCRIPTION
CLEAR INPUT	3	When low, resets and holds counter at 0. Must be high for normal counting.
CLOCK INPUT	2	Each positive-going transition will increment the counter provided that the circuit is in the normal counting mode (serial and parallel count enable inputs low, clear input high).
PARALLEL COUNT ENABLE INPUT (PCEI)	23	Must be low for normal counting mode. When high, counter will be inhibited. Logic level must not be changed when the clock is low.
SERIAL COUNT ENABLE INPUT (SCEI)	1	Must be low for normal counting mode, also must be low to enable maximum count output to go low. When high, counter will be inhibited and maximum count output will be driven high. Logic level must not be changed when the clock is low.
MAXIMUM COUNT OUTPUT	22	Will go low when the counter is at 9 and serial count enable input is low. Will return high when the counter changes to 0 and will remain high during counts 1 through 8. Will remain high (inhibited) as long as serial count enable input is high.
LATCH STROBE INPUT	21	When low, data in latches follow the data in the counter. When high, the data in the latches are held constant, and the counter may be operated independently.
LATCH OUTPUTS (Q_A, Q_B, Q_C, Q_D)	17, 18, 19, 20	The BCD data that drives the decoder can be stored in the 4-bit latch and is available at these outputs for driving other logic and/or processors. The binary weights of the outputs are: $Q_A = 1$, $Q_B = 2$, $Q_C = 4$, $Q_D = 8$.
DECIMAL POINT INPUT	7	Must be high to display decimal point. The decimal point is not displayed when this input is low or when the display is blanked.
BLANKING INPUT (BI)	5	When high, will blank (turn off) the entire display and force RBO low. Must be low for normal display. May be pulsed to implement intensity control of the display.
RIPPLE-BLANKING INPUT (RBI)	4	When the data in the latches is BCD 0, a low input will blank the entire display and force the RBO low. This input has no effect if the data in the latches is other than 0.
RIPPLE-BLANKING OUTPUT (RBO)	6	Supplies ripple blanking information for the ripple blanking input of the next decade. Provides a low if BI is high, or if RBI is low and the data in the latches in BCD 0; otherwise, this output is high. This pin has a resistive pull-up circuit suitable for performing a wire-AND function with any open-collector output. Whenever this pin is low the entire display will be blanked; therefore, this pin may be used as an active-low blanking input.
LED/LAMP DRIVER OUTPUTS (a, b, c, d, e, f, g, dp)	15, 16, 14, 9 11, 10, 13, 8	Outputs for driving seven-segment LED's or lamps and their decimal points. See segment identification and resultant displays on following page.



SEGMENT IDENTIFICATION

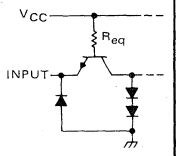


NUMERICAL DESIGNATIONS—RESULTANT DISPLAYS

schematics of inputs and outputs

'143, '144

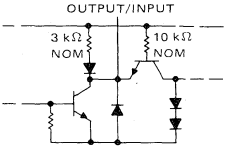
EQUIVALENT OF EACH INPUT EXCEPT BI/RBO



SCE1: R_{eq} = 4 kΩ NOM
Other inputs: R_{eq} = 8 kΩ NOM

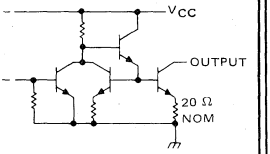
'143, '144

EQUIVALENT OF BI/RBO



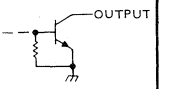
'143

TYPICAL OF ALL OUTPUTS EXCEPT BI/RBO



'144

TYPICAL OF ALL OUTPUTS EXCEPT BI/RBO



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state voltage at outputs "a" thru "g" and "dp", '144 . . . . . 15 V
Off-state current at outputs "a" thru "g" and "dp", '143 . . . . . 250 μA
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 2) . . . . . 1.4 W
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For the SN54143 and SN54144 in the N and W packages, this rating applies at (or below) 80°C free-air temperature. For operation above this temperature, derate linearly at the rate of 11.7 mW/°C for the W package and 14.7 mW/°C for the N package. No derating is required for these devices in the J package.

recommended operating conditions

		SN54143, SN54144			SN74143, SN74144			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
On-state voltage at outputs a thru g and dp ('143 only)		1		5	1		5	V
High-level output current, I_{OH}	Q_A, Q_B, Q_C, Q_D			−240			−240	μA
	Maximum count			−560			−560	
	RBO			−120			−120	
Low-level output current, I_{OL}	Q_A, Q_B, Q_C, Q_D, RBO			4.8			4.8	mA
	Maximum count			11.2			11.2	
Clock pulse width, $t_{w(clock)}$	High logic level	25			25			ns
	Low logic level	55			55			
Clear pulse width, $t_{w(clear)}$		25			25			ns
Setup time, t_{setup}	Serial and parallel carry	30↑			30↑			ns
	Clear inactive state	60↑			60↑			
Operating free-air temperature, T_A		−55		125	0		70	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

'2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54143, SN74143			SN54144, SN74144			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX	2.4			2.4			V
		Q_A, Q_B, Q_C, Q_D								
		Maximum count								
V_{OL}	Low-level output voltage	Q_A, Q_B, Q_C, Q_D, RBO	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.4			0.4	V
		Maximum count								
$V_{O(off)}$	Off-state output voltage	Outputs a thru g, dp	V_{CC} = MAX, I_{OH} = 250 μA	7			15			V
$V_{O(on)}$	On-State output voltage	Outputs a thru g, dp	V_{CC} = MIN, See Note 3						0.6	V
$I_{O(on)}$	On-state output current	Outputs a thru g	V_{CC} = MIN, V_O = 1 V	9	15					mA
			V_{CC} = 5 V, V_O = 2 V		15					
			V_{CC} = MAX, V_O = 5 V		15	22				
		Output dp	V_{CC} = MIN, V_O = 1 V	4.5	7					
			V_{CC} = 5 V, V_O = 2 V		7					
			V_{CC} = MAX, V_O = 5 V		7	12				
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Serial carry	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		RBO node		−0.12	−0.5		−0.12	−0.5		mA
		Other inputs				20			20	μA
I_{IL}	Low-level input current	Serial carry	V_{CC} = MAX, V_I = 0.4 V, See Note 4			−1.6			−1.6	mA
		RBO node			−1.5	−2.4		−1.5	−2.4	
		Other inputs				−0.8			−0.8	
I_{OS}	Short-circuit output current	Q_A, Q_B, Q_C, Q_D	V_{CC} = MAX	−9		−27.5	−9		−27.5	mA
		Maximum count		−15		−55	−15		−55	
I_{CC}	Supply current		V_{CC} = MAX, See Note 5		56	93		56	93	mA

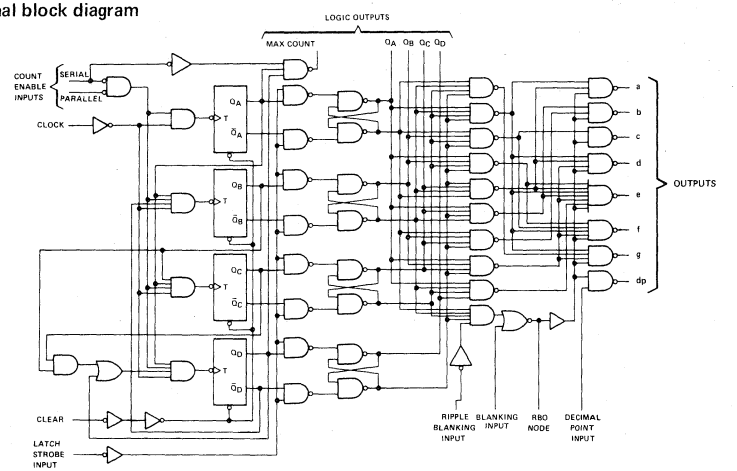
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 3. For SN54144, I_{OL} = 20 mA; for SN74144, I_{OL} = 25 mA.
4. I_{IL} at RBO node is tested with BI grounded and RBI at 4.5 V.
5. I_{CC} is measured after the following conditions are established:
a) Strobe = RBI = DP = 4.5 V
b) Parallel count enable = serial count enable = BI = GND
c) Clear (⊓) then clock until all outputs are on (⊔)
d) For '143, outputs "a" through "g" and "dp" = 2.5 V, all other outputs open. For '144, all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER §	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				12	18		MHz
t_{PLH}	Serial look-ahead	Maximum count	C_L = 15 pF, R_L = 560 Ω, See Note 6		12	20	ns
t_{PHL}					23	35	
t_{PLH}	Clock	Maximum count			26	40	ns
t_{PHL}					29	45	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D	C_L = 15 pF, R_L = 1.2 kΩ, See Note 6		28	45	ns
t_{PHL}					38	60	
t_{PHL}	Clear	Q_A, Q_B, Q_C, Q_D			57	90	ns

§ f_{max} ≡ Maximum clock frequency, t_{PLH} ≡ Propagation delay time, low-to-high-level output, t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 6: Load circuit and voltage waveforms are shown on page 148.

functional block diagram

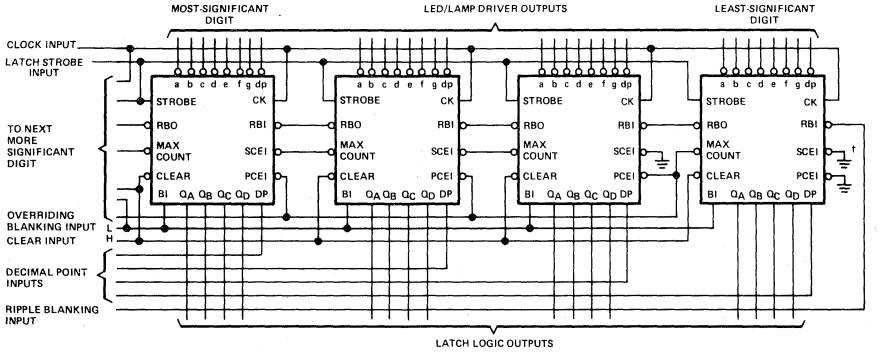


. . . Dynamic input activated by a transition from a high level to a low level.

TYPICAL APPLICATION DATA

This application demonstrates how the drivers may be cascaded for N-bit display applications. It features:

- Synchronous, look-ahead counting
- Ripple blanking of leading zeros; blanking of trailing zeros (not illustrated) can also be implemented
- Overriding blanking for total suppression or intensity modulation of display
- Direct parallel clear
- Latch strobe permits counter to acquire next display while viewing current display



†The serial count-enable input of the least-significant digit is normally grounded; however, it may be used as a count-enable control for the entire counter (high to disable, low to count) provided the logic level on this pin is not changed while the clock line is low or false counting may result.

TYPES SN54145, SN74145
BCD-TO-DECIMAL DECODER/DRIVERS

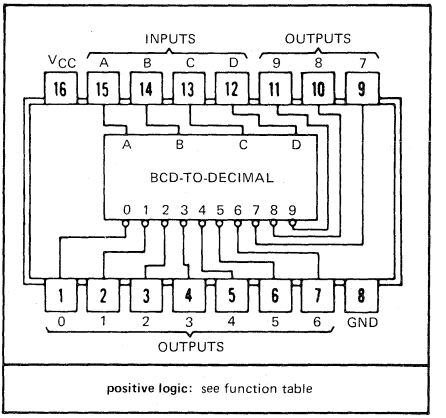
BULLETIN NO. DL-S 7211815, DECEMBER 1972

FOR USE AS LAMP, RELAY, OR MOS DRIVERS

featuring

- Full Decoding of Input Logic
- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



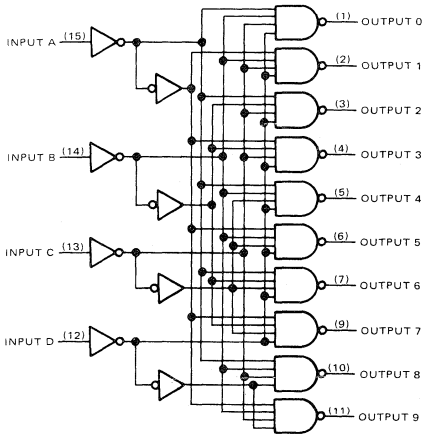
logic

FUNCTION TABLE

NO.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level (off), L = low level (on)

functional block diagram



description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Maximum current into any output (off-state) . . . . . 1 mA
Operating free-air temperature range: SN54145 Circuits . . . . . −55°C to 125°C
SN74145 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54145			SN74145			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Off-state output voltage			15			15	V
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
$V_{O(on)}$	On-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	$I_{O(on)}$ = 80 mA		0.5	0.9	V
			$I_{O(on)}$ = 20 mA			0.4	
$V_{O(off)}$	Off-state output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, $I_{O(off)}$ = 250 μA		15			V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54145		43	62	mA
			SN74145		43	70	

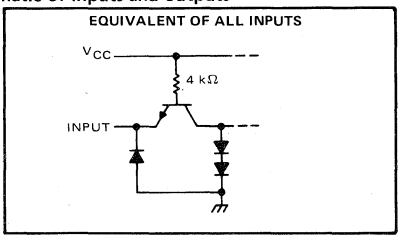
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with all inputs grounded and outputs open.

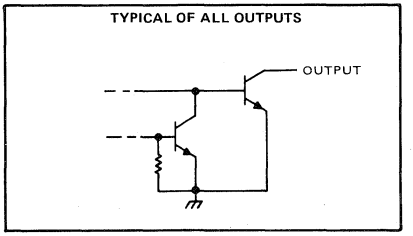
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 100 Ω, See Note 3			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output				50	ns

NOTE 3: Load circuit and waveforms are shown on page 148.

schematic of inputs and outputs





TYPES SN54147, SN54148, SN74147, SN74148
10-LINE-TO-4-LINE AND 8-LINE-TO-3-LINE PRIORITY ENCODERS

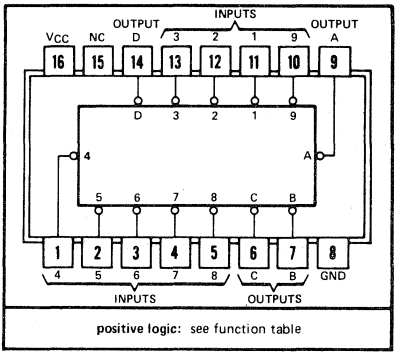
BULLETIN NO. DL-S 7211727, MAY 1972 – REVISED DECEMBER 1972

SN54147, SN74147

- Encodes 10-Line Decimal to 4-Line BCD
- Applications Include:

  Keyboard Encoding
  Range Selection
- Typical Data Delay . . . 10 ns
- Typical Power Dissipation . . . 225 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



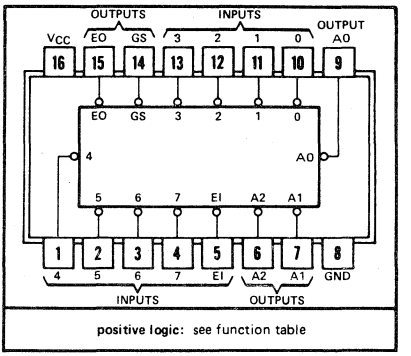
NC–No internal connection

SN54148, SN74148

- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:

  N-Bit Encoding
  Code Converters and Generators
- Typical Data Delay . . . 10 ns
- Typical Power Dissipation . . . 190 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



description

These TTL encoders feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. The SN54147 and SN74147 encode nine data lines to four-line (8-4-2-1) BCD. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All inputs are buffered to represent one normalized Series 54/74 load. The SN54148 and SN74148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

SN54147, SN74147
FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

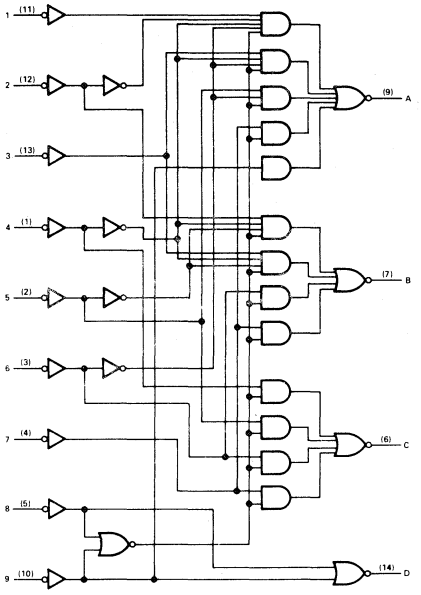
SN54148, SN74148
FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

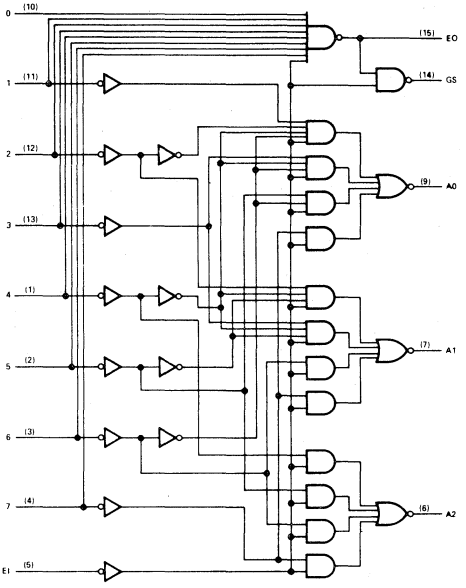
H = high logic level, L = low logic level, X = irrelevant

functional block diagrams

SN54147, SN74147



SN54148, SN74148



3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage: SN54148, SN74148 Circuits only (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54147, SN54148 Circuits . . . . . −55°C to 125°C
SN74147, SN74148 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For SN54148/SN74148 circuits, this rating applies between any two of the eight data lines, 0 through 7.

recommended operating conditions

	SN54147, SN54148			SN74147, SN74148			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54147 SN74147			SN54148 SN74148			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OH} = −800 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	0 input	V_{CC} = MAX, V_I = 2.4 V							40	μA
		Any input except 0					40			80	
I_{IL}	Low-level input current	0 input	V_{CC} = MAX, V_I = 0.4 V							−1.6	mA
		Any input except 0					−1.6			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−35		−85	−35		−85	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition 1		50	70		40	60	mA
				Condition 2		42	62		35	55	mA

NOTE 3: For SN54147, SN74147, I_{CC} (condition 1) is measured with input 7 grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open. For SN54148, SN74148, I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

SN54147, SN74147 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Any	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		9	14	ns
t_{PHL}						7	11	
t_{PLH}	Any	Any	Out-of-phase output			13	19	ns
t_{PHL}						10	15	

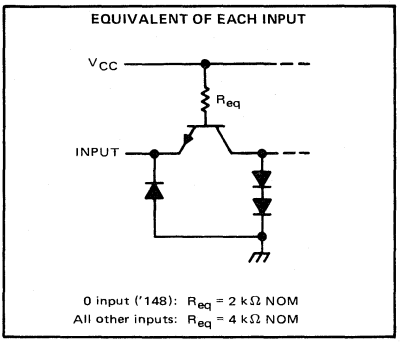
SN54148, SN74148 switching characteristics, V_{CC} = 5 V, T_A = 25°C

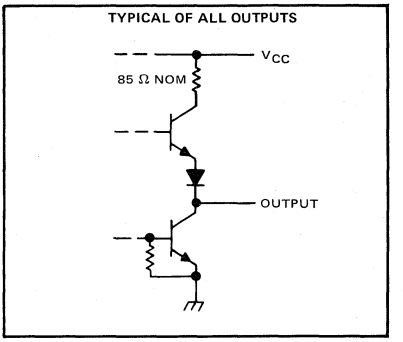
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	0 thru 7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		10	15	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	A0, A1, or A2	Out-of-phase output			13	19	ns
t_{PHL}						10	15	
t_{PLH}	0 thru 7	EO	Out-of-phase output			6	10	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	GS	In-phase output			14	21	ns
t_{PHL}						12	18	
t_{PLH}	EI	A0, A1, or A2	In-phase output			10	15	ns
t_{PHL}						10	15	
t_{PLH}	EI	GS	In-phase output			8	12	ns
t_{PHL}						10	15	
t_{PLH}	EI	EO	In-phase output			8	13	ns
t_{PHL}						13	19	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

NOTE 4: Load circuits and waveforms are shown on page 148.

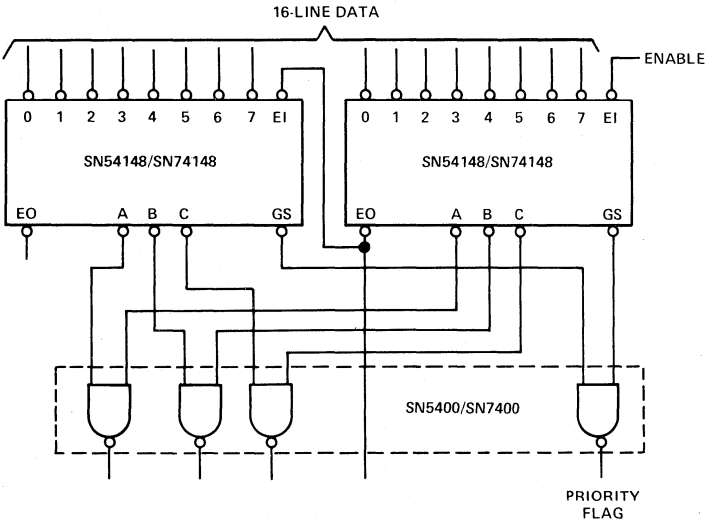
schematic of inputs and outputs





TYPICAL APPLICATION DATA

16-LINE-TO-4-LINE BINARY ENCODER



Full 4-bit binary 16-line-to-4-line encoding can be implemented as shown above. The enable input must be low to enable the function. Decoding with 2-input NAND gates produces true (active-high) data for the 4-line binary outputs. If active-low data is required, the SN5408/SN7408 AND gate may be used.

TYPES SN54150, SN54151A, SN54152A, SN54LS151, SN54LS152, SN54S151, SN74150, SN74151A, SN74152A, SN74LS151, SN74LS152, SN74S151
DATA SELECTORS/MULTIPLEXERS

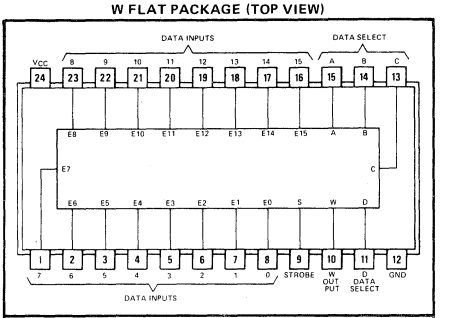
BULLETIN NO. DL-S 7211819, DECEMBER 1972

- '150 Selects One-of-Sixteen Data Sources
- Others Select One-of-Eight Data Sources
- Performs Parallel-to-Serial Conversion
- Permits Multiplexing from N Lines to One Line
- Also For Use as Boolean Function Generator
- Input-Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME DATA INPUT TO W OUTPUT	TYPICAL POWER DISSIPATION
'150	11 ns	200 mW
'151A	8 ns	145 mW
'152A	8 ns	130 mW
'LS151	11 ns†	30 mW
'LS152	11 ns†	28 mW
'S151	4.5 ns	225 mW

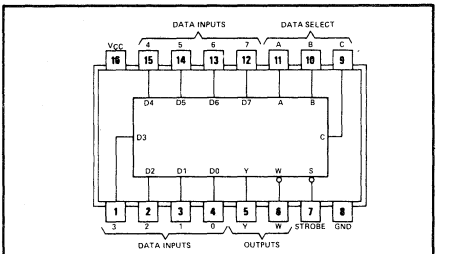
†Tentative data

'150
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



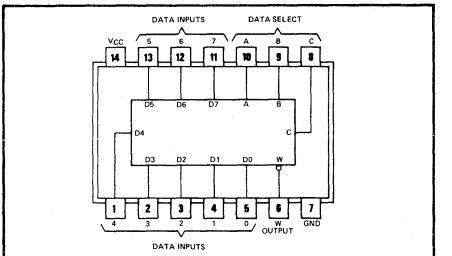
positive logic: see function table

'151A, 'LS151, 'S151
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

'152A, 'LS152
W FLAT PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select the desired data source. The '150 selects one-of-sixteen data sources; the '151A, '152A, 'LS151, 'LS152, and 'S151 select one-of-eight data sources. The '150, '151A, 'LS151, and 'S151 have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output (as applicable) low.

The '151A, 'LS151, and 'S151 feature complementary W and Y outputs whereas the '150, '152A, and 'LS152 have an inverted (W) output only.

The '151A and '152A incorporate address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the '151A outputs are enabled (i.e., strobe low).

logic

'150

FUNCTION TABLE

INPUTS					OUTPUT
SELECT				STROBE	W
D	C	B	A	S	
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

'151A, 'LS151, 'S151

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

'152A, 'LS152

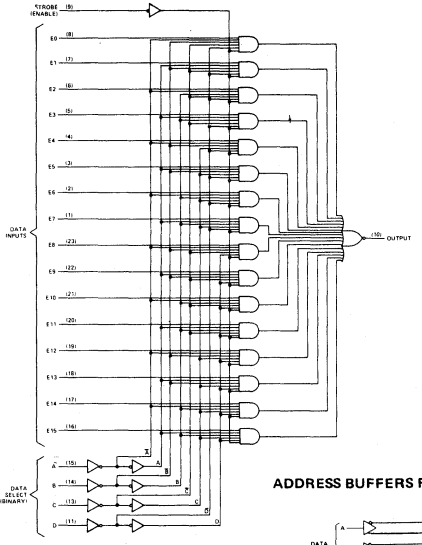
FUNCTION TABLE

SELECT INPUTS			OUTPUT
C	B	A	W
L	L	L	$\overline{D0}$
L	L	H	$\overline{D1}$
L	H	L	$\overline{D2}$
L	H	H	$\overline{D3}$
H	L	L	$\overline{D4}$
H	L	H	$\overline{D5}$
H	H	L	$\overline{D6}$
H	H	H	$\overline{D7}$

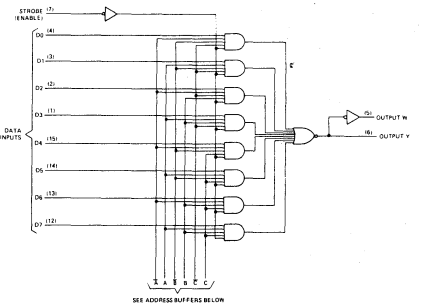
H = high level, L = low level, X = irrelevant
$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input
D0, D1 . . . D7 = the level of the D respective input

functional block diagrams

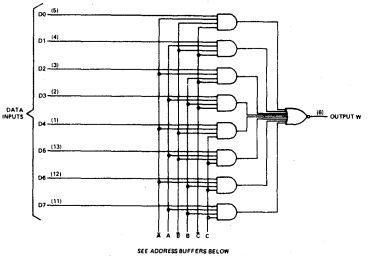
'150



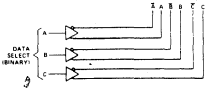
'151A, 'LS151, 'S151



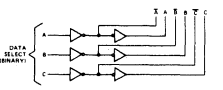
'152A, 'LS152



ADDRESS BUFFERS FOR '151A, '152A



ADDRESS BUFFERS FOR 'LS151, 'S151, 'LS152



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range: . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For the '150, input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN54'			SN74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'150			'151A, '152A			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA							−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−55	−20		−55	mA
			SN74'	−18		−55	−18		−55	
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	'150		40	68				mA
			'151A					29	48	
			'152A					26	43	

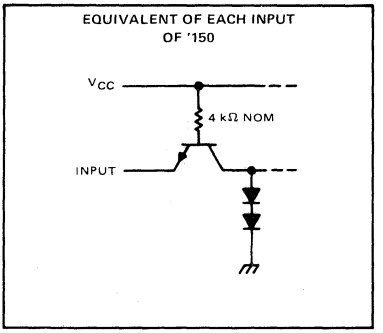
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output of the '151A should be shorted at a time.
NOTE 3: I_{CC} is measured with the strobe and data select inputs at 4.5 V, all other inputs and outputs open.

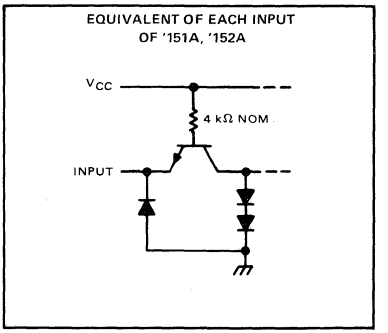
switching characteristics, V_{CC} = 5 V, T_A = 25°C

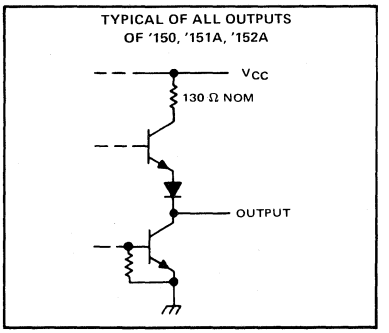
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'150			'151A, '152A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 400 Ω, See Note 4					25	38	ns
t_{PHL}								25	38	
t_{PLH}	A, B, C, or D (3 levels)	W			23	35		17	26	ns
t_{PHL}					22	33		19	30	
t_{PLH}	Strobe	Y						21	33	ns
t_{PHL}								22	33	
t_{PLH}	Strobe	W			15.5	24		14	21	ns
t_{PHL}					21	30		15	23	
t_{PLH}	D0 thru D7	Y						13	20	ns
t_{PHL}								18	27	
t_{PLH}	E0 thru E15, or D0 thru D7	W			13	20		8	14	ns
t_{PHL}					8.5	14		8	14	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS' Circuits . . . . . −55°C to 125°C
SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS'			SN74LS'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS'			SN74LS'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.6			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, Outputs open, All inputs at 4.5 V	'LS151		6.0	10		6.0	10	mA
			'LS152		5.6	9		5.6	9	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

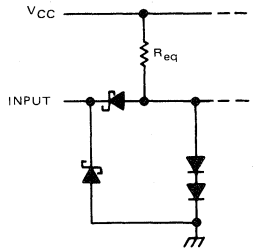
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS', SN74LS'			UNIT
				MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 5		27	43	ns
t_{PHL}					31	50	
t_{PLH}	A, B, or C (3 levels)	W			24	39	ns
t_{PHL}					20	32	
t_{PLH}	Strobe	Y			23	37	ns
t_{PHL}					26	42	
t_{PLH}	Strobe	W			19	31	ns
t_{PHL}					16	26	
t_{PLH}	Any D	Y			16	26	ns
t_{PHL}					20	32	
t_{PLH}	Any D	W			13	21	ns
t_{PHL}					9	15	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 5: See load circuits and waveforms on page 149.

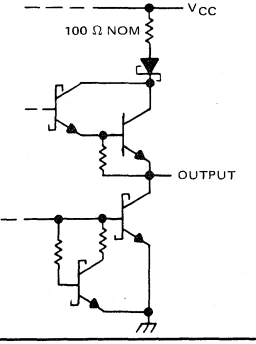
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT
OF 'LS151, 'LS152



Data select and strobe: R_{eq} = 20 kΩ NOM
Data inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF ALL OUTPUTS
OF 'LS151, 'LS152



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S151 Circuits . . . . . −55°C to 125°C
SN74S151 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S151			SN74S151			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs at 4.5 V, All outputs open			45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

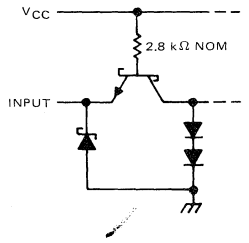
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S151, SN74S151			UNIT
				MIN	TYP	MAX	
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 280 Ω, See Note 4		12	18	ns
t_{PHL}					12	18	
t_{PLH}	A, B, or C (3 levels)	W			10	15	ns
t_{PHL}					9	13.5	
t_{PLH}	Any D	Y			8	12	ns
t_{PHL}					8	12	
t_{PLH}	Any D	W			4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	Strobe	Y			11	16.5	ns
t_{PHL}					12	18	
t_{PLH}	Strobe	W			9	13	ns
t_{PHL}					8.5	12	

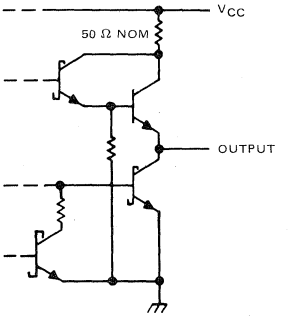
¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 4: See load circuits and waveforms on page 148.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT OF 'S151



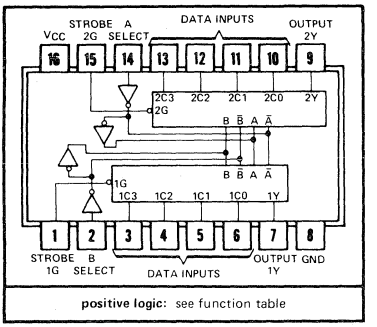
TYPICAL OF ALL OUTPUTS OF 'S151



TYPES SN54153, SN54L153, SN54LS153, SN54S153, SN74153, SN74L153, SN74LS153, SN74S153
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7211852, DECEMBER 1972

'153, 'LS153, 'S153 . . . J, N, OR W PACKAGE
'L153 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

- Permits Multiplexing from N lines to 1 line
- Performs Parallel-to-Serial Conversion
- Strobe (Enable) Line Provided for Cascading (N lines to n lines)
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with most TTL and DTL Circuits

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIMES FROM DATA	FROM STROBE	FROM SELECT	TYPICAL POWER DISSIPATION
'153	14 ns	17 ns	22 ns	180 mW
'L153	27 ns	34 ns	44 ns	90 mW
'LS153	14 ns	19 ns	22 ns	31 mW
'S153	6 ns	9.5 ns	12 ns	225 mW

3

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

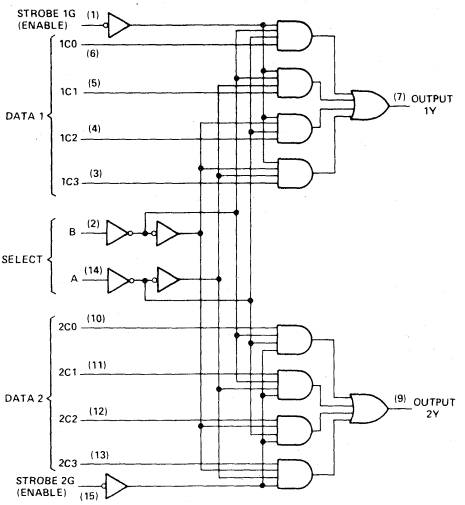
Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '153, 'L153, 'S153 . . . . . 5.5 V
'LS153 . . . . . 7 V
Operating free-air temperature range: SN54', SN54L', SN54LS', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74LS', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

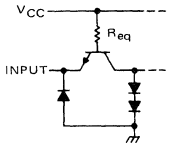
NOTE 1: Voltage values are with respect to network ground terminal.

functional block diagram



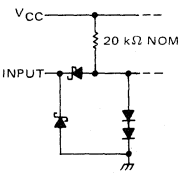
schematics of inputs and outputs

EQUIVALENT OF INPUTS OF '153, 'L153

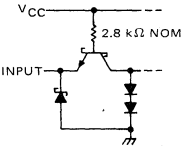


'153: R_{eq} = 4 kΩ NOM
'L153: R_{eq} = 8 kΩ NOM

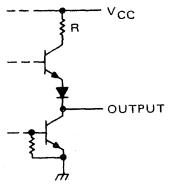
EQUIVALENT OF INPUTS OF 'LS153



EQUIVALENT OF INPUTS OF 'S153

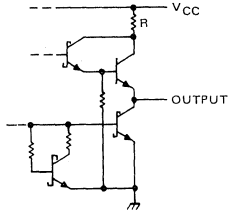


TYPICAL OF OUTPUTS OF '153, 'L153



'153: R = 130 Ω NOM
'L153: R = 260 Ω NOM

TYPICAL OF OUTPUTS OF 'LS153, 'S153



'LS153: R = 200 Ω NOM
'S153: R = 50 Ω NOM

recommended operating conditions

	SN54153			SN74153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54153			SN74153			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−57	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2		36	52		36	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 30 pF, R_L = 400 Ω, See Note 3		12	18	ns
t_{PHL}	Data	Y			15	23	ns
t_{PLH}	Select	Y			22	34	ns
t_{PHL}	Select	Y			22	34	ns
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}	Strobe	Y			15	23	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

recommended operating conditions

	SN54L153			SN74L153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L153			SN74L153			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.8			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−10		−28	−9		−30	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2		18	26		18	30	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 30 pF, R_L = 400 Ω, See Note 3		24	36	ns
t_{PHL}	Data	Y			30	46	ns
t_{PLH}	Select	Y			44	68	ns
t_{PHL}	Select	Y			44	68	ns
t_{PLH}	Strobe	Y			38	60	ns
t_{PHL}	Strobe	Y			30	46	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

recommended operating conditions

	SN54LS153			SN74LS153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS153			SN74LS153			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.6			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.36			−0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, See Note 2			6.2	10		6.2	10	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 4		10	15	ns
t_{PHL}	Data	Y			17	26	ns
t_{PLH}	Select	Y			19	29	ns
t_{PHL}	Select	Y			25	38	ns
t_{PLH}	Strobe	Y			16	24	ns
t_{PHL}	Strobe	Y			21	32	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuits and voltage waveforms are shown on page 149.

recommended operating conditions

	SN54S153			SN74S153			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		V
			Series 74S	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX, See Note 2			45	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE: 2: I_{CCL} is measured with the outputs open and all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 280 Ω, See Note 3		6	9	ns
t_{PHL}	Data	Y			6	9	ns
t_{PLH}	Select	Y			11.5	18	ns
t_{PHL}	Select	Y			12	18	ns
t_{PLH}	Strobe	Y			10	15	ns
t_{PHL}	Strobe	Y			9	13.5	ns

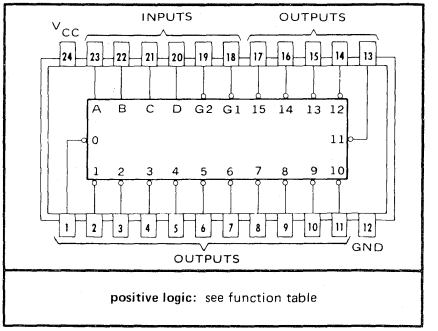
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54154, SN54L154, SN74154, SN74L154
4-LINE-TO-16-LINE DECODERS/ DEMULTIPLEXERS

BULLETIN NO. DL-S 7211805, DECEMBER 1972

- '154 is Ideal for High-Performance Memory Decoding
- 'L154 is Designed for Power-Critical Applications
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data From One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits

'154 . . . J, N, OR W PACKAGE
'L154 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

TYPE	TYPICAL AVERAGE PROPAGATION DELAY 3 LEVELS OF LOGIC	STROBE	TYPICAL POWER DISSIPATION
'154	23 ns	19 ns	170 mW
'L154	46 ns	38 ns	85 mW

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. For ultra-high-speed systems, SN54S138/SN74S138 and SN54S139/SN74S139 are recommended.

These circuits are fully compatible for use with most other TTL and DTL circuits. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Series 54 and 54L devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74L devices are characterized for operation from 0°C to 70°C.

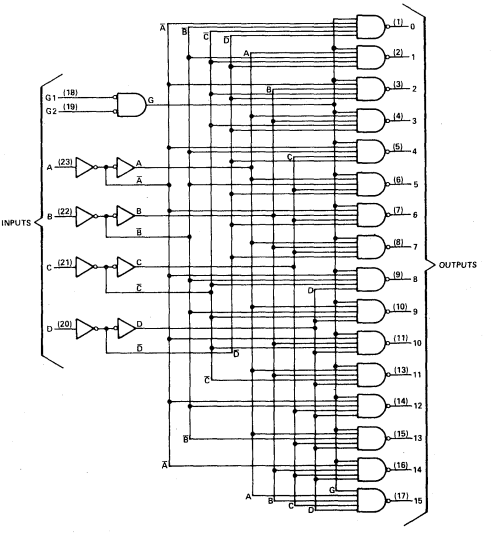
logic

FUNCTION TABLE

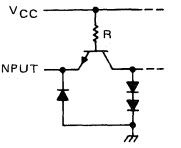
INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

functional block diagram and schematics of inputs and outputs

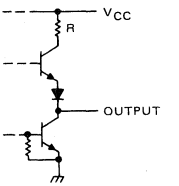


EQUIVALENT OF EACH INPUT



'154: R = 4 kΩ NOM
'L154: R = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



'154: R = 130 Ω NOM
'L154: R = 260 Ω NOM

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54154			SN74154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54154			SN74154			UNIT
			MIN	TYP	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−55	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		34	49		34	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54L154 Circuits . . . . . −55°C to 125°C
SN74L154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54L154			SN74L154			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−9		−29	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54L154		17	25	mA
			SN74L154		17	28	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 800 Ω, See Note 3		48	72	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			44	66	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			36	54	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

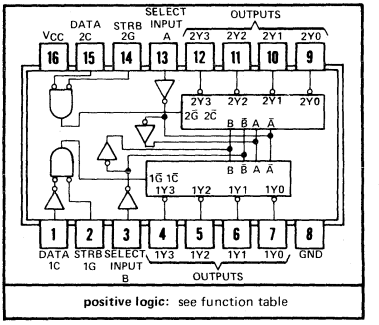
TYPES SN54155, SN54156, SN54LS155, SN74155, SN74156, SN74LS155
DUAL 2-LINE-TO-4-LINE DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7211850, DECEMBER 1972

- Applications:
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
  - Totem Pole ('155, 'LS155)
  - Open-Collector ('156)

TYPES	TYPICAL AVERAGE PROPAGATION DELAY 3 GATE LEVELS	TYPICAL POWER DISSIPATION
'155, '156	21 ns	125 mW
'LS155	18 ns	31 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

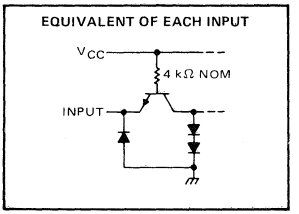
description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. Input clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design.

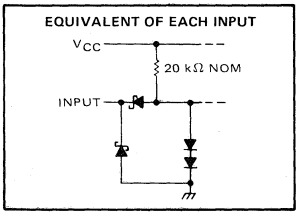
Series 54 and 54LS are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

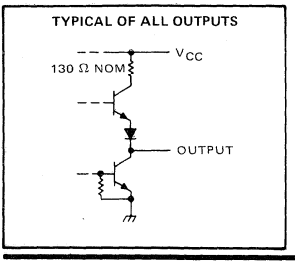
'155, '156



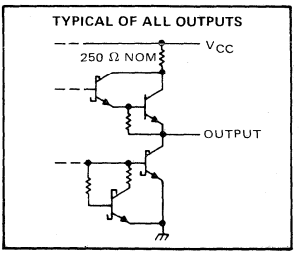
'LS155



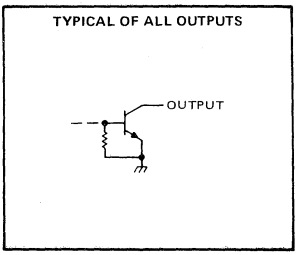
'155



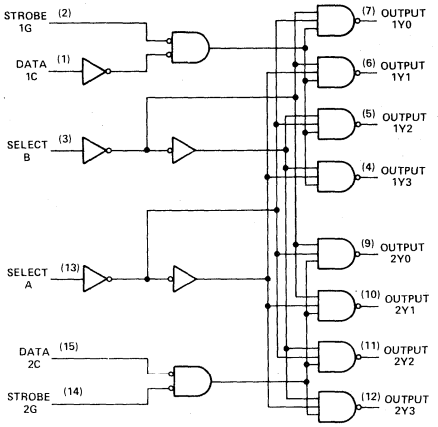
'LS155



'156



functional block diagram and logic



FUNCTION TABLES
2-LINE-TO-4-LINE DECODER
OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

FUNCTION TABLE
3-LINE-TO-8-LINE DECODER
OR 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: '155, '156 . . . . . 5.5 V
'LS155 . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' . . . . . −55°C to 125°C
SN74', SN74LS' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54155			SN74155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54155 SN74155			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54155	−20		−55	mA
			SN74155	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54155		25	35	mA
			SN74155		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			18	27	ns
t_{PLH}	A or B	Y	3			21	32	ns
t_{PHL}	A or B	Y	3			21	32	ns
t_{PLH}	1C	Y	3			16	24	ns
t_{PHL}	1C	Y	3			20	30	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148

recommended operating conditions

	SN54LS155			SN74LS155			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS155			SN74LS155			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.36			−0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			6.1	10		6.1	10	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	SN54LS155 SN74LS155			UNIT
					MIN	TYP	MAX	
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 2 kΩ, See Note 4		10	15	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			19	30	ns
t_{PLH}	A or B	Y	3			17	26	ns
t_{PHL}	A or B	Y	3			19	30	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			18	27	ns

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 149.

recommended operating conditions

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54156 SN74156			UNIT
				MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54156		25	35	mA
			SN74156		25	40	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with outputs open, A, B, and 1C inputs at 4.5 V, and 2C, 1G, and 2G inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	C_L = 15 pF, R_L = 400 Ω, See Note 3		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2			20	30	ns
t_{PLH}	A or B	Y	3			23	34	ns
t_{PHL}	A or B	Y	3			23	34	ns
t_{PLH}	1C	Y	3			18	27	ns
t_{PHL}	1C	Y	3			22	33	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54157, SN54L157, SN54S157, SN54S158, SN74157, SN74L157, SN74S157, SN74S158
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7211847, DECEMBER 1972

features

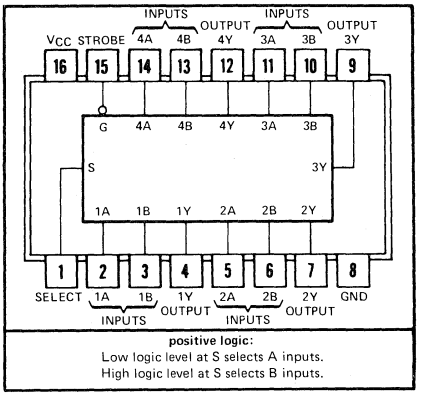
- Buffered Inputs and Outputs
- Three Speed/Power Ranges Available

TYPES	TYPICAL AVERAGE PROPAGATION TIME	TYPICAL POWER DISSIPATION
'157	9 ns	150 mW
'L157	18 ns	75 mW
'S157	5 ns	250 mW
'S158	4 ns	195 mW

applications

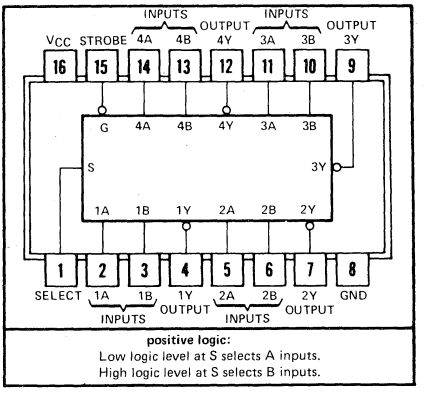
- Expand Any Data Input Point
- Multiplex Dual-Data Buses
- Generate Four Functions of Two Variables (One Variable is Common)
- Source Programmable Counters

'157, 'S157 . . . J, N, OR W PACKAGE
'L157 . . . J OR N PACKAGE
(TOP VIEW)



positive logic:
Low logic level at S selects A inputs.
High logic level at S selects B inputs.

'S158 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic:
Low logic level at S selects A inputs.
High logic level at S selects B inputs.

description

These monolithic, data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The '157, 'L157, and 'S157 present true data whereas the 'S158 presents inverted data to minimize propagation delay time.

FUNCTION TABLE

INPUTS				OUTPUT Y	
STROBE	SELECT	A	B	'157, 'L157, 'S157	'S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant

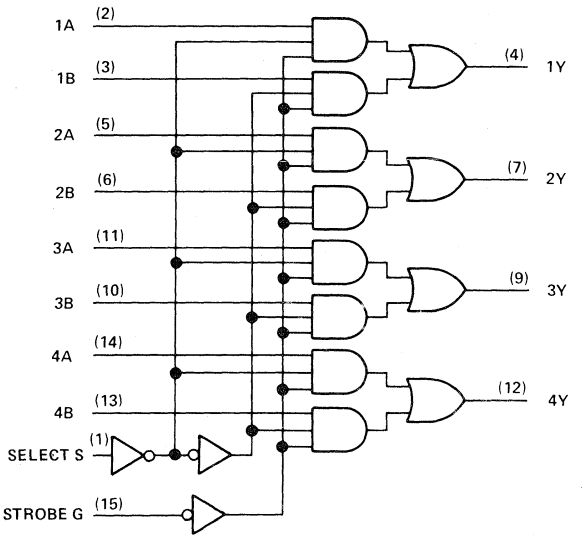
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54L', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74L', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

functional block diagram

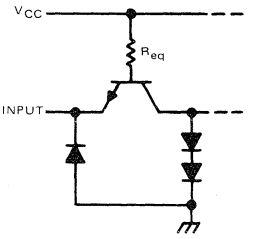
'157, 'L157



schematics of inputs and outputs

'157, 'L157,

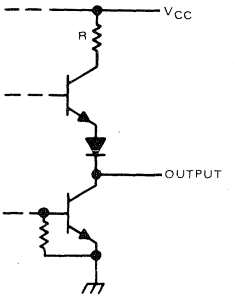
EQUIVALENT OF EACH INPUT



'157: R_{eq} = 4 kΩ NOM
'L157: R_{eq} = 8 kΩ NOM

'157, 'L157

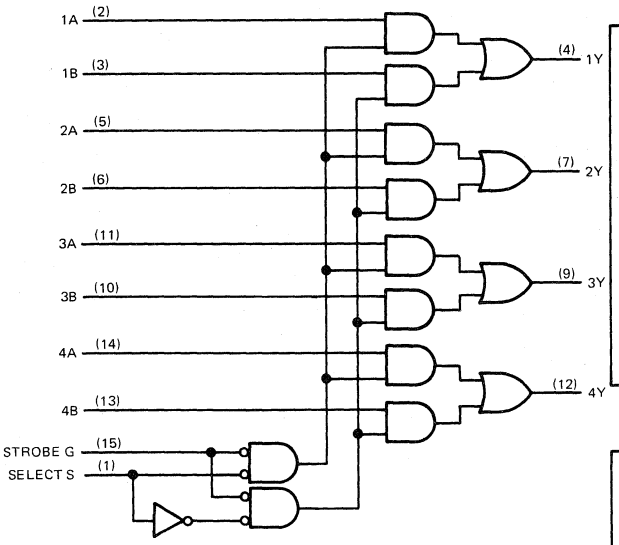
TYPICAL OF ALL OUTPUTS



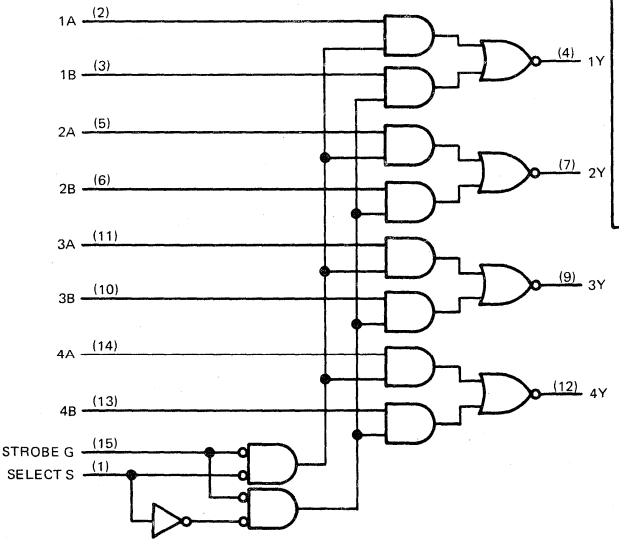
'157: R = 100 Ω NOM
'L157: R = 200 Ω NOM

functional block diagrams

'S157



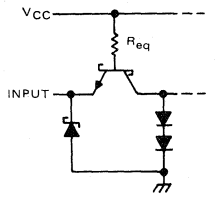
'S158



schematics of inputs and outputs

'S157, 'S158

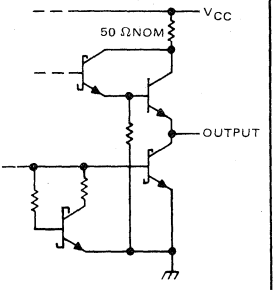
EQUIVALENT OF EACH INPUT



S or G inputs: R_{eq} = 1.4 kΩ NOM
A or B inputs: R_{eq} = 2.8 kΩ NOM

'S157, 'S158

TYPICAL OF ALL OUTPUTS



3

recommended operating conditions

	SN54157			SN74157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54157			SN74157			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		30	48		30	48	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 400 Ω, See Note 3		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

recommended operating conditions

	SN54L157			SN74L157			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−9		−28	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		15	24	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 800 Ω, See Note 3		18	28	ns
t_{PHL}				18	28	
t_{PLH}	Strobe			26	40	ns
t_{PHL}				28	42	
t_{PLH}	Select			30	46	ns
t_{PHL}				36	54	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms shown on page 148.

recommended operating conditions

	SN54S157 SN54S158			SN74S157 SN74S158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S157 SN74S157			SN54S158 SN74S158			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	Series 54S	2.5	3.4		2.5	3.4		V
				Series 74S	2.7	3.4		2.7	3.4		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	S or G input	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
		A or B input					50			50	
I_{IL}	Low-level input current	S or G input	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
		A or B input					−2			−2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			50	78		39	61	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.

NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	SN54S157 SN74S157			SN54S158 SN74S158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	C_L = 15 pF, R_L = 280 Ω, See Note 3		5	7.5		4	6	ns
t_{PHL}				4.5	6.5		4	6	
t_{PLH}	Strobe			8.5	12.5		6.5	11.5	ns
t_{PHL}				7.5	12		7	12	
t_{PLH}	Select			9.5	15		8	12	ns
t_{PHL}				9.5	15		8	12	

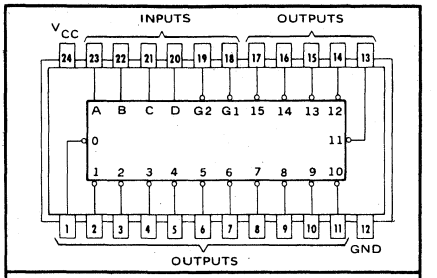
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54159, SN74159
4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS
WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7211800, DECEMBER 1972

- Open-Collector Outputs for Interfacing with MOS or Memory Decoders/Drivers
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data from One Input Line to Any One of 16 Outputs
- Typical Average Propagation Delay Times:
  24 ns through 3 Levels of Logic
  19 ns from Strobe Input
- Output Off-State Current is Less Than 50 μA
- Fully Compatible with Most TTL, DTL, and MSI Circuits

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive open-collector outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing MOS memory decoding or for interfacing with discrete memory address drivers. For ultra-high-speed applications, the SN54S138/SN74S138 or SN54S139/SN74S139 is recommended.

These circuits are fully compatible for use with most other TTL and DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54159 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN74159 is characterized for operation from 0°C to 70°C.

function table

Same as SN54154, SN74154. See page 309.

functional block diagram

Same as SN54154, SN74154. See page 309.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54159 Circuits	–55°C to 125°C
SN74159 Circuits	0°C to 70°C
Storage temperature range	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal

recommended operating conditions

	SN54159			SN74159			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V			50	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, All inputs grounded		34	56	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

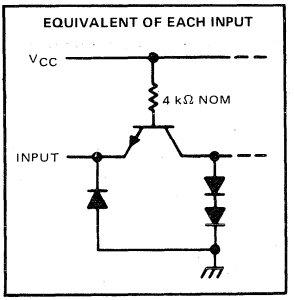
3

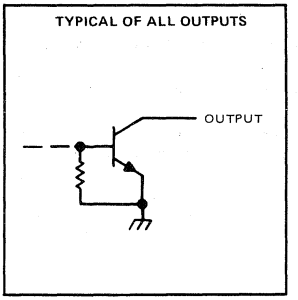
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 2		23	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			24	36	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			22	36	ns

NOTE 2: See load circuit and waveforms shown on page 148.

schematics of inputs and outputs





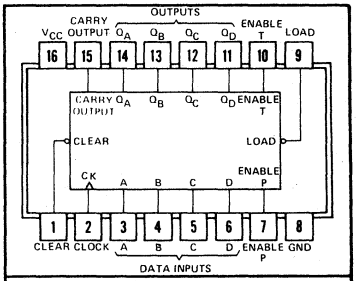
TYPES SN54160 THRU SN54163, SN74160 THRU SN74163
SYNCHRONOUS 4-BIT COUNTERS

BULLETIN NO. DL-S 7211385, OCTOBER 1970–REVISED DECEMBER 1972

SN54160, SN54161, SN74160, SN74161 . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
SN54162, SN54163, SN74162, SN74163 . . . FULLY SYNCHRONOUS COUNTERS

- Internal Look-Ahead for Fast Counting Schemes
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs
- Typical Maximum Input Clock Frequency . . . 32 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see description

3

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The '160 and '162 are decade counters and the '161 and '163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the '160 and '161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. The clear function for the '162 and '163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

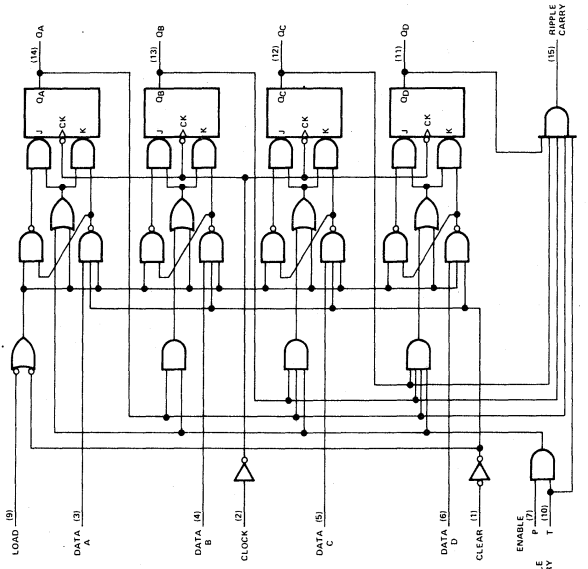
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

functional block diagrams

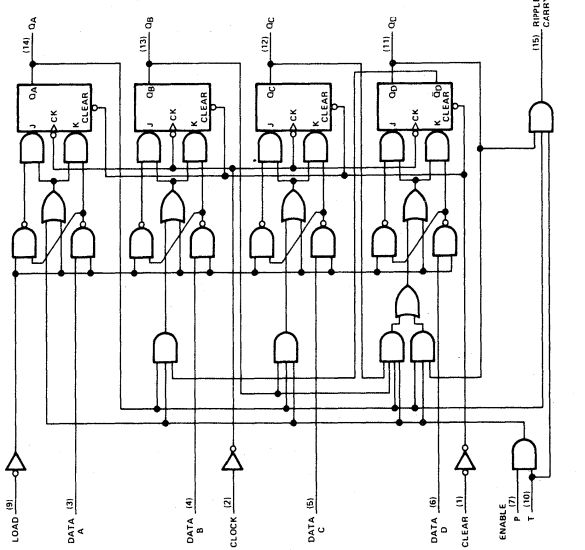
SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.

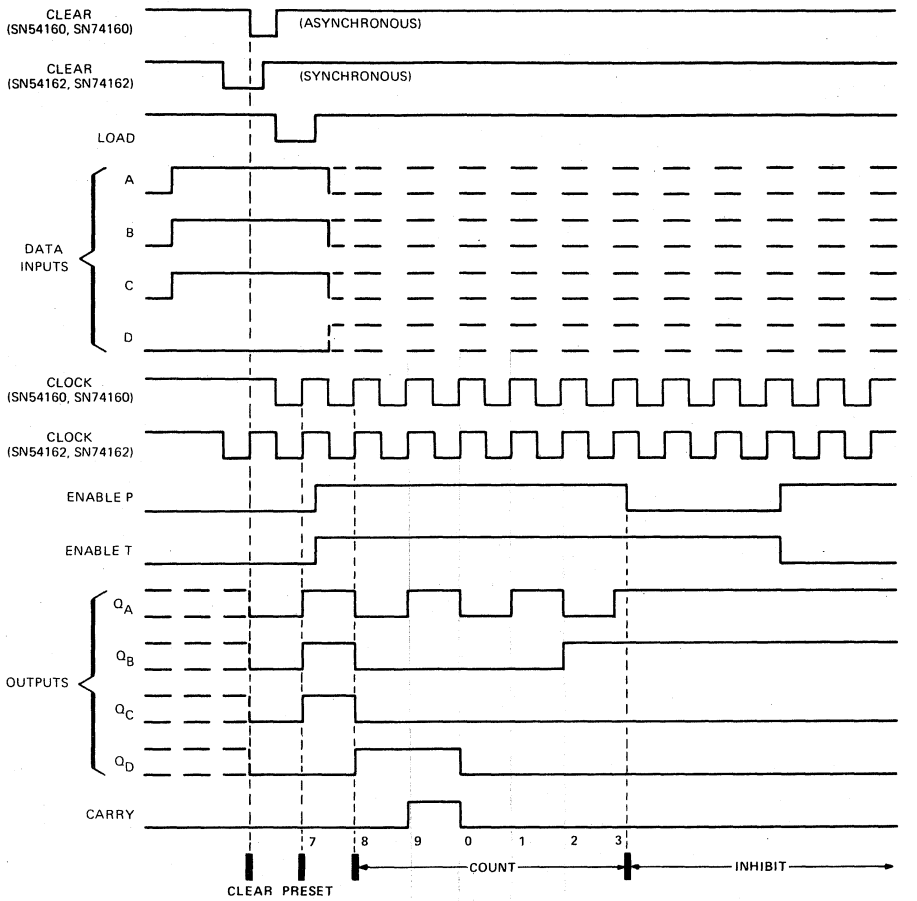


SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit

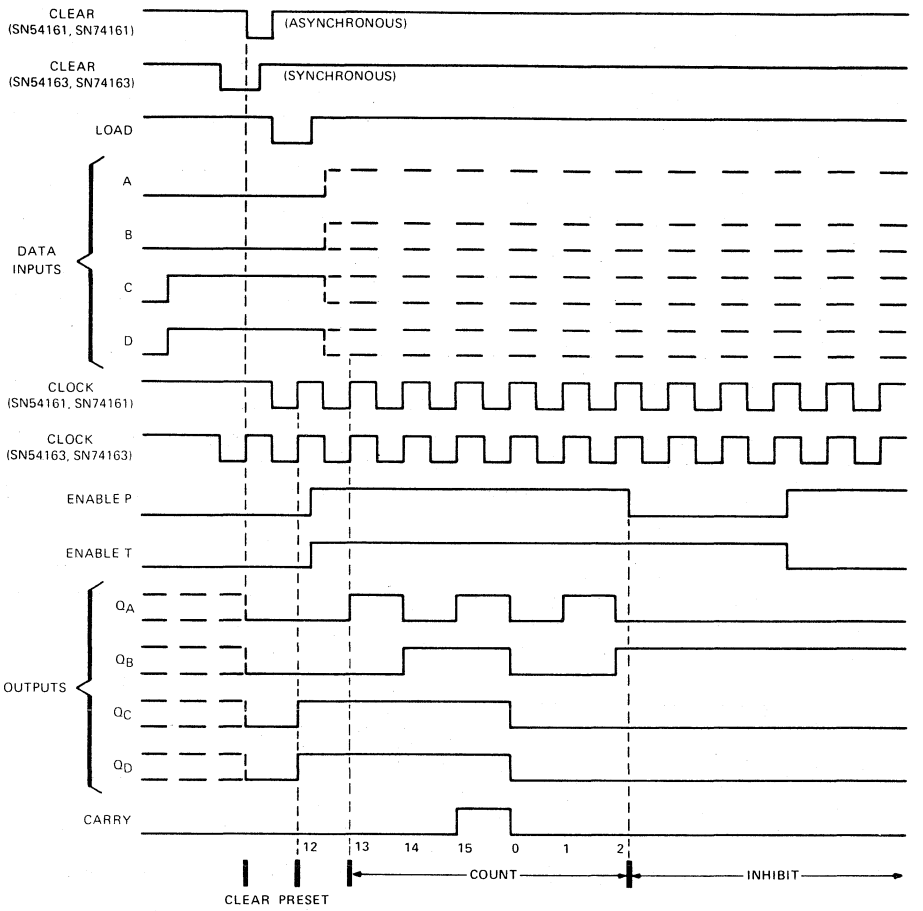


SN54161, SN54163, SN74161, SN74163 SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 3)	Data inputs A, B, C, D	15			15			ns
	Enable P	20			20			
	Load	25			25			
	Clear◇	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

◇This applies only for '162 and '163, which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

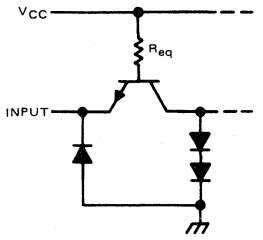
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		SEE FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	1, 2	C_L = 15 pF, R_L = 400 Ω, See Notes 5 and 6	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock	1, 2			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock	1, 2			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock (load input high)	1, 2			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock (load input high)	1, 2			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T	1, 3			10	14	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T	1, 3			10	14	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear	1, 3			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock (load input low)	1, 3			17	25	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock (load input low)	1, 3			19	29	ns

NOTES: 5. Propagation delay for clearing is measured from the clear input for the '160 and '161 or from the clock input transition for the '162 and '163.
6. See waveforms in Figures 1 and 2. Load circuit is shown on page 148.

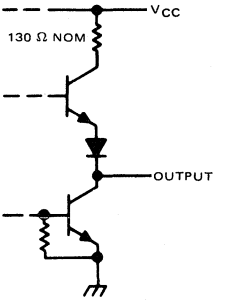
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

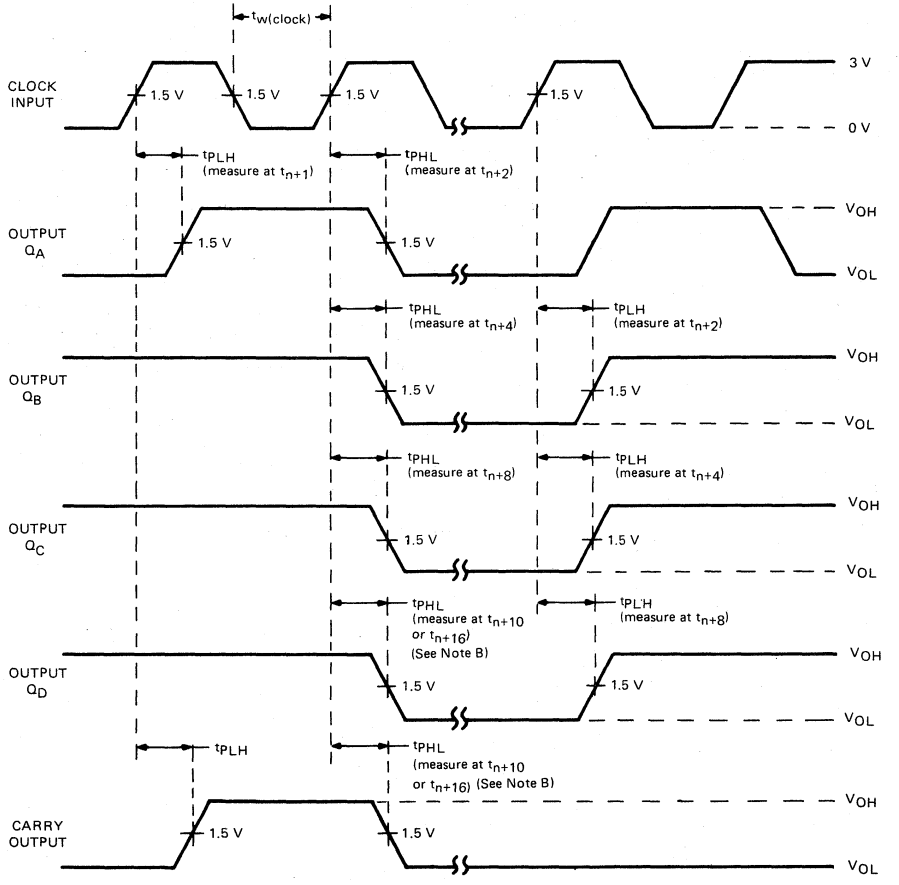


Clock: R_{eq} = 2.8 kΩ NOM
Enable T: R_{eq} = 2 kΩ NOM
Clear, Enable P: R_{eq} = 4 kΩ NOM
A, B, C, D: R_{eq} = 6 kΩ NOM

TYPICAL OF ALL OUTPUTS



PARAMETER MEASUREMENT INFORMATION



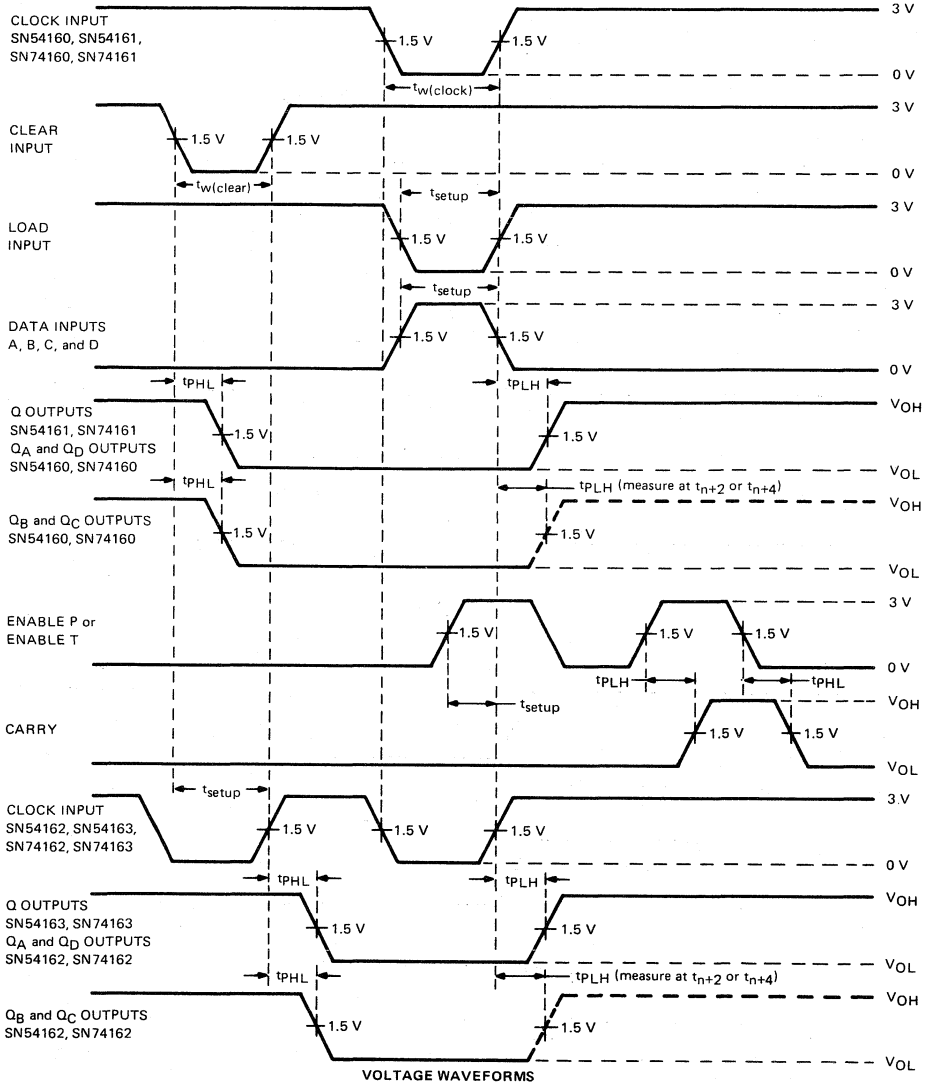
VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the SN54160, SN54162, SN74160, and SN74162, and at t_{n+16} for the SN54161, SN54163, SN74161, and SN74163, where t_n is the bit time when all outputs are low.

FIGURE 1—SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by generators having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

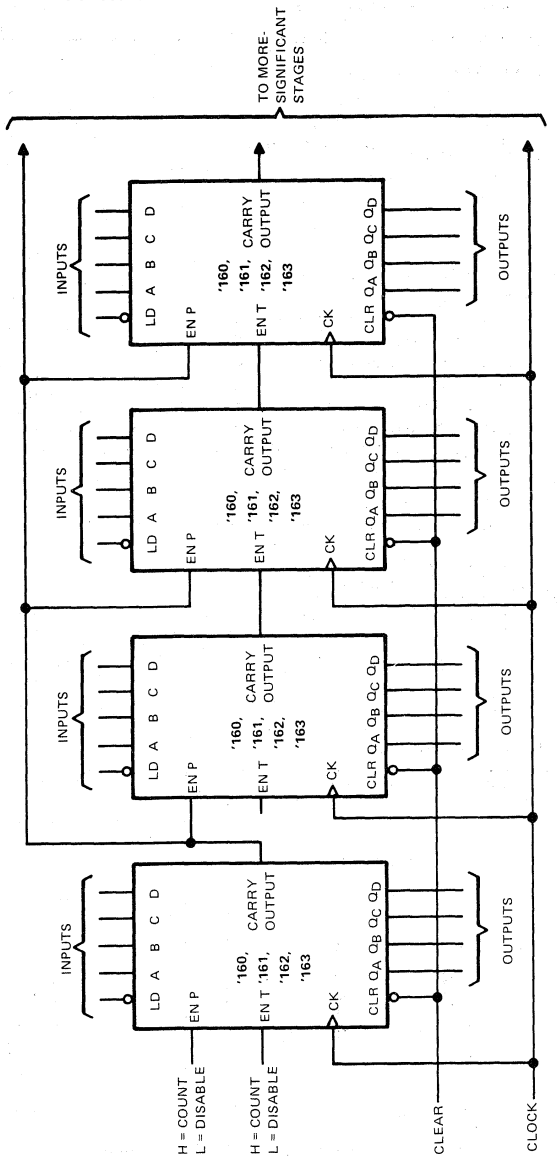
B. Enable P and enable T setup times are measured at $t_n = 0$.

FIGURE 2–SWITCHING TIMES

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS USING '160, '161, '162 AND '163 COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The '160 or '162 will count in BCD and the '161 or '163 will count in binary. Virtually any count mode (modulo-N, N_1-to-N_2, N_1-to-maximum) can be used with this fast look-ahead scheme.



3

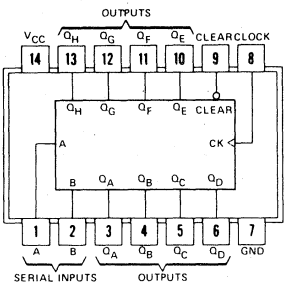
TYPES SN54164, SN54L164, SN74164, SN74L164
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

BULLETIN NO. DL-S 7211835, DECEMBER 1972

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'164	36 MHz	21 mW per bit
'L164	18 MHz	11 mW per bit

'164 . . . J, N, OR W PACKAGES
'L164 . . . J, N, OR T PACKAGES
(TOP VIEW)



positive logic: see function table

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Series 54 and 54L devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74L devices are characterized for operation from 0°C to 70°C.

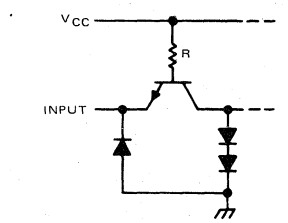
FUNCTION TABLE

INPUTS				OUTPUTS			
CLEAR	CLOCK	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{A0}	Q_{B0}		Q_{H0}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

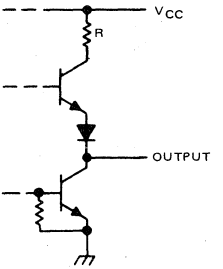
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



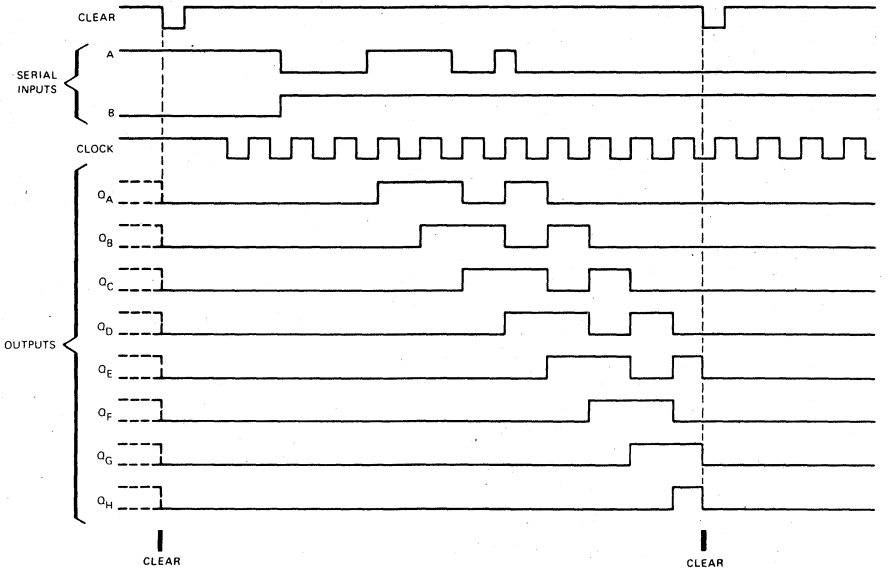
'164: R = 4 kΩ NOM
'L164: R = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS

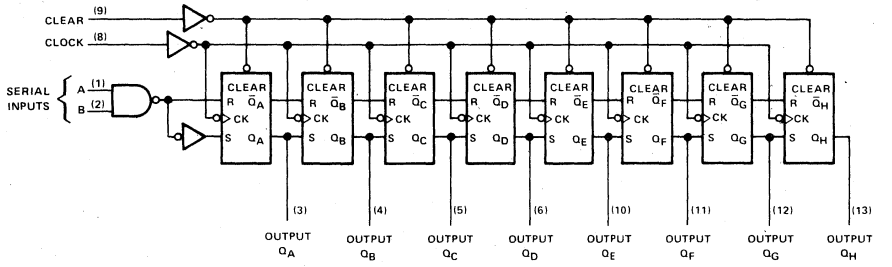


'164: R = 200 Ω NOM
'L164: R = 400 Ω NOM

typical clear, shift, and clear sequences



functional block diagram



. . . . dynamic input activated by transition from a high level to a low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54164 Circuits . . . . . −55°C to 125°C
SN74164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54164			SN74164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			8			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	15			15			ns
Data hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54164			SN74164			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.2		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 8 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−10		−27.5	−9		−27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	$V_{I(clock)}$ = 0.4 V		30			30		mA
			$V_{I(clock)}$ = 2.4 V		37	54		37	54	

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than two outputs should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF		24	36	ns
			C_L = 50 pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8	17	27	ns
			C_L = 50 pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10	21	32	ns
			C_L = 50 pF	10	25	37	

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54L164 Circuits . . . . . −55°C to 125°C
SN74L164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54L164			SN74L164			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−200			−200	μA
Low-level output current, I_{OL}			4			4	mA
Clock frequency, f_{clock}	0		12	0		12	MHz
Width of clock or clear input pulse, t_w	40			40			ns
Data setup time, t_{setup} (see Figure 1)	30			30			ns
Data hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

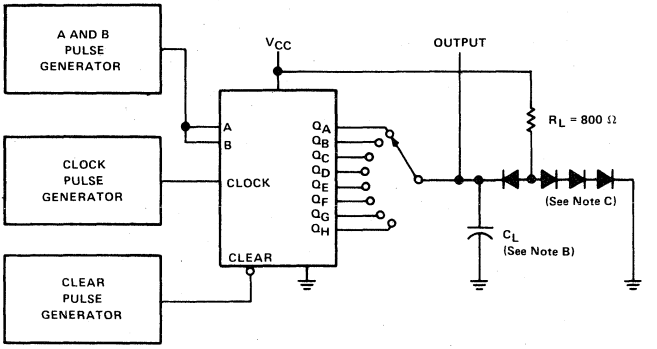
PARAMETER		TEST CONDITIONS†	SN54L164			SN74L164			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −200 μA	2.4	3.2		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 4 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.8			−0.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−5		−20	−4		−20	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		19	27		19	27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, the clock input at 2.4 V, and a momentary ground, then 4.5 V, applied to clear.

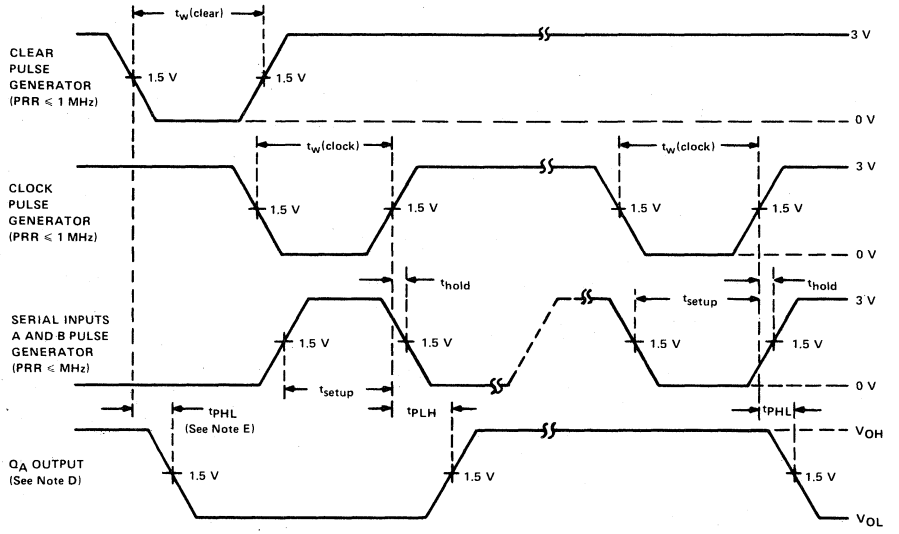
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	12	18		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF		48	72	ns
			C_L = 50 pF		56	84	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8	34	54	ns
			C_L = 50 pF	10	20	60	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10	42	64	ns
			C_L = 50 pF	10	50	74	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or 1N916.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

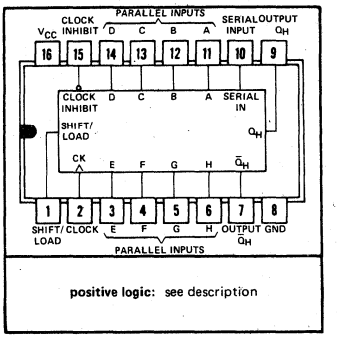
FIGURE 1–SWITCHING TIMES

TYPES SN54165, SN74165
PARALLEL-LOAD 8-BIT SHIFT REGISTERS

BULLETIN NO. DL-S 7211375, OCTOBER 1970—REVISED DECEMBER 1972

- Typical Maximum Input Clock Frequency . . . 26 MHz
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see description

description

The SN54105 and SN74105 are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

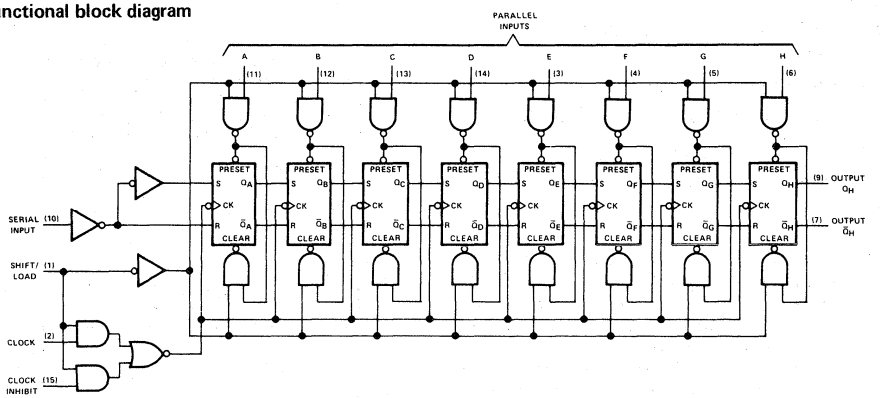
All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The SN54105 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74165 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

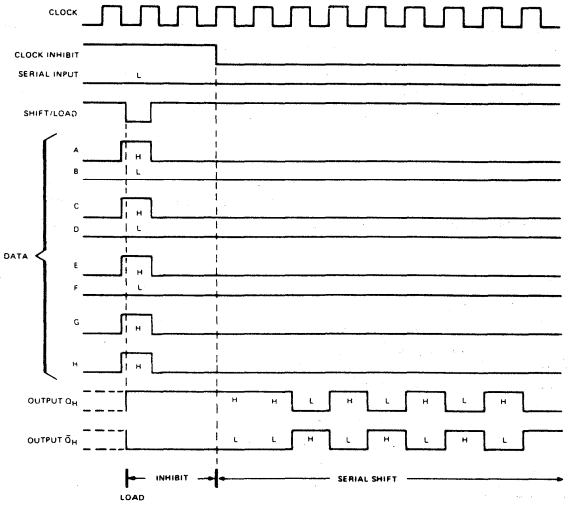
INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn}, = the level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

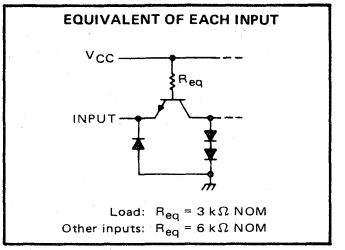
functional block diagram

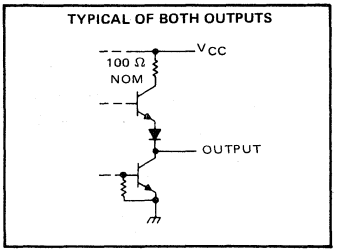


typical shift, load, and inhibit sequences



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54165 Circuits	−55°C to 125°C
SN74165 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the shift/load input in conjunction with the clock or clock-inhibit inputs.

recommended operating conditions

	SN54165			SN74165			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	15			15			ns
Clock-enable setup time, t_{setup} (see Figure 1)	30			30			ns
Parallel input setup time, t_{setup} (see Figure 1)	10			10			ns
Serial input setup time, t_{setup} (see Figure 2)	20			20			ns
Shift setup time, t_{setup} (see Figure 2)	45			45			ns
Hold time at any input, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54165			SN74165			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Load input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		42	63		42	63	mA

NOTE 3: With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

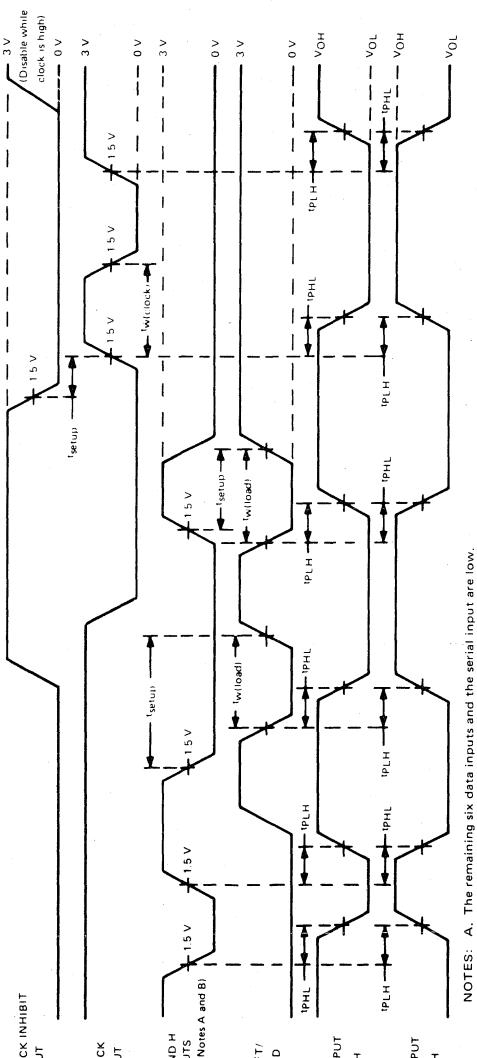
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See figures 1 thru 3	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\overline{Q}_H$			18	27	ns
t_{PHL}					18	27	

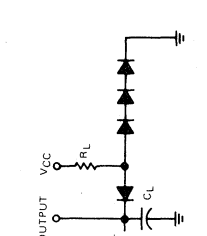
¶f_{max} = Maximum clock frequency
t_{PLH} = Propagation delay time, low-to-high-level output
t_{PHL} = Propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



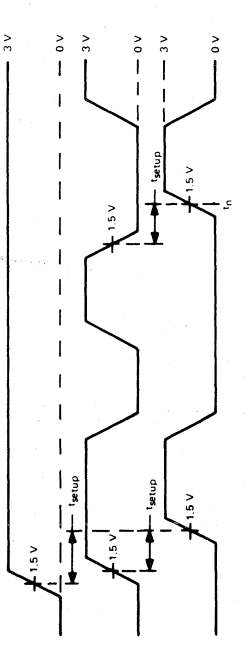
NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.
When testing f_{max} vary clock PRR.

FIGURE 1–VOLTAGE WAVEFORMS



NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

FIGURE 3–LOAD CIRCUIT FOR SWITCHING TESTS



NOTES: A. The eight data inputs and the clock inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

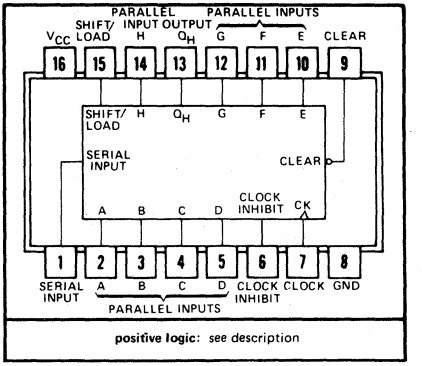
FIGURE 2–VOLTAGE WAVEFORMS

TEXAS INSTRUMENTS

TYPES SN54166, SN74166
8-BIT SHIFT REGISTERS

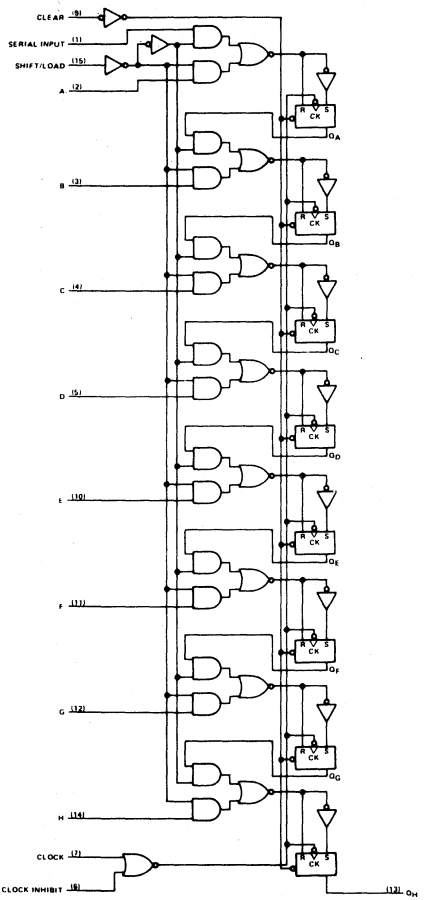
BULLETIN NO. DL-S 7211808, DECEMBER 1972

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see description

functional block diagram



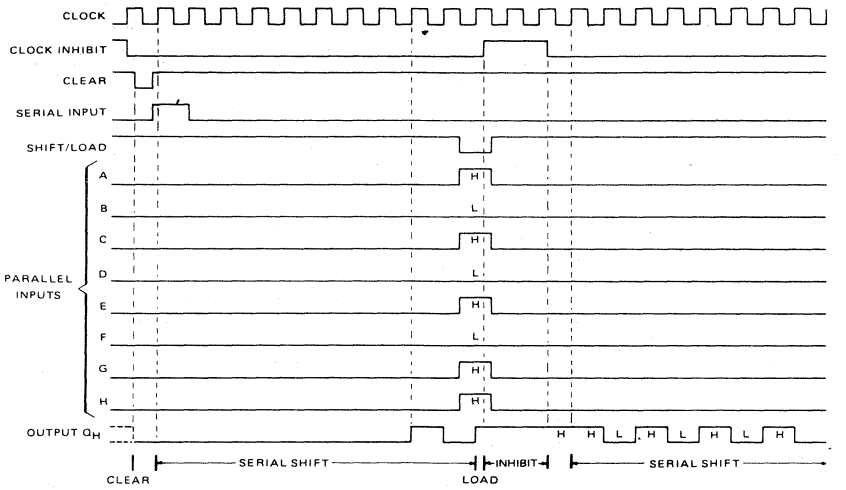
. . . dynamic input activated by transition from a high level to a low level.

description

The SN54166 and SN74166 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

typical clear, shift, load, inhibit, and shift sequences

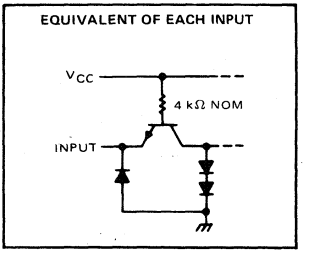


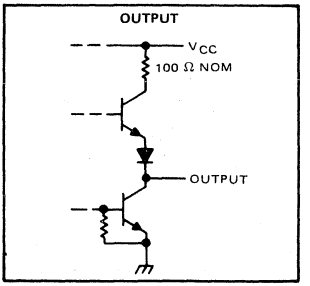
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G, respectively, before the most-recent ↑ transition of the clock.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54166 Circuits (see Note 2) . . . . . −55°C to 125°C
SN74166 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN54166			SN74166			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{setup}	30			30			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Hold time at any input, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

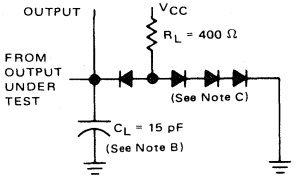
PARAMETER		TEST CONDITIONS†	SN54166			SN74166			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3		72	104		72	116	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54166 in the N package operating at free-air temperatures above 122°C requires a heat-sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 48°C/W.
3. With all outputs open, 4.5 V applied to the serial input, all other inputs except the clock grounded, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

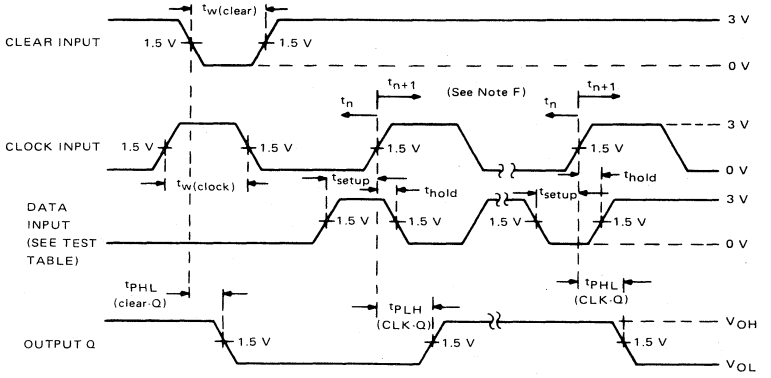
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
H	0 V	Q_H at t_{n+1}
Serial Input	4.5 V	Q_H at t_{n+8}



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq 20$ ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq 20$ ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

F. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

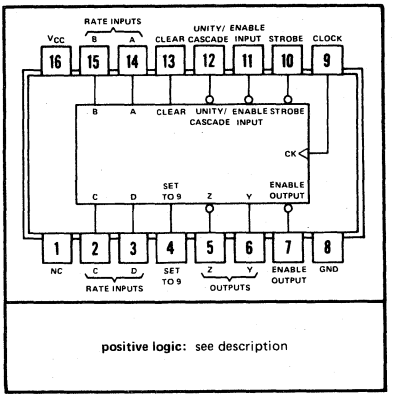
FIGURE 1

TYPES SN54167, SN74167
SYNCHRONOUS DECADE RATE MULTIPLIERS

BULLETIN NO DL-S 7211813, DECEMBER 1972

- Perform Fixed-Rate or Variable-Rate Frequency Division
- For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations
- Typical Maximum Clock Frequency . . . 32 Megahertz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



NC—No internal connection

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. These decade counters feature buffered clock, clear, enable and set-to-nine inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe set-to-nine, and enable inputs are low. With the counter enabled, the output frequency is equal to the input frequency multiplied by the rate input M and divided by 10, ie.:

$$f_{out} = \frac{M \cdot f_{in}}{10}$$

where: $M = D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$ for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform two-decade rate multiplication (0-99), the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output. For longer words, see typical application data, Figure 1.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

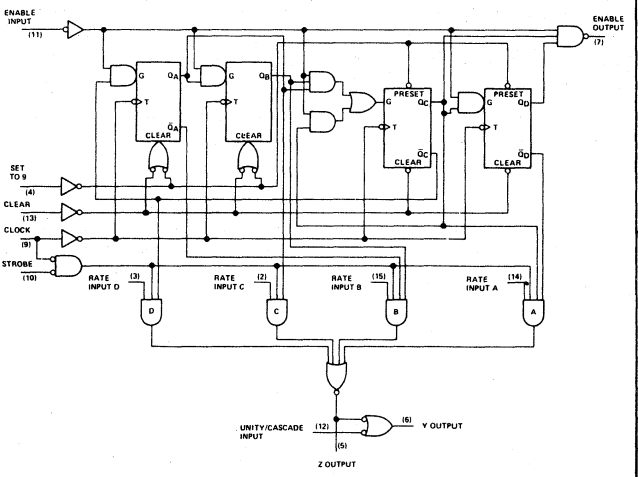
All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the output. These devices are completely compatible with most TTL and DTL families. Typical dissipation is 270 milliwatts. The SN54167 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74167 is characterized for operation from 0°C to 70°C.

STATE AND/OR RATE FUNCTION TABLE (See Note A)

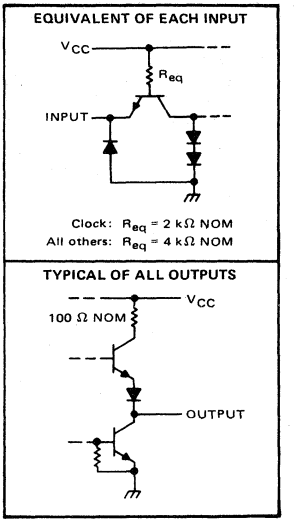
INPUTS									OUTPUTS			
			BCD RATE				NUMBER OF	UNITY/	LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	D	C	B	A	CLOCK PULSES	CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	C
L	L	L	L	L	L	H	10	H	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	C
L	L	L	L	L	H	H	10	H	3	3	1	C
L	L	L	L	H	L	L	10	H	4	4	1	C
L	L	L	L	H	L	H	10	H	5	5	1	C
L	L	L	L	H	H	L	10	H	6	6	1	C
L	L	L	L	H	H	H	10	H	7	7	1	C
L	L	L	H	L	L	L	10	H	8	8	1	C
L	L	L	H	L	L	H	10	H	9	9	1	C
L	L	L	H	L	H	L	10	H	8	8	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.
B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low unity/cascade will cause output Y to remain high.
C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.
D. These input conditions exceed the range of the decimal rate inputs.
E. Unity/cascade can be used to inhibit output Y.

functional block diagram



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54167 . . . . . −55°C to 125°C
SN74167 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54167			SN74167			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Input clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	15			15			ns
Width of set-to-nine pulse $t_{w(set\text{-}to\text{-}9)}$	15			15			ns
Setup time, t_{setup}: (See Figure 1)							
From positive-going transition of clock pulse	25			25			ns
From negative-going transition of previous clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	ns
Hold time, t_{hold}: (See Figure 1)							
From positive-going transition of clock pulse	0		$t_{w(clock)}-10$	0		$t_{w(clock)}-10$	ns
From negative-going transition of previous clock pulse	20		$t_{cp}-10$	20		$t_{cp}-10$	ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	clock input	V_{CC} = MAX,	V_I = 2.4 V			80	μA
		other inputs					40	
I_{IL}	Low-level input current	clock inputs	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
		other inputs					−1.6	
I_{OS}	Short circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH}	Supply current, output high		V_{CC} = MAX,	See Note 2		43		mA
I_{CCL}	Supply current, output low		V_{CC} = MAX,	See Note 3		65	99	mA

NOTES: 2. I_{CCH} is measured with outputs open and all inputs low.
3. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input which is low.

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETERS¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 4	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PHL}	Set-to-9	Enable			18	27	ns
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

¶f_{max} is maximum input clock frequency.
t_{PLH} is propagation delay time, low-to-high-level output.
t_{PHL} is propagation delay time, high-to-low-level output.
NOTE 4: Load circuit, voltage waveforms, and input conditions for measuring switching characteristics are the same as those for the SN5497 and SN7497, page 252.

3

TYPICAL APPLICATION DATA

This application demonstrates how the decimal-rate multipliers may be cascaded for longer words. Three decades are illustrated (0.999 to 999) although longer words can be implemented by using the pattern shown. The output is decoded either from output Y with a NOR gate or from output Z with a NAND gate. Either method of decoding produces the complement of the output used.

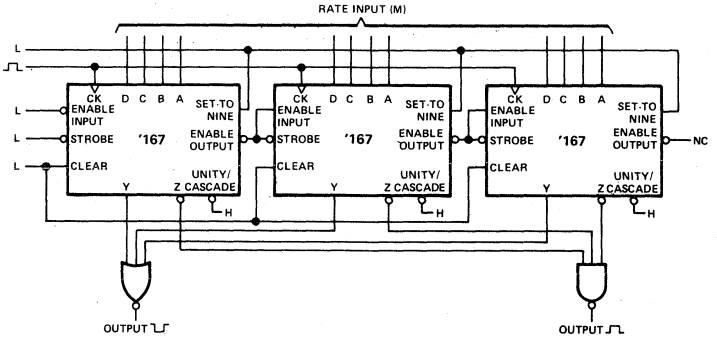


FIGURE 1

TEXAS INSTRUMENTS

TYPES SN54170, SN74170
4-BY-4 REGISTER FILES

BULLETIN NO. DL-S 7211349, JUNE 1970—REVISED DECEMBER 1972

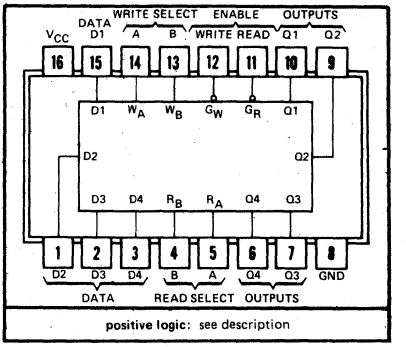
- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Open-Collector Outputs with 30-μA Maximum Off-State Current
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:

  Scratch-Pad Memory

  Buffer Storage between Processors

  Fast Multiplication Schemes

SN54170 . . . J OR W PACKAGE
SN74170 . . . J, N, OR W PACKAGE
(TOP VIEW)



description

The SN54170 and SN74170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates on a monolithic chip measuring only 90 by 110 mils. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a nondestructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

The SN54170 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74170 is characterized for operation from 0°C to 70°C.

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant.
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_0 = the level of Q before the indicated input conditions were established.
D. W0B1 = The first bit of word 0, etc.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
High-level output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54170 (see Note 2) . . . . . −55°C to 125°C
SN74170 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

3

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Figure 1)	Data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	Write select with respect to write enable, $t_{setup(W)}$	15			15			ns
Hold times, high- or low-level data (see Note 3 and Figure 1)	Data input with respect to write enable, $t_{hold(D)}$	15			15			ns
	Write select with respect to write enable, $t_{hold(W)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 4)		25			25			ns
Operating free-air temperature range, T_A (see Note 2)		−55		125	0		70	°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54170 in the W package operating at free-air temperatures above 105°C requires a heat sink that provides a thermal resistance from case to free-air, $R_{\theta CA}$, of not more than 38°C/W.
3. Write-select setup time will protect the data written into the previous address. If protection of data in the previous address is not required, $t_{setup(W)}$ can be ignored as any address selection sustained for the final 30 ns of the write-enable pulse and during $t_{hold(W)}$ will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.
4. Latch time is the time required for the internal output of the latch to assume the state of new data. See Figure 1. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_O = 5.5 V			30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 5	SN54170		127§	140	mA
			SN74170		127§	150	

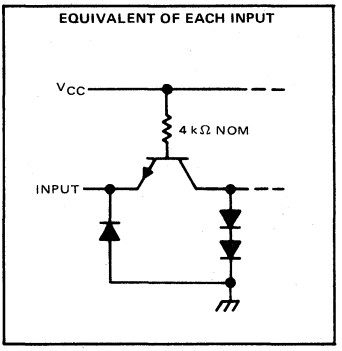
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Typical supply current shown is an average for 50% duty cycle.
NOTE 5: Maximum I_{CC} is guaranteed for the following worst-case conditions: 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

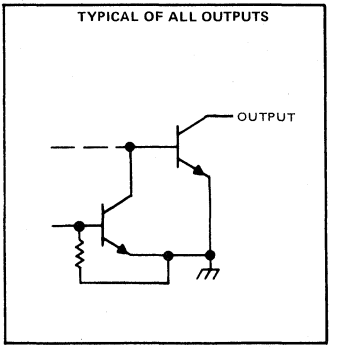
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Read enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Figure 1		10	15	ns
t_{PHL}					20	30	
t_{PLH}	Write enable	Any Q			25	40	ns
t_{PHL}					34	45	
t_{PLH}	Read address	Any Q			23	35	ns
t_{PHL}					30	40	
t_{PLH}	Data	Any Q			20	30	ns
t_{PHL}					30	45	

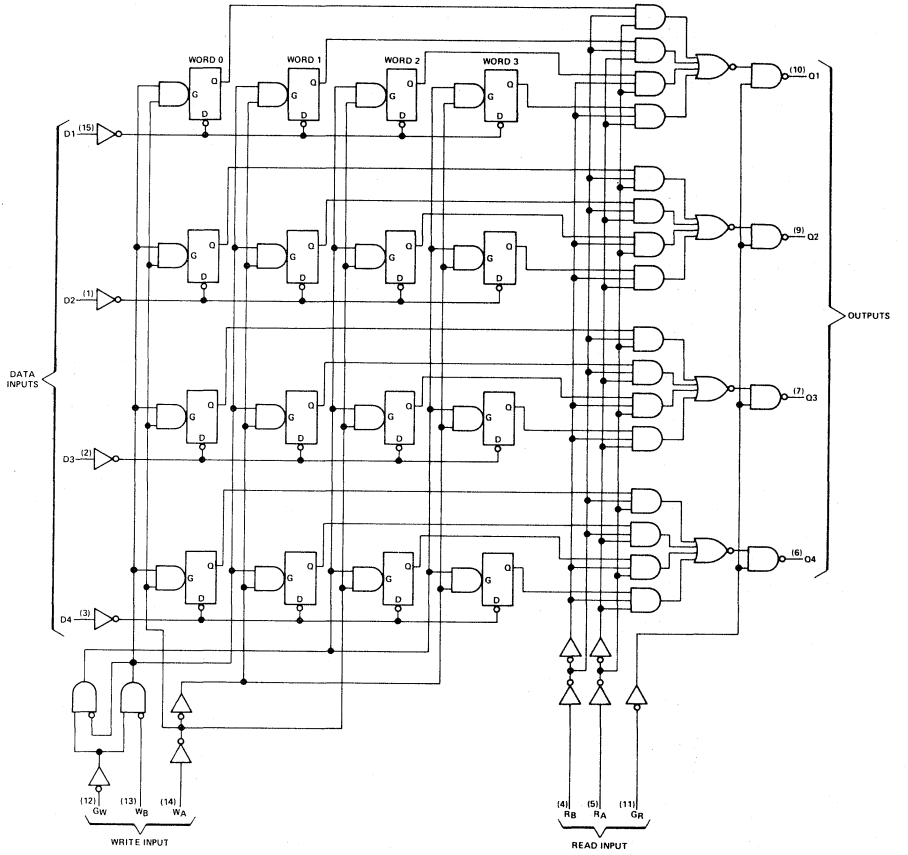
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

schematics of inputs and outputs

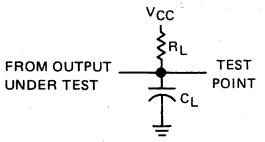




functional block diagram

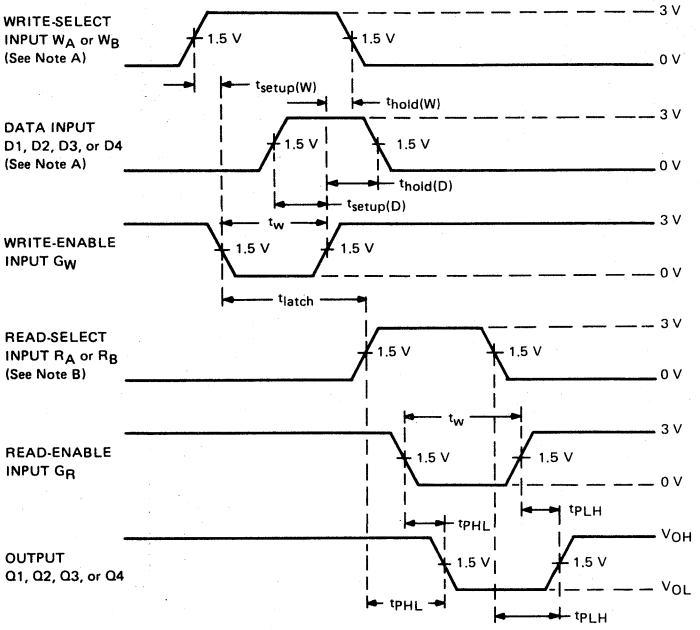


PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance

LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. High-level input pulses at the select and data inputs are illustrated; however, times associated with low-level pulses are measured from the same reference points.

B. When measuring delay times from a read-select input, the read-enable input is low. When measuring delay times from the read-enable input, both read-select inputs have been established at steady states.

C. Input waveforms are supplied by generators having the following characteristics: PRR $\leq$ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle $\leq$ 50%, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

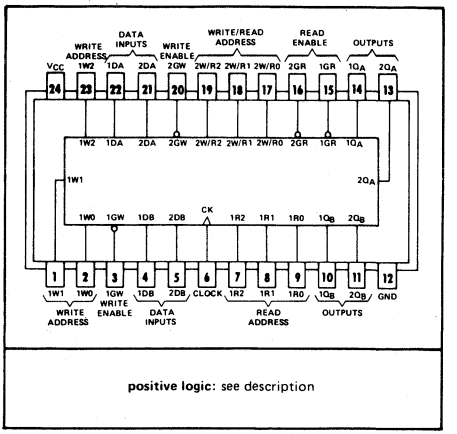
FIGURE 1–SWITCHING TIMES

TYPE SN74172
16-BIT MULTIPLE-PORT REGISTER FILE WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211744, MAY 1972 – REVISED DECEMBER 1972

- **Independent Read/Write Addressing Permits Simultaneous Reading and Writing**
- **Organized as Eight Words of Two Bits Each**
- **Fast Access Times:**
  From Read Enable . . . 15 ns Typical
  From Read Select . . . 33 ns Typical
- **Three-State Outputs Simplify Use in Bus-Organized Systems**
- **Applications:**
  Stacked Data Registers
  Scratch-Pad Memory
  Buffer Storage Between Processors
  Fast Multiplication Schemes

J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)



positive logic: see description

description

The SN74172, containing the equivalent of 201 gates on a monolithic chip, is a high-performance 16-bit register file organized as eight words of two bits each.

Multiple address decoding circuitry is used so that the read and write operation can be performed independently on two word locations. This provides a true simultaneous read/write capability. Basically, the file consists of two distinct sections (see Figure A).

Section 1 permits the writing of data into any two-bit word location while reading two bits of data from another location simultaneously. To provide this flexibility, independent decoding is incorporated.

Section 2 of the register file is similar to section 1 with the exception that common read/write address circuitry is employed. This means that section 2 can be utilized in one of three modes:

1) Writing new data into two bits
2) Reading from two bits
3) Writing into and simultaneously reading from the same two bits.

Regardless of the mode, the operation of section 2 is entirely independent of section 1.

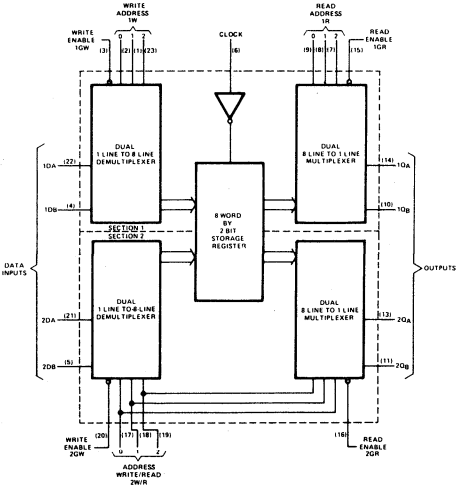


FIGURE A

description (continued)

The three-state outputs of this register file permit connection of up to 129 compatible outputs and one Series 54/74 high-logic-level load to a common system bus. The outputs are controlled by the read-enable circuitry so that they operate as standard TTL totem-pole outputs when the appropriate read-enable input is low or they are placed in a high-impedance state when the associated read-enable input is at a high logic level. To minimize the possibility that two outputs from separate register files will attempt to take a common bus to opposite logic levels, the read-enable circuitry is designed such that disable times are shorter than enable times.

All inputs are buffered to lower the drive requirements of the clock, read/write address, and write-enable inputs to one normalized Series 54/74 load, and of all other inputs to one-half of one normalized Series 54/74 load.

Functions of the inputs and outputs of the SN74172 are as shown in the following table.

FUNCTION	SECTION 1	SECTION 2	DESCRIPTION
Write Address	1W0, 1W1, 1W2	2W/R0, 2W/R1, 2W/R2	Binary write address selects one of eight two-bit word locations.
Write Enable	1GW	2GW	When low, permits the writing of new data into the selected word location on a positive transition of the clock input.
Data Inputs	1DA, 1DB	2DA, 2DB	Data at these inputs is entered on a positive transition of the clock input into the location selected by the write address inputs if the write enable input is low. Since the two sections are independent, it is possible for both write functions to be activated with both write addresses selecting the same word location. If this occurs and the information at the data inputs is not the same for both sections (i.e., 1DA $\neq$ 2DA and/or 1DB $\neq$ 2DB) the low-level data will predominate in each bit and be stored.
Read Address	1R0, 1R1, 1R2	Common with write address	Binary write address selects one of eight two-bit word locations.
Read Enable	1GR	2GR	When read enable is low, the outputs assume the levels of the data stored in the location selected by read address inputs. When read enable is high, the associated outputs remain in the high-impedance state and neither significantly load nor drive the lines to which they are connected.
Data Outputs	$1Q_A$, $1Q_B$	$2Q_A$, $2Q_B$	
Clock	CK		The positive-going transition of the clock input will enter new data into the addressed location if the write enable input is low. The clock is common to both sections.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the high-impedance state.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}				−5.2	mA
Low-level output current, I_{OL}				16	mA
Input clock frequency, f_{clock}		0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			ns
Setup time, t_{setup} (see Figure 1)	Write select	$t_{w(clock)}$+10			ns
	High-level data	30			
	Low-level data	45			
	Write enable	35			
Hold time, t_{hold} (see Figure 1)	Write select	0			ns
	Write enable	0			
Data release time, $t_{release}$ (see Figure 1)	High-level data			10	ns
	Low-level data			10	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

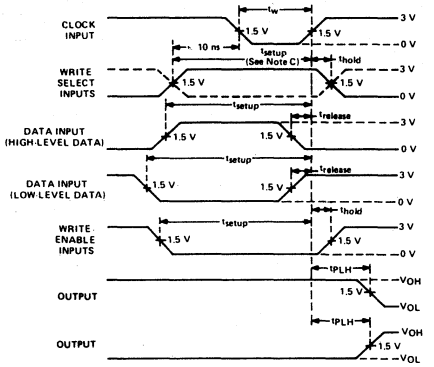
PARAMETER			TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −5.2 mA	2.4	3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4	V
$I_{O(off)}$	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 2.4 V			40	μA
			V_{CC} = MAX, V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	2W/R0, 2W/R1, 2W/R2, 1GW, 2GW, or clock	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
		Any other input				−0.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 4.5 V, Outputs open		112	170	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

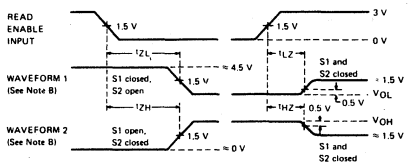
switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, See Figure 1	20			MHz
t_{PLH}	Propagation delay time, low-to-high-level output from read select			33	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output from read select			30	45	
t_{PLH}	Propagation delay time, low-to-high-level output from clock			35	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			35	50	
t_{ZH}	Output enable time to high level			14	30	ns
t_{ZL}	Output enable time to low level			16	30	
t_{HZ}	Output disable time from high level	C_L = 5 pF, See Figure 1		6	20	ns
t_{LZ}	Output disable time from low level			11	20	

PARAMETER MEASUREMENT INFORMATION



SWITCHING TIMES FROM CLOCK INPUT



ENABLE AND DISABLE TIMES FROM READ ENABLE

NOTES: A. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled. Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

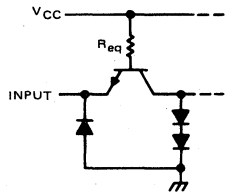
C. Write select setup time, as specified, will protect data written into previous address.

D. Load circuit is shown on page 148.

VOLTAGE WAVEFORMS
FIGURE 1

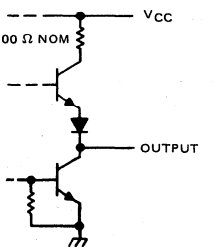
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



2W/R0, 2W/R1, 2W/R2,
1GW, 2GW, or Clock: R_{eq} = 4 kΩ NOM
Other inputs: R_{eq} = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



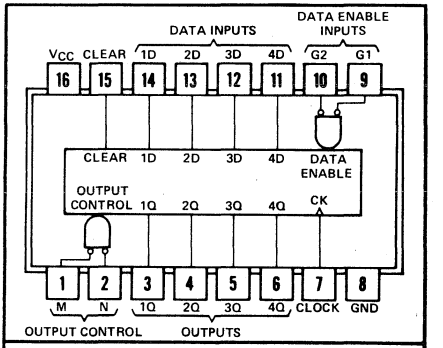
TYPES SN54173, SN74173
4-BIT D-TYPE REGISTERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211721, MAY 1972–REVISED DECEMBER 1972

- Three-State Outputs Interface Directly with System Bus
- Gated Output-Control Lines for Enabling or Disabling the Outputs
- Fully Independent Clock Virtually Eliminates Restrictions for Operating in One of Two Modes:

  Parallel Load
  Do Nothing (Hold)
- Average Propagation Delay . . . 23 ns Typical
- Maximum Clock Frequency . . . 35 MHz Typical
- Power Dissipation . . . 250 mW Typical
- For Application as Bus Buffer Registers

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

The SN54173 and SN74173 four-bit registers include D-type flip-flops featuring totem-pole three-state outputs capable of driving highly capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these flip-flops with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. For applications not requiring three-state outputs, the SN54174 or SN74174 hex D-type flip-flop can be used for a 33% reduction in package count and a 40% reduction in power, or the SN54175 or SN74175 quadruple D-type flip-flop can be used for a similar reduction in power.

FUNCTION TABLE

INPUTS					OUTPUT
CLEAR	CLOCK	DATA ENABLE		DATA	Q
		G1	G2	D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however sequential operation of the flip-flops is not affected.

H = high level (steady state)
L = low level (steady state)
↑ = low-to-high-level transition
X = irrelevant (any input including transitions)
Q_0 = the level of Q before the indicated steady-state input conditions were established.

Gated enable inputs are provided on the SN54173 and SN74173 for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states (high or low levels) of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

Rated at −5.2 mA high-logic-level drive current, up to 128 of the SN74173 outputs may be connected to a common bus and still drive two Series 54/74 TTL normalized loads. Similarly, up to 49 of the SN54173 outputs can be connected to a common bus and drive one additional Series 54/74 TTL load. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times by 10 nanoseconds. The SN54173 and SN74173 are guaranteed to accept clock input frequencies up to 25 MHz.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Output voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54173 Circuits . . . . . −55°C to 125°C
SN74173 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminals.
2. This is the maximum voltage which should be applied to any output when it is in the high-impedance state.

recommended operating conditions

		SN54173			SN74173			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−2			−5.2	mA
Low-level output current, I_{OL}				16			16	mA
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Data enable	17			17			ns
	Data	10			10			
	Clear inactive state	10			10			
Hold time, t_{hold}	Data enable	2			2			ns
	Data	10			10			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			40	μA
			V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−70	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		50	72	mA

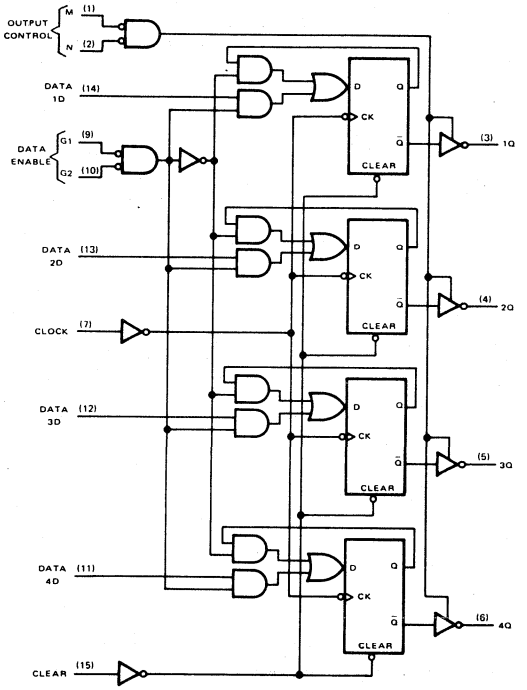
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with all outputs open; clear grounded following momentary connection to 4.5 V; N, G1, G2, and all data inputs grounded; and the clock input and M at 4.5 V.

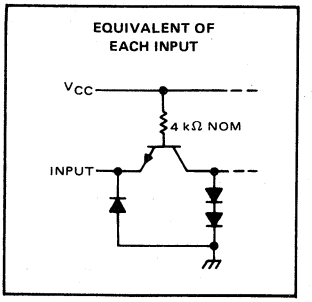
switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 400 Ω

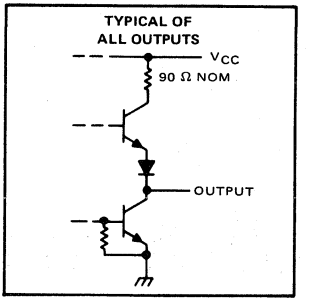
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, See Note 4	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear input			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock input			28	43	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock input			19	31	
t_{ZH}	Output enable time to high level		7	16	30	ns
t_{ZL}	Output enable time to low level		7	21	30	
t_{HZ}	Output disable time from high level	C_L = 5 pF, See Note 4	3	5	14	ns
t_{LZ}	Output disable time from low level		3	11	20	

NOTE 4: Load circuits and voltage waveforms are shown on page 148.

functional block diagram and schematics of inputs and outputs







. . . dynamic input activated by a transition from a high level to a low level.

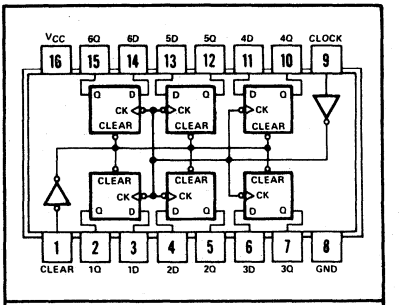
TYPES SN54174, SN54175, SN54LS174, SN54LS175, SN54S174, SN54S175, SN74174, SN74175, SN74LS174, SN74LS175, SN74S174, SN74S175
HEX/QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

BULLETIN NO. DL-S 7211803, DECEMBER 1972

'174, 'LS174, 'S174 . . . HEX D-TYPE FLIP-FLOPS
'175, 'LS175, 'S175 . . . QUADRUPLE D-TYPE FLIP-FLOPS

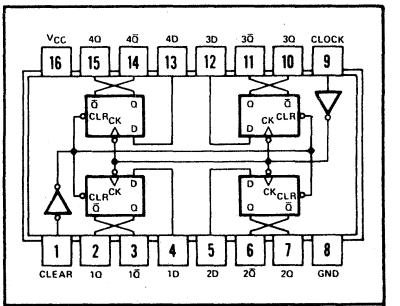
- '174, 'LS174, 'S174 Contain Six Flip-Flops with Single-Rail Outputs
- '175, 'LS175, 'S175 Contain Four Flip-Flops with Double-Rail Outputs
- Three Performance Ranges Offered: See Table Lower Right
- Buffered Clock and Direct Clear Inputs
- Individual Data Input to Each Flip-Flop
- Applications include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators

SN54S174 . . . J OR W PACKAGE
'174, 'LS174, SN74S174 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic: see function table

'175, 'LS175, 'S175 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and 'S175 feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

These circuits are fully compatible for use with most TTL or DTL circuits.

FUNCTION TABLE
(EACH FLIP-FLOP)

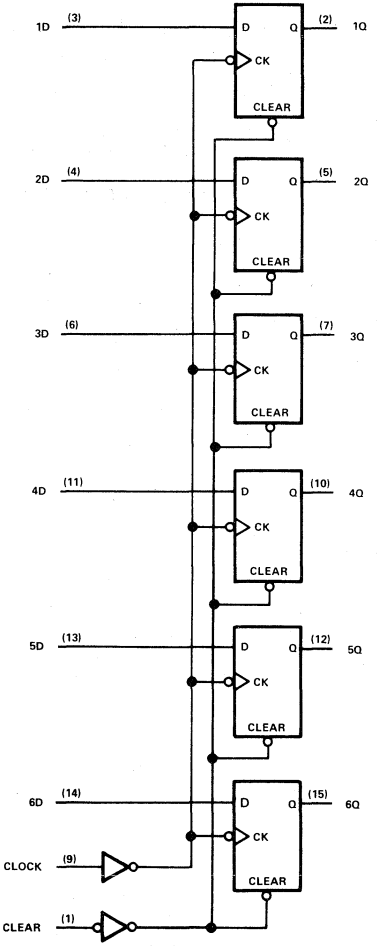
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, and 'S175 only

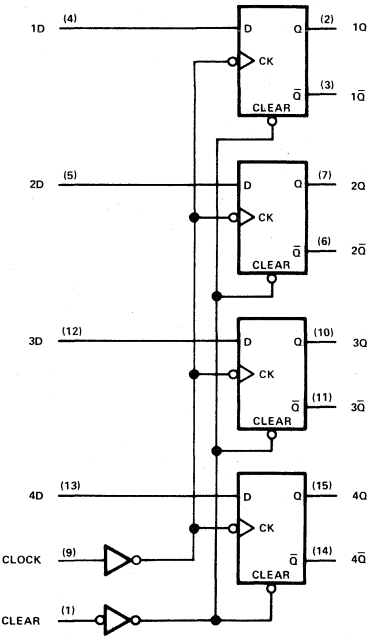
TYPES	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION PER FLIP-FLOP
'174, '175	35 MHz	38 mW
'LS174, 'LS175	40 MHz	11 mW
'S174, 'S175	110 MHz	75 mW

functional block diagrams

'174, 'LS174, 'S174



'175, 'LS175, 'S175

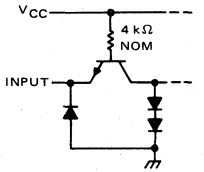


. . . dynamic input activated by transition from a high level to a low level.

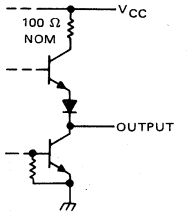
schematics of inputs and outputs

SN54174, SN54175, SN74174, SN74175

EQUIVALENT OF ALL INPUTS

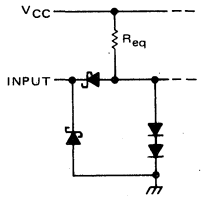


TYPICAL OF ALL OUTPUTS



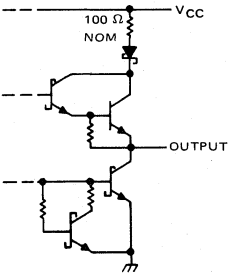
SN54LS174, SN54LS175, SN74LS174, SN74LS175

EQUIVALENT OF ALL INPUTS



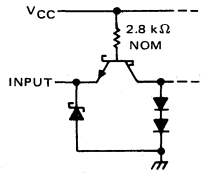
Clock: R_{eq} = 17 kΩ NOM
Clear, D: R_{eq} = 30 kΩ NOM

TYPICAL OF ALL OUTPUTS

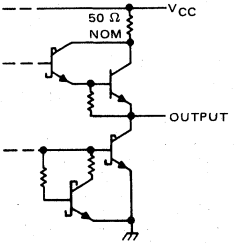


SN54S174, SN54S175, SN74S174, SN74S175

EQUIVALENT OF ALL INPUTS



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54174, SN54175 Circuits . . . . . −55°C to 125°C
SN74174, SN74175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54174, SN54175			SN74174, SN74175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_{hold}		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54'	−20		−57	mA
			SN74'	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'174		45	65	mA
			'175		30	45	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 3	25	35		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear (SN54175, SN74175 only)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS174, SN54LS175 Circuits . . . . . −55°C to 125°C
SN74LS174, SN74LS175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Data input	20			20			ns
	Clear inactive-state	25			25			ns
Data hold time, t_{hold}		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS174 SN54LS175			SN74LS174 SN74LS175			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current, Clock input	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
	Low-level input current, Other inputs					−0.36			−0.36	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'LS174		13	22		13	22	mA
			'LS175		9	15		9	15	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Note 4	30	40		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear (SN54LS175, SN74LS175 only)			16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	30	ns

NOTE 4: Load circuit and voltage waveforms are shown on page 149.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S174, SN54S175 Circuits . . . . . −55°C to 125°C
SN74S174, SN74S175 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S174, SN54S175			SN74S174, SN74S175			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		75	0		75	MHz
Pulse width, t_w	Clock	7			7			ns
	Clear	10			10			
Setup time, t_{setup}	Data input	5			5			ns
	Clear inactive-state	5			5			
Data hold time, t_{hold}		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	'174		90	144	mA
			'175		60	96	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.
NOTE 2: With all outputs open and 4.5 V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5 V, is applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω, See Note 3	75	110		MHz
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output from clear (SN54S175, SN74S175 only)			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			13	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation time, high-to-low-level output from clock			11.5	17	ns

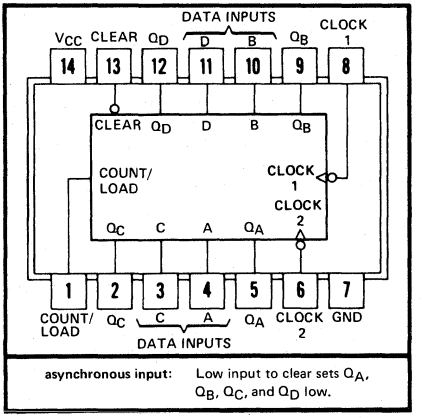
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54176, SN54177, SN74176, SN74177
35-MHz PRESETTABLE DECADE AND BINARY COUNTERS/LATCHES

BULLETIN NO. DL-S 7211478, MAY 1971–REVISED DECEMBER 1972

- Reduced-Power Versions of SN54196, SN54197, SN74196, and SN74197 50-MHz Counters
- D-C Coupled Counters Designed to Replace Signetics 8280, 8281, 8290, and 8291 Counters in Most Applications
- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 35 MHz
- Input Clamping Diodes Simplify System Design

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

3

description

These high-speed monolithic counters consist of four d-c coupled master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54176, SN74176) or a divide-by-two and a divide-by-eight counter (SN54177, SN74177). These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 35 megahertz at the clock-1 input and 0 to 17.5 megahertz at the clock-2 input. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. The circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 150 milliwatts. The SN54176 and SN54177 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74176 and SN74177 circuits are characterized for operation from 0°C to 70°C.

typical count configurations

SN54176 and SN74176

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence function table shown at right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary function table.

SN54176, SN74176
FUNCTION TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

H = high level, L = low level

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54177 and SN74177

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, and Q_D outputs as shown in the function table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

SN54177, SN74177
FUNCTION TABLE
(See Note A)

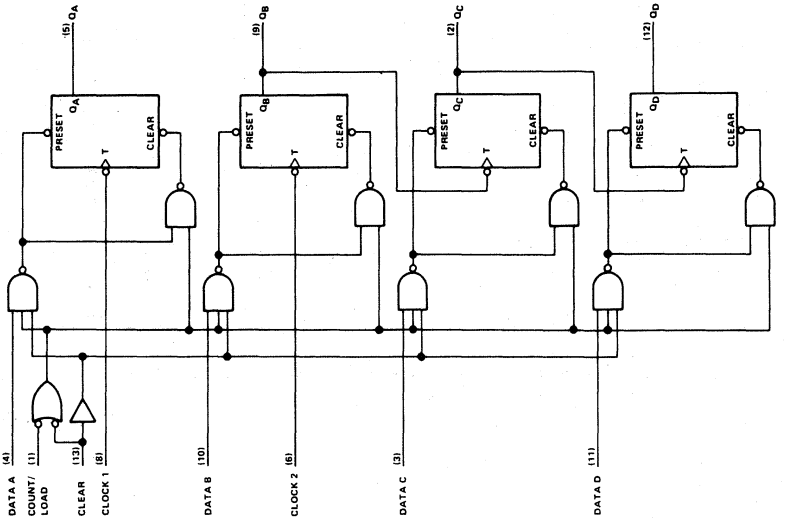
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = high level, L = low level

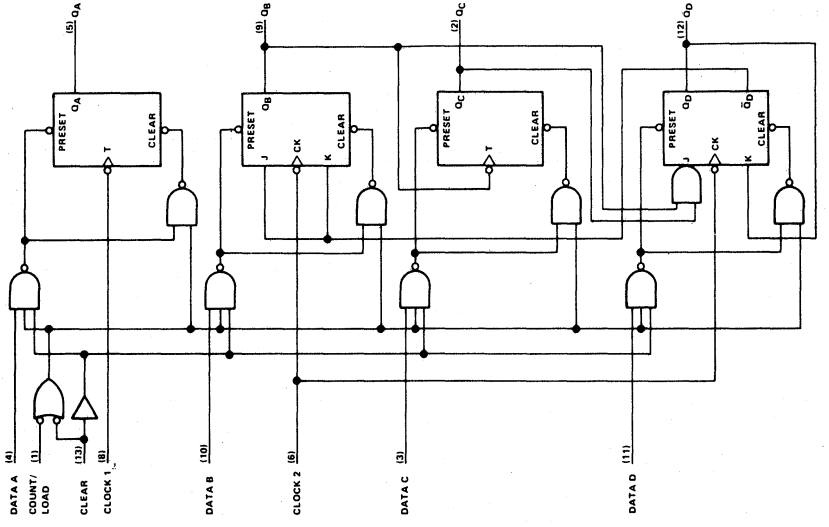
NOTE A: Output Q_A connected to clock-2 input.

functional block diagrams

SN54177, SN74177



SN54176, SN74176

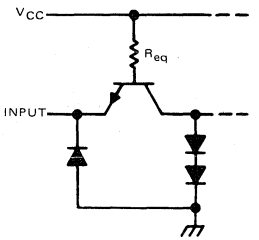


. . . dynamic input activated by transition from a high level to a low level

3

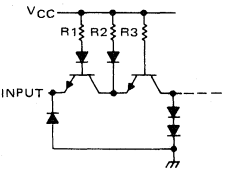
schematics of inputs and outputs

EQUIVALENT OF COUNT/LOAD, CLEAR, AND DATA INPUTS



Data, Count/load: R_{eq} = 4 kΩ NOM
Clear: R_{eq} = 2 kΩ NOM

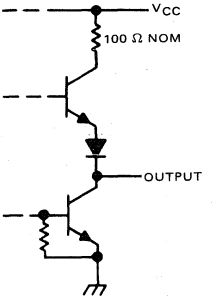
EQUIVALENT OF CLOCK INPUTS



NOMINAL VALUES OF R1, R2, and R3

INPUT	'176	'177
Clock 1	4 kΩ	4 kΩ
Clock 2	4 kΩ	6 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54176, SN54177 Circuits . . . . . −55°C to 125°C
SN74176, SN74177 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54'	4.5	5	5.5	V
	SN74'	4.75	5	5.25	
High-level output current, I_{OH}				−800	μA
Low-level output current, I_{OL}				16	mA
Count frequency (see Figure 1)	Clock-1 input	0		35	MHz
	Clock-2 input	0		17.5	
Pulse width, t_w (see Figure 1)	Clock-1 input	14			ns
	Clock-2 input	28			
	Clear	20			
	Load	25			
Input hold time, t_{hold} (see Figure 1)	High-level data	$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			
Input setup time, t_{setup} (see Figure 1)	High-level data	15			ns
	Low-level data	20			
Count enable time, t_{enable} (see Note 3 and Figure 1)		25			ns
Operating free-air temperature, T_A	SN54'	−55		125	°C
	SN74'	0		70	

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54176, SN74176			SN54177, SN74177			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Clear, clock 1					80			80	
		Clock 2					120			80	
I_{IL}	Low-level input current	Data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		Clear					−3.2			−3.2	
		Clock 1					−4.8			−4.8	
		Clock 2					−4.8			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			30	48		30	48	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock 2 input. This permits driving the clock 2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, see figure 1

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	SN54176, SN74176			SN54177, SN74177			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	35	50		35	50		MHz
t_{PLH}	Clock 1	Q_A		8	13		8	13	ns
t_{PHL}				11	17		11	17	
t_{PLH}	Clock 2	Q_B		11	17		11	17	ns
t_{PHL}				17	26		17	26	
t_{PLH}	Clock 2	Q_C		27	41		27	41	ns
t_{PHL}				34	51		34	51	
t_{PLH}	Clock 2	Q_D		13	20		44	66	ns
t_{PHL}				17	26		50	75	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		19	29		19	29	ns
t_{PHL}				31	46		31	46	
t_{PLH}	Load	Any		29	43		29	43	ns
t_{PHL}				32	48		32	48	
t_{PHL}	Clear	Any		32	48		32	48	ns

◇f_{max} ≡ maximum input count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION

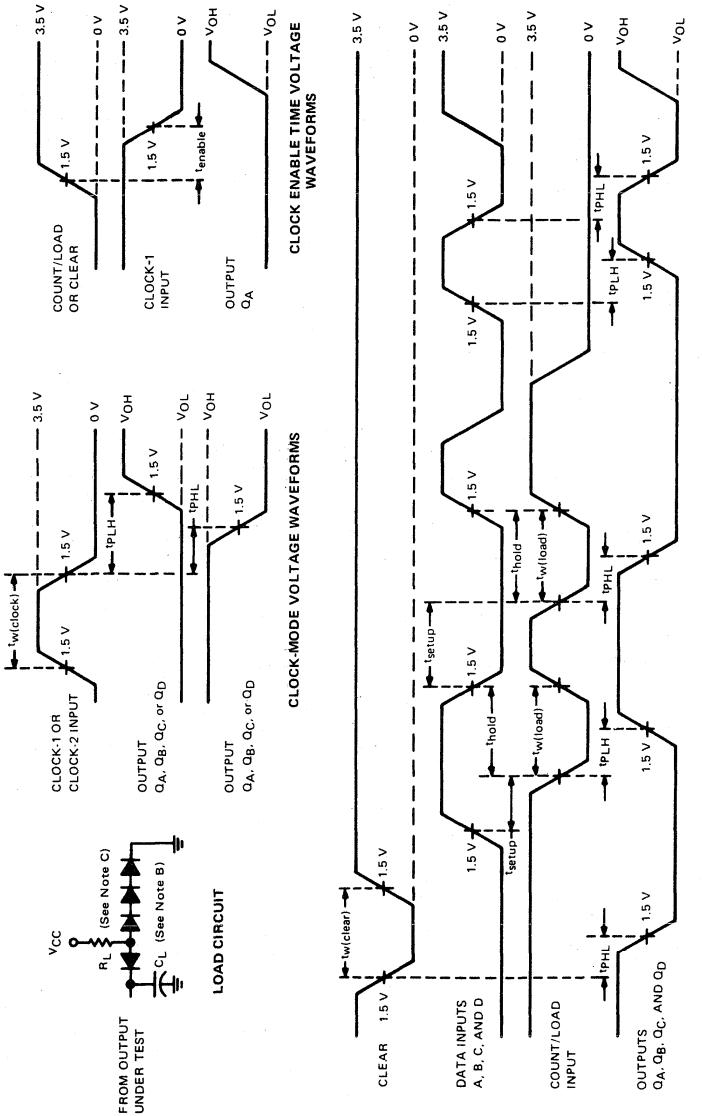


FIGURE 1

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, duty cycle ⩽ 50%, $t_r < 5$ ns, and unless specified, $t_f < 5$ ns. When testing f_{max}, vary PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Unless otherwise specified, Q_A is connected to clock 2.

TYPES SN54178, SN54179, SN74178, SN74179
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7211846, DECEMBER 1972

- **Typical Maximum Clock Frequency . . . 39 MHz**
- **Three Operating Modes:**
  - **Synchronous Parallel Load**
  - **Right Shift**
  - **Hold (Do Nothing)**
- **Negative-Edge-Triggered Clocking**
- **D-C Coupling Symplifies System Designs**

description

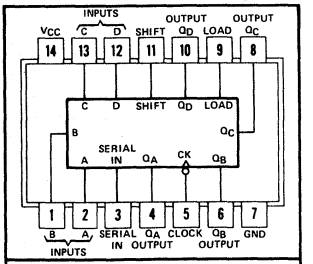
These shift registers utilize fully d-c coupled storage elements and feature synchronous parallel inputs and parallel outputs. The SN54179/SN74179 has a direct clear line and complementary output from the D flip-flop, thereby differing from the SN54178/SN74178.

Parallel loading is accomplished by taking the shift input low, applying the four bits of data, and taking the load input high. The data is loaded into the associated flip-flop synchronously and appears at the outputs after a high-to-low transition of the clock. During loading, serial data flow is inhibited.

Shift right is also accomplished on the falling edge of the clock pulse when the shift input is high regardless of the level of the load input. Serial data for this mode is entered at the serial data input.

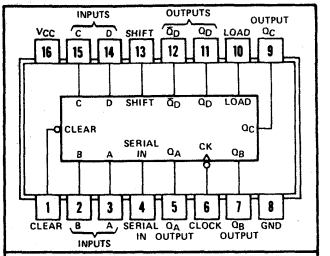
When both the shift and load inputs are low, clocking of the register can continue; however, data appearing at each output is fed back to the flip-flop input creating a mode in which the data is held unchanged. Thus, the system clock may be left free-running without changing the contents of the register.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)
SN54178, SN74178



positive logic: see function table

SN54179, SN74179



positive logic: see function table

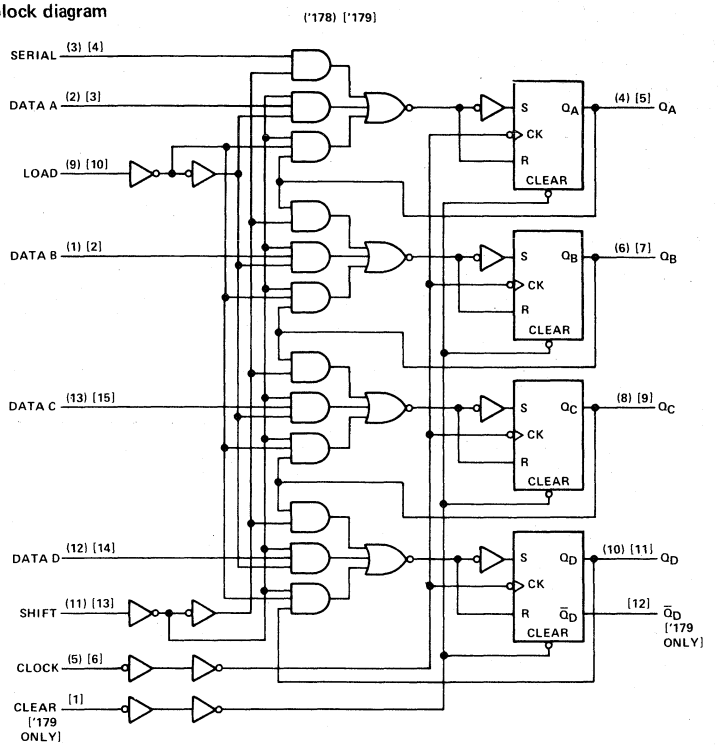
'178, '179†
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR†	SHIFT	LOAD	CLOCK	SERIAL	PARALLEL A	PARALLEL B	PARALLEL C	PARALLEL D	Q_A	Q_B	Q_C	Q_D	$\bar{Q}_D$†
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	X	X	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\bar{Q}_{D0}$
H	L	L	↓	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\bar{Q}_{D0}$
H	L	H	↓	X	a	b	c	d	a	b	c	d	$\bar{d}$
H	H	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$
H	H	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\bar{Q}_{Cn}$

†The columns for clear, $\bar{Q}_D$, and the top line of the table apply for the '179 only.

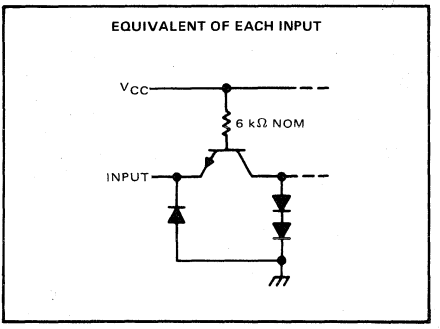
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↓ transition of the clock.

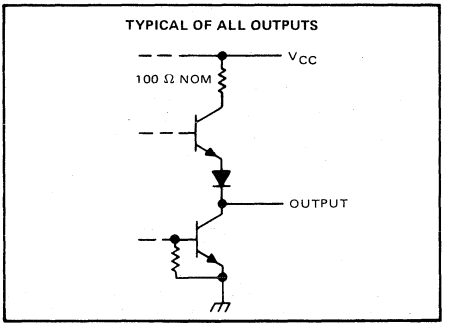
functional block diagram



. . . Denotes input activated by a transition from a high level to a low level.

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54178, SN54179 Circuits . . . . . −55°C to 125°C
SN74178, SN74179 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54178, SN54179			SN74178, SN74179			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)		20			20			ns
Setup time, t_{setup} (see Figure 1)	Shift (H or L) or load	35			35			ns
	Data	30			30			
	Clear-inactive-state (SN54179 and SN74179)	15			15			
Hold time at any input, t_{hold}		5			5			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54178, SN54179			SN74178, SN74179			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		46	70		46	75	mA

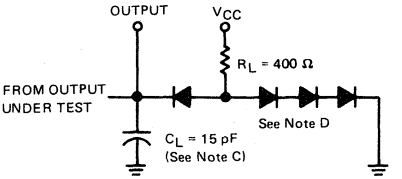
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured as follows:
a) 4.5 V is applied to serial inputs, load, shift, and clear,
b) Parallel inputs A through D are gounded,
c) 4.5 V is momentarily applied to clock which is then grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

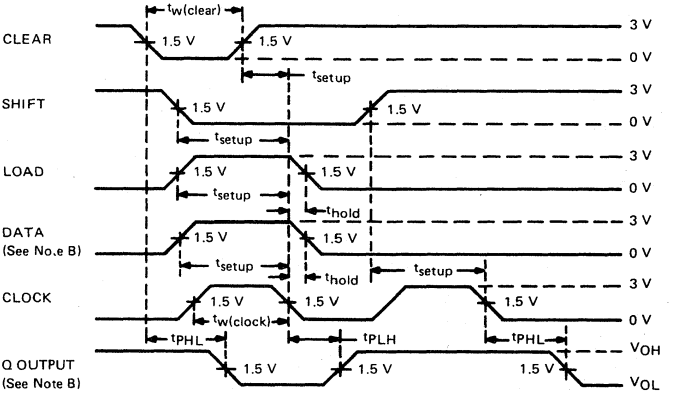
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	39		MHz
t_{PLH}	Clear	$\overline{Q}_D$			15	23	ns
t_{PHL}		Q_A, Q_B, Q_C, Q_D			24	36	
t_{PLH}	Clock	Any output			17	26	ns
t_{PHL}					23	35	

¶ f_{max} ≡ Maximum input clock frequency
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PLH} ≡ Propagation delay time, low-to-high-level output

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_{TLH} \leq 10$ ns, $t_{THL} \leq 10$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. Data input and Q output are any related pair. Serial and other data inputs are at GND. Serial data input is tested in conjunction with Q_A output in the shift mode.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

FIGURE 1–SWITCHING TIMES

TYPES SN54180, SN74180
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7211814, DECEMBER 1972

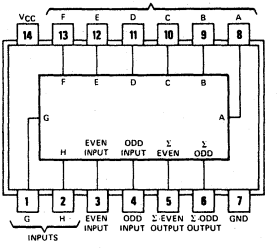
logic

FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF H's AT A THRU H	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = high level, L = low level, X = irrelevant

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These universal, monolithic, 9-bit (8 data bits plus 1 parity bit) parity generators/checkers, utilize familiar Series 54/74 TTL circuitry and feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

The SN54180/SN74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54180 Circuits . . . . . −55°C to 125°C
SN74180 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54180			SN74180			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54180			SN74180			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.3		2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Any data input	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Even or odd input				80			80	
I_{IL}	Low-level input current	Any data input	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Even or odd input				−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2		34	49		34	56	mA

NOTE 2: I_{CC} is measured with even and odd inputs at 4.5 V, all other inputs and outputs open.
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

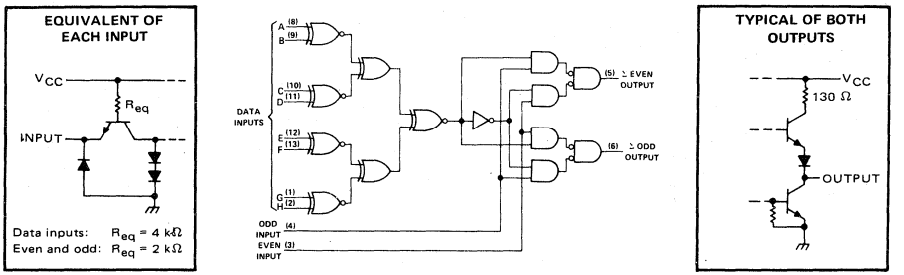
3

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 400 Ω, Odd input grounded, See Note 3		40	60	ns
t_{PHL}					45	68	
t_{PLH}	Data	Σ Odd			32	48	ns
t_{PHL}					25	38	
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 400 Ω, Even input grounded, See Note 3		32	48	ns
t_{PHL}					25	38	
t_{PLH}	Data	Σ Odd			40	60	ns
t_{PHL}					45	68	
t_{PLH}	Even or Odd	Σ Even or Σ Odd	C_L = 15 pF, R_L = 400 Ω, See Note 3		13	20	ns
t_{PHL}					7	10	

NOTE 3: Load circuits and waveforms are shown on page 148.
¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

functional block diagram



TEXAS INSTRUMENTS

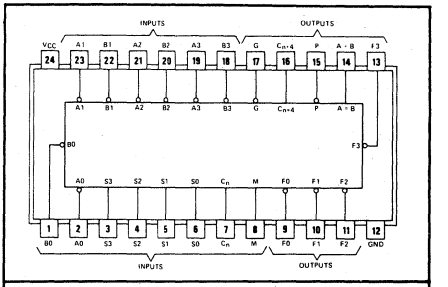
TYPES SN54181, SN54LS181, SN54S181, SN74181, SN74LS181, SN74S181
ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

BULLETIN NO. DL-S 7211831, DECEMBER 1972

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

'181, 'LS181 . . . J, N, OR W PACKAGE
SN54S181 . . . J OR W PACKAGE
SN74S181 . . . J, N, OR W PACKAGE
(TOP VIEW)



logic: see tables 1 and 2

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

TYPICAL ADDITION TIMES

NUMBER OF BITS	ADDITION TIMES USING '181 AND '182	ADDITION TIMES USING 'LS181 AND '182	ADDITION TIMES USING 'S181 AND 'S182	PACKAGE COUNT ARITHMETIC/ LOGIC UNITS	PACKAGE COUNT LOOK-AHEAD CARRY GENERATORS	CARRY METHOD BETWEEN ALU's
1 to 4	24 ns	24 ns	11 ns	1		NONE
5 to 8	36 ns	40 ns	18 ns	2		RIPPLE
9 to 16	36 ns	44 ns	19 ns	3 or 4	1	FULL LOOK-AHEAD
17 to 64	60 ns	68 ns	28 ns	5 to 16	2 to 5	FULL LOOK-AHEAD

description

The '181, 'LS181, and 'S181 are arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made

description (continued)

available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the SN54182, SN54S182, SN74182, or SN74S182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown above illustrate the little additional time required for addition of longer words when full carry look-ahead is employed. The method of cascading '182 or 'S182 circuits with these ALU's to provide multi-level full carry look ahead is illustrated under typical applications data for the '182 and 'S182.

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The '181, 'LS181 and 'S181 will accommodate active-high or active-low data if the pin designations are interpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	$\overline{Y}$
Active-low data (Table II)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

3

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1 which requires an end-around or forced carry to provide A−B.

The '181, 'LS181 or 'S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that is can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-HIGH DATA (FIGURE 1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A ≤ B	A ≥ B
H	L	A > B	A < B
L	H	A < B	A > B
L	L	A ≥ B	A ≤ B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

Series 54, 54LS, and 54S devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, 74LS, and 74S devices are characterized for operation from 0°C to 70°C.

description (continued)

ALU Signal Designations

The '181, 'LS181, and 'S181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

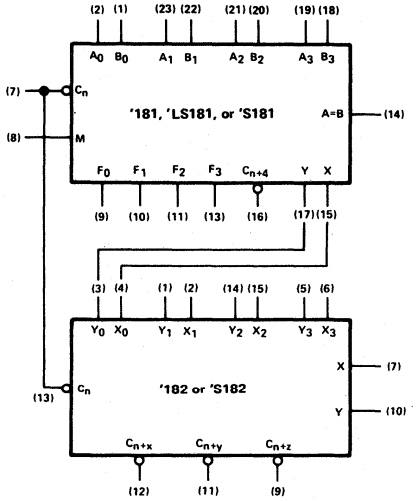


FIGURE 1
(FOR TABLE 1)

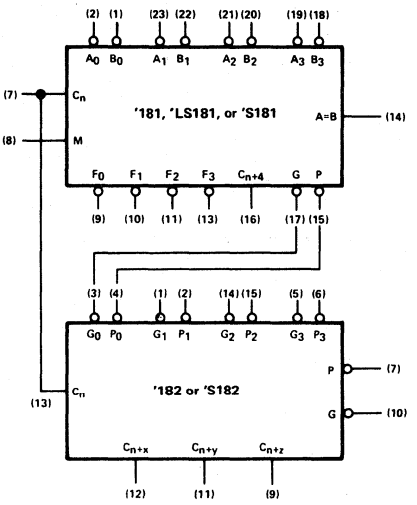


FIGURE 2
(FOR TABLE 2)

TABLE 1

SELECTION	M = H	ACTIVE-HIGH DATA M = L: ARITHMETIC OPERATIONS	
S3 S2 S1 S0	LOGIC FUNCTIONS	C_n = H (no carry)	C_n = L (with carry)
L L L L	F = $\overline{A}$	F = A	F = A PLUS 1
L L L H	F = $\overline{A+B}$	F = A + B	F = (A + B) PLUS 1
L L H L	F = $A\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	F = $\overline{AB}$	F = A PLUS A$\overline{B}$	F = A PLUS A$\overline{B}$ PLUS 1
L H L H	F = $\overline{B}$	F = (A + B) PLUS A$\overline{B}$	F = (A + B) PLUS A$\overline{B}$ PLUS 1
L H H L	F = A ⊕ B	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A$\overline{B}$	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
H L L L	F = $\overline{A}$ + B	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	F = $\overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A + $\overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

TABLE 2

SELECTION	M = H	ACTIVE-LOW DATA M = L: ARITHMETIC OPERATIONS	
S3 S2 S1 S0	LOGIC FUNCTIONS	C_n = L (no carry)	C_n = H (with carry)
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	F = $\overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A}$ + B	F = A$\overline{B}$ MINUS 1	F = A$\overline{B}$
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	F = $\overline{A+B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	F = $\overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{A}$B	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	F = A ⊕ B	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = A$\overline{B}$ PLUS (A + B)	F = A$\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = A$\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = A$\overline{B}$ PLUS A	F = A$\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54181 . . . . . −55°C to 125°C
SN74181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54181			SN74181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54181			SN74181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		Any A or B input					120			120	
		Any S input					160			160	
		Carry input					200			200	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		Any A or B input					−4.8			−4.8	
		Any S input					−6.4			−6.4	
		Carry input					−8			−8	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−20		−55	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		88	127		88	140	mA
				Condition B		94	135		94	150	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

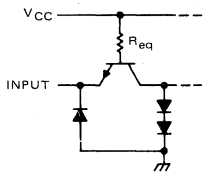
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 400 Ω, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			12	18	ns
t_{PHL}					13	19	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		28	43	ns
t_{PHL}					27	41	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		35	50	ns
t_{PHL}					33	50	
t_{PLH}	C_n	Any F	M = 0 V (SUM or DIFF mode)		13	19	ns
t_{PHL}					12	18	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		13	19	ns
t_{PHL}					13	19	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		17	25	ns
t_{PHL}					17	25	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		13	19	ns
t_{PHL}					17	25	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		17	25	ns
t_{PHL}					17	25	
t_{PLH}	A_i or B_i	F_i	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V (SUM mode)		28	42	ns
t_{PHL}					21	32	
t_{PLH}	A_i or B_i	F_i	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	A_i or B_i	F_i	M = 4.5 V (logic mode)		32	48	ns
t_{PHL}					23	34	
t_{PLH}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V (DIFF mode)		35	50	ns
t_{PHL}					32	48	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

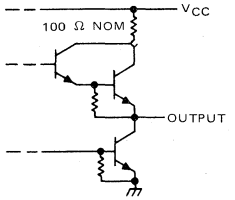
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

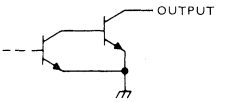


Mode control: R_{eq} = 4 kΩ NOM
Any A or B: R_{eq} = 2 kΩ NOM
Any S: R_{eq} = 1.3 kΩ NOM
C_n: R_{eq} = 1 kΩ NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



absolute maximum ratings over recommended operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS181 . . . . . −55°C to 125°C
SN74LS181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54LS181			SN74LS181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS181			SN74LS181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V				100			100	μA
V_{OL}	Low-level output voltage	All outputs	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
				I_{OL} = 8 mA					0.35	0.5	
		Output G		I_{OL} = 16 mA		0.47	0.7		0.47	0.7	
		Output P		I_{OL} = 8 mA		0.35	0.6		0.35	0.5	
I_I	Input current at max. input voltage	Mode input	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
		Any A or B input					0.3			0.3	
		Any S input					0.4			0.4	
		Carry input					0.5			0.5	
I_{IH}	High-level input current	Mode input	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
		Any A or B input					60			60	
		Any S input					80			80	
		Carry input					100			100	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX, V_I = 0.4 V				−0.36			−0.36	mA
		Any A or B input					−1.08			−1.08	
		Any S input					−1.44			−1.44	
		Carry input					−2			−2	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition A		20	32		20	34	mA
				Condition B		21	35		21	37	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: With outputs open, I_{CC} is measured for the following conditions:
A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded.
B. S0 through S3 and M are at 4.5 V, all other inputs are grounded.

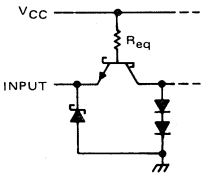
switching characteristics, V_{CC} = 5 V, T_A = 25°C, (C_L = 15 pF, R_L = 2 kΩ, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			18	27	ns
t_{PHL}					13	20	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		25	38	ns
t_{PHL}					25	38	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = S3 = 0 V S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		27	41	ns
t_{PHL}					27	41	
t_{PLH}	C_n	Any F	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		17	26	ns
t_{PHL}					13	20	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		19	29	ns
t_{PHL}					15	23	
t_{PLH}	Any A or B	G	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		21	32	ns
t_{PHL}					17	26	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V, ($\overline{SUM}$ mode)		20	30	ns
t_{PHL}					20	30	
t_{PLH}	Any A or B	P	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		20	30	ns
t_{PHL}					22	33	
t_{PLH}	A_i or B_i	F_i	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		21	32	ns
t_{PHL}					13	20	
t_{PLH}	A_i or B_i	F_i	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		21	32	ns
t_{PHL}					15	23	
t_{PLH}	A_i or B_i	F_i	M = 4.5 V (logic mode)		22	33	ns
t_{PHL}					19	29	
t_{PLH}	Any A or B	A = B	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		33	50	ns
t_{PHL}					41	62	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 149.

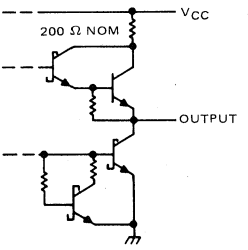
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

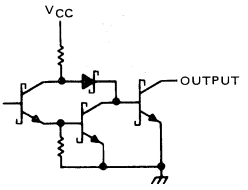


Mode control: R_{eq} = 17 kΩ NOM
Any A or B: R_{eq} = 5.67 kΩ NOM
Any S: R_{eq} = 4.25 kΩ NOM
C_n: R_{eq} = 2.86 kΩ NOM

TYPICAL OF ALL OUTPUTS EXCEPT A = B



A = B OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature: SN54S181 . . . . . −55°C to 125°C
SN74S181 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

	SN54S181			SN74S181			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH} (All outputs except A = B)			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S181			SN74S181			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage, any output except A = B		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
I_{OH}	High-level output current, A = B output only		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Mode input	V_{CC} = MAX,	V_I = 2.4 V			50			50	μA
		Any A or B input					150			150	
		Any S input					200			200	
		Carry input					250			250	
I_{IL}	Low-level input current	Mode input	V_{CC} = MAX,	V_I = 0.4 V			−2			−2	mA
		Any A or B input					−6			−6	
		Any S input					−8			−8	
		Carry input					−10			−10	
I_{OS}	Short-circuit output current, any output except A = B§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	T_A = 125°C, W package only			159				mA
			V_{CC} = MAX,	See Note 3, All packages		120	220		120	220	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured for the following conditions (the typical and maximum values apply to both):
A. S0 through S3, M, and A inputs are at 4.5 V, all other inputs are grounded, and all outputs are open.
B. S0 through S3 and M are at 4.5 V, all other inputs grounded, and all outputs are open.

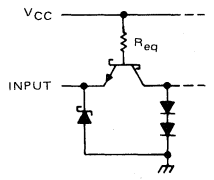
switching characteristics, V_{CC} = 5 V, T_A = 25°C (C_L = 15 pF, R_L = 280 Ω, see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}			7	10.5	ns
t_{PHL}					7	10.5	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		12.5	18.5	ns
t_{PHL}					12.5	18.5	
t_{PLH}	Any A or B	C_{n+4}	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15.5	23	ns
t_{PHL}					15.5	23	
t_{PLH}	C_n	Any F	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		7	12	ns
t_{PHL}					7	12	
t_{PLH}	Any A or B	G	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		8	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any A or B	G	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	Any A or B	P	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		7.5	12	ns
t_{PHL}					7.5	12	
t_{PLH}	Any A or B	P	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		10.5	15	ns
t_{PHL}					10.5	15	
t_{PLH}	A_i or B_i	F_i	M = 0 V, S0 = $\overline{S3}$ = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		11	16.5	ns
t_{PHL}					11	16.5	
t_{PLH}	A_i or B_i	F_i	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	A_i or B_i	F_i	M = 4.5 V (logic mode)		14	20	ns
t_{PHL}					14	22	
t_{PLH}	Any A or B	A = B	M = 0 V, S0 = $\overline{S3}$ = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		15	23	ns
t_{PHL}					20	30	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

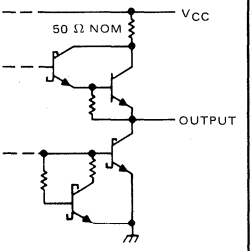
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT

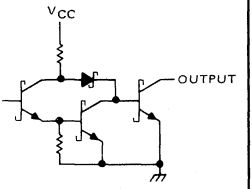


Mode control: R_{eq} = 2.8 kΩ NOM
Any A or B: R_{eq} = 940 Ω NOM
Any S: R_{eq} = 700 Ω NOM
C_n: R_{eq} = 560 Ω NOM

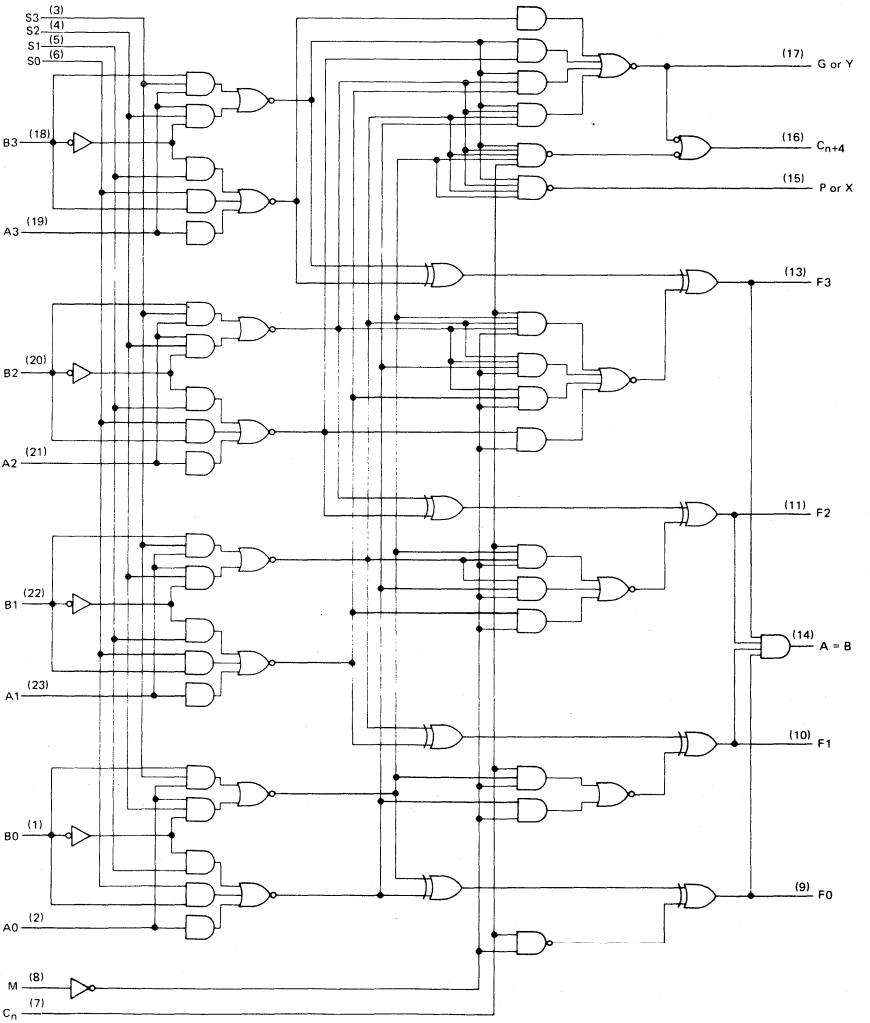
TYPICAL OF ALL OUTPUTS
EXCEPT A = B



A = B OUTPUT



functional block diagram



PARAMETER MEASUREMENT INFORMATION

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A	All B	Any F or C_{n+4}	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_{n+4}	Out-of-Phase

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A and B	None	C_{n+4} or any F	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_{n+4}	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_{n+4}	In-Phase

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = M = 4.5 V, S0 = S3 = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM (See Note 4)
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

NOTE 4: Load circuit and voltage waveforms are shown on pages 148 and 149.

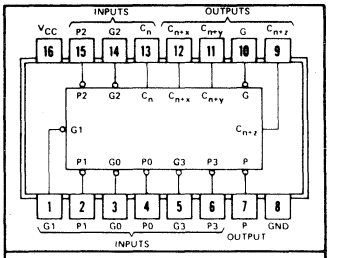
TYPES SN54182, SN54S182, SN74182, SN74S182
LOOK-AHEAD CARRY GENERATORS

BULLETIN NO. DL-S 7211823, DECEMBER 1972

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



logic: see description

TYPE	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'182	13 ns	180 mW
'S182	7 ns	260 mW

3

description

The SN54182, SN54S182, SN74182, and SN74S182 are high-speed, look-ahead carry generators capable of anticipating a carry across four binary adders or group of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

When used in conjunction with the '181, 'LS181, or 'S181 arithmetic logic unit (ALU), these generators provide high-speed carry look-ahead capability for any word length. Each '182 or 'S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading '182 or 'S182 circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the '181, 'LS181, and 'S181 ALU's are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the '181, 'LS181, and 'S181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the '182 and 'S182 are:

$$C_{n+x} = \overline{G}_0 + \overline{P}_0\, C_n$$
$$C_{n+y} = \overline{G}_1 + \overline{P}_1\, \overline{G}_0 + \overline{P}_1\, \overline{P}_0\, C_n$$
$$C_{n+z} = \overline{G}_2 + \overline{P}_2\, \overline{G}_1 + \overline{P}_2\, \overline{P}_1\, \overline{G}_0 + \overline{P}_2\, \overline{P}_1\, \overline{P}_0\, C_n$$
$$\overline{G} = \overline{G}_3\,(\overline{P}_3 + \overline{G}_2)\,(\overline{P}_3 + \overline{P}_2 + \overline{G}_1)\,(\overline{P}_3 + \overline{P}_2 + \overline{P}_1 + \overline{G}_0)$$
$$\overline{P} = \overline{P}_3\, \overline{P}_2\, \overline{P}_1\, \overline{P}_0$$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54', SN54S' Circuits . . . . . −55°C to 125°C
SN74', SN74S' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor. For these circuits, this rating applies to each G input in conjunction with any other G input or in conjunction with any P input.

recommended operating conditions

	SN54182			SN74182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54182			SN74182			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	C_n input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		P3 input				120			120	
		P2 input				160			160	
		P0, P1, or G3 input				200			200	
		G0 or G2 input				360			360	
		G1 input				400			400	
I_{IL}	Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		P3 input				−4.8			−4.8	
		P2 input				−6.4			−6.4	
		P0, P1, or G3 input				−8			−8	
		G0 or G2 input				−14.4			−14.4	
		G1 input				−16			−16	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5 V, See Note 3		27			27		mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		45	65		45	72	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5 V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open; inputs G0, G1, and G2 at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Note 5		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	22	ns

NOTE 5: Load circuit and voltage waveforms are shown on page 148.

recommended operating conditions

	SN54S182			SN74S182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN54S182			SN74S182			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	C_n input	V_{CC} = MAX, V_I = 2.7 V			50			50	μA
		P3 input				100			100	
		P2 input				150			150	
		P0, P1, or G3 input				200			200	
		G0 or G2 input				350			350	
		G1 input				400			400	
I_{IL}	Low-level input current	C_n input	V_{CC} = MAX, V_I = 0.5 V			−2			−2	mA
		P3 input				−4			−4	
		P2 input				−6			−6	
		P0, P1, or G3 input				−8			−8	
		G0 or G2 input				−14			−14	
		G1 input				−16			−16	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−40		−100	−40		−100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = 5 V, See Note 3		35			35		mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		69	99		69	109	mA

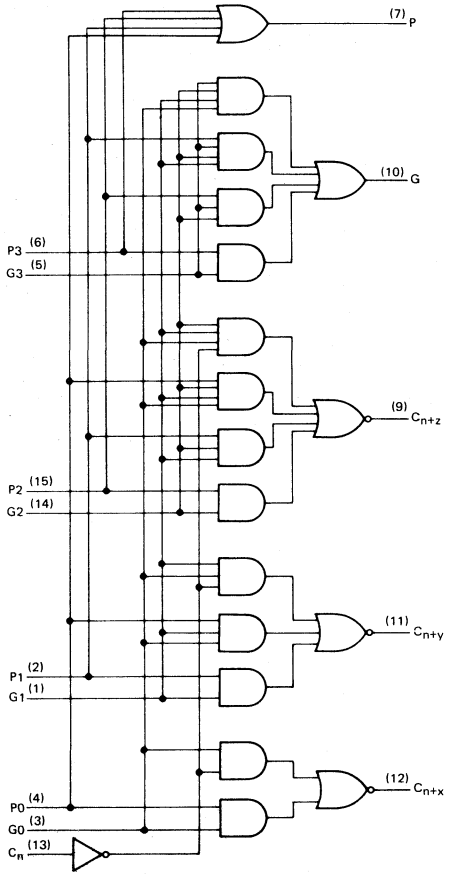
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTES: 3. I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5 V, and all other inputs grounded.
4. I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5 V; and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	G0, G1, G2, G3, P0, P1, P2, or P3	C_{n+x}, C_{n+y}, or C_{n+z}	R_L = 280 Ω, C_L = 15 pF, See Note 5		4.5	7	ns
t_{PHL}					4.5	7	
t_{PLH}	G0, G1, G2, G3, P1, P2, or P3	G			5	7.5	ns
t_{PHL}					7	10.5	
t_{PLH}	P0, P1, P2, or P3	P			4.5	6.5	ns
t_{PHL}					6.5	10	
t_{PLH}	C_n	C_{n+x}, C_{n+y}, or C_{n+z}			6.5	10	ns
t_{PHL}					7	10.5	

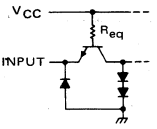
¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 5: Load circuit and voltage waveforms are shown on page 148.

functional block diagram and schematics of inputs and outputs



'182

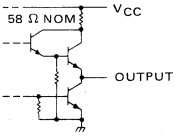
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
C_n	2.8 kΩ
P3	1.4 kΩ
P2	940 Ω
P0, P1, G3	700 Ω
G0, G4	400 Ω
G1	350 Ω

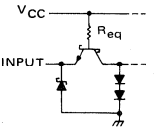
'182

TYPICAL OF ALL OUTPUTS



'S182

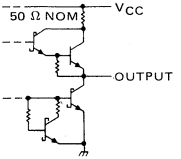
EQUIVALENT OF EACH INPUT



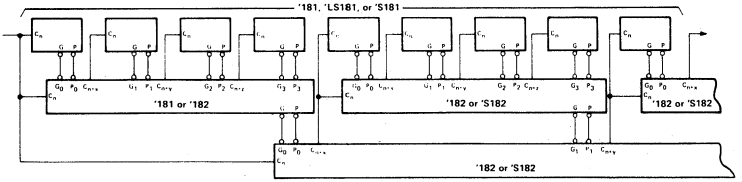
INPUT	R_{eq} NOM
C_n	2.8 kΩ
P3	1.4 kΩ
P2	940 Ω
P0, P1, G3	700 Ω
G0, G4	400 Ω
G1	350 Ω

'S182

TYPICAL OF ALL OUTPUTS



TYPICAL APPLICATION DATA



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

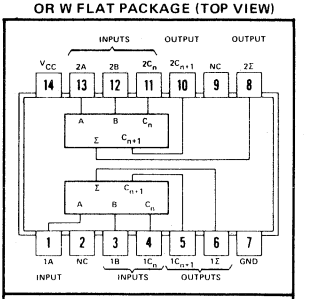
A and B inputs and F outputs of '181, 'LS181, and 'S181 are not shown.

TYPES SN54H183, SN74H183
DUAL CARRY-SAVE FULL ADDERS

BULLETIN NO. DL-S 7211848, DECEMBER 1972

- For Use in High-Speed Wallace-Tree Summing Networks
- Sum and Carry Propagation Delays Both Average Typically 11 ns
- High-Speed, High-Fan-Out Darlington Outputs
- Input Clamping Diodes Simplify System Design
- Compatible with Most TTL and DTL Circuits
- Typical Power Dissipation . . . 110 mW per Bit

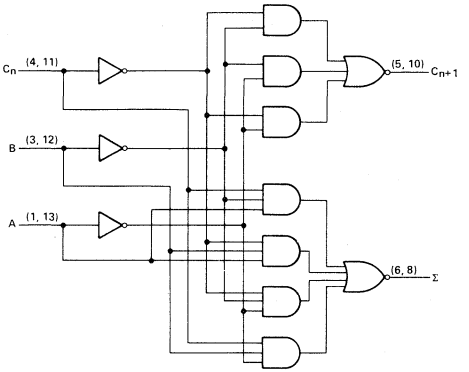
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC—No internal connection

functional block diagram (each adder)

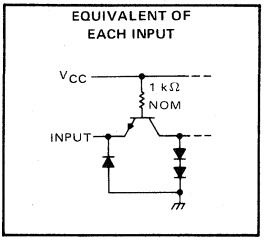


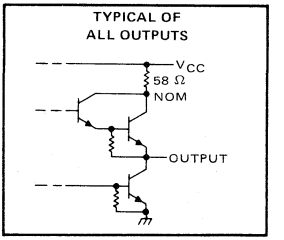
FUNCTION TABLE
(EACH ADDER)

INPUTS			OUTPUTS	
C_n	B	A	Σ	C_{n+1}
L	L	L	L	L
L	L	H	H	L
L	H	L	H	L
L	H	H	L	H
H	L	L	H	L
H	L	H	L	H
H	H	L	L	H
H	H	H	H	H

H = high level, L = low level

schematics of inputs and outputs





description

These dual full adders feature an individual carry output from each bit for use in multiple-input, carry-save techniques to produce the true sum and true carry outputs with no more than two levels of logic. The circuit utilizes high-speed, high-fan-out, transistor-transistor logic (TTL), but is compatible with both DTL and TTL families. Typical average sum and carry propagation delay times are 11 nanoseconds each. Typical power dissipation is 110 milliwatts per bit. The SN54H183 is characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74H183 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54H183 Circuits . . . . . −55°C to 125°C
SN74H183 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between any two inputs to the same adder.

recommended operating conditions

	SN54H183			SN74H183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA		2.4	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				150	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX, See Note 3	SN54H183		48	69	mA
			SN74H183		48	75	
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX, See Note 4			40		mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTES: 3. I_{CCL} is measured with all outputs open and all inputs grounded.
4. I_{CCH} is measured with all outputs open and all outputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 25 pF, R_L = 280 Ω, See Note 5		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	18	ns

NOTE 5: Load circuit and waveforms are shown on page 148.

TYPES SN54184, SN54185A, SN74184, SN74185A
BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

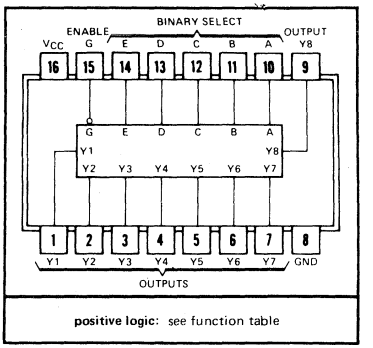
BULLETIN NO. DL-S 7211392, FEBRUARY 1971 – REVISED DECEMBER 1972

SN54184, SN74184 BCD-TO-BINARY CONVERTERS
SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the function tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the '185A and all "don't care" conditions of the '184 are programmed high. The outputs are of the open-collector type.

The SN54184 and SN54185A are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

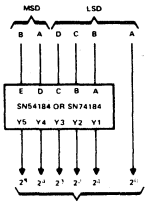
a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

TABLE I
SN54184, SN74184
PACKAGE COUNT AND DELAY TIMES
FOR BCD-TO-BINARY CONVERSION

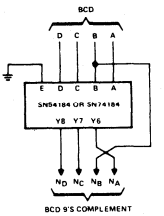
INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	56	80
3	6	140	200
4	11	196	280
5	19	280	400
6	28	364	520

SN54184 and SN74184 BCD-to-binary converters (continued)

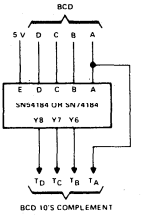
6-BIT CONVERTER



BCD 9'S COMPLEMENT CONVERTER



BCD 10'S COMPLEMENT CONVERTER



FUNCTION TABLE
BCD-TO-BINARY CONVERTER

BCD WORDS	INPUTS (See Note A)					OUTPUTS (See Note B)				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.

B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table (above, right) when the devices are connected as shown above the function table.

FUNCTION TABLE
BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

TABLE II

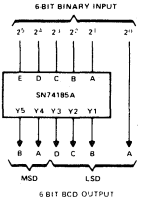
SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES

FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns)	
		TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER



FUNCTION TABLE

BINARY WORDS	INPUTS						OUTPUTS							
	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 · 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 · 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 · 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 · 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 · 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 · 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 · 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 · 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 · 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 · 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 · 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 · 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 · 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 · 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 · 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 · 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 · 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 · 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 · 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 · 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 · 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 · 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 · 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 · 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 · 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 · 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 · 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 · 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 · 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 · 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 · 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 · 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54184, SN54185A . . . . . −55°C to 125°C
SN74184, SN74185A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54184, SN54185A			SN74184, SN74185A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

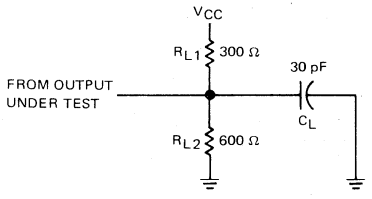
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 12 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all programmed outputs low				62	99	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable G	C_L = 15 pF,		19	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable G	R_{L1} = 400 Ω,		22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from binary select	R_{L2} = 600 Ω,		27	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from binary select	See Figure 1 and Note 2		23	40	ns

PARAMETER MEASUREMENT INFORMATION

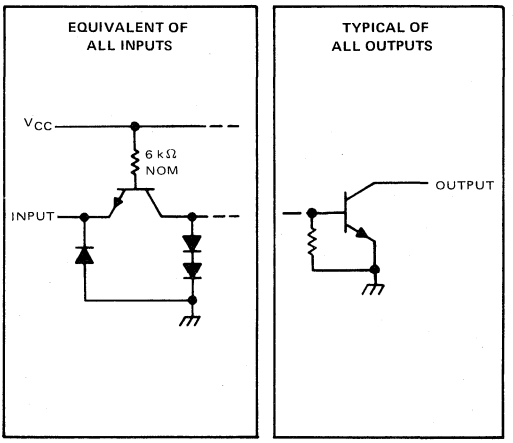


C_L includes probe and jig capacitance.

LOAD CIRCUIT
FIGURE 1

NOTE 2: Voltage waveforms are shown on page 148.

schematics of inputs and outputs



TYPICAL APPLICATION DATA
SN54184, SN74184

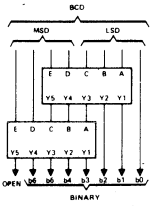


FIGURE 1–BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

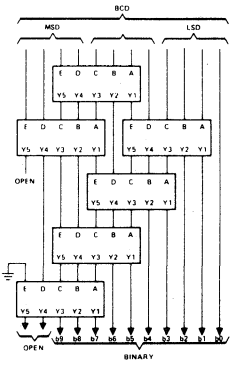


FIGURE 2–BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

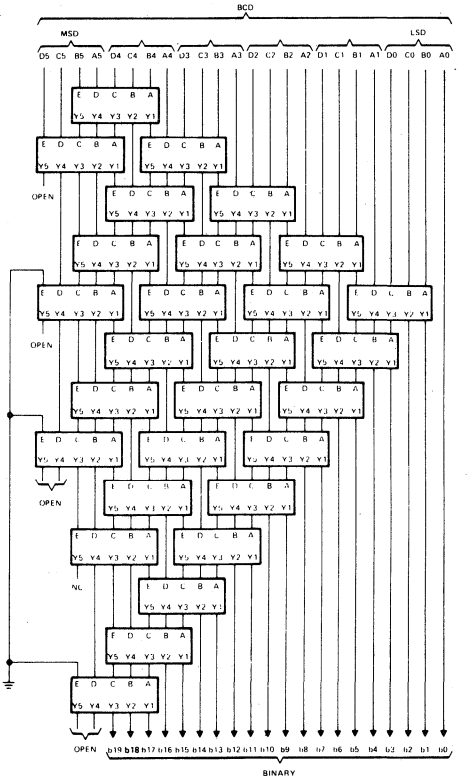


FIGURE 3–BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

MSD–most significant decade
LSD–least significant decade
Each rectangle represents an SN54184 or SN74184.

TYPICAL APPLICATION DATA
SN54185A, SN74185A

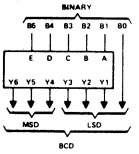


FIGURE 4–6-BIT BINARY-TO-BCD CONVERTER

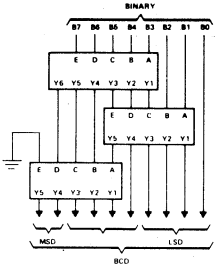


FIGURE 5–8-BIT BINARY-TO-BCD CONVERTER

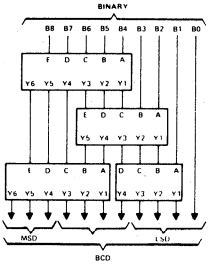


FIGURE 6–9-BIT BINARY-TO-BCD CONVERTER

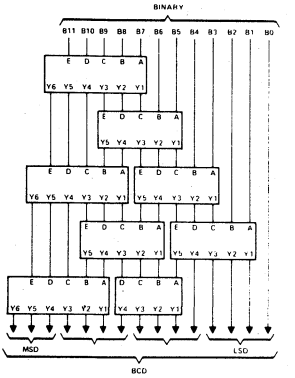


FIGURE 7–12-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

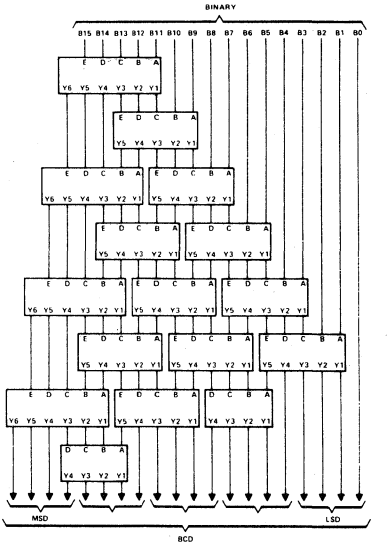


FIGURE 8–16-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

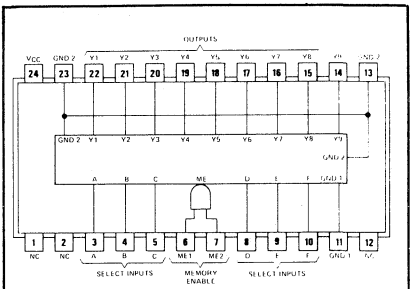
MSD—Most significant decade
LSD—Least significant decade
NOTES: A. Each rectangle represents an SN54185A or an SN74185A.
B. All unused E inputs are grounded.

TYPES SN54186, SN74186
512-BIT PROGRAMMABLE READ-ONLY MEMORIES

BULLETIN NO. DL-S 7211862, DECEMBER 1972

- Field-Programmable for Direct Implementation of Customized or Prototype Memories
- Ideal for Microprogramming, Reference Tables, and Code Converters
- Typical Access Time . . . 50 ns
- Typical Power Dissipation . . . 0.6 mW/Bit
- 64 Words of 8 Bits Each Available for Programming
- 65th Word and 9th Bit Used to Ensure Uniformity of Programming and to Test for Proper Function
- Open-Collector Outputs for Easy Word Expansion
- Fully Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see description
Y9 is used for testing purposes. The logic at Y9 is undefined.

NC—No internal connection

description

The SN54186 and SN74186 are field-programmable, 512-bit, read-only memories organized as 64 words of eight bits each. These monolithic transistor-transistor-logic memory arrays are addressed in conventional six-bit binary with full on-chip decoding. Taking either one or both of the memory-enable inputs low will inhibit the memory by causing all eight outputs to be high (off). Open-collector outputs permit easy word expansion to 3,712 words of n-bits with no additional output buffering.

The address of an eight-bit word is accomplished through the buffered binary select inputs in coincidence with high-logic-level voltages at both enable inputs. Where multiple '186 devices are used in memory system, the enable inputs allow easy decoding of additional address bits.

The circuit actually contains a ninth bit at each word location and a sixty-fifth word location which are programmed during testing to ensure capability of being programmed using the procedures specified on the following page.

Data can be electronically programmed as desired at any of the remaining 512 bit locations of the '186 in accordance with the programming procedure specified. When symbolized as SN54186 or SN74186, the unprogrammed memory will provide a low-level output from all 512 bit locations. The programming procedure open-circuits a fusible metal link which results in a high-level (off-state) output at the locations selected and programmed. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a high level. Outputs never having been altered may later be programmed to supply a high-level output. Operation of the memory within the absolute maximum ratings and the recommended operating conditions will not alter the memory content.

The open-collector outputs of these memories are capable of sinking 12 milliamperes of current and may be wire-AND connected to other memories to increase the number of words without additional output buffering. Table 1 shows typical load resistor values for fan-outs of one to seven Series 54/74 loads and indicates the maximum number of wire-AND connections and resultant word capacity limits.

TABLE 1
WORD CAPACITY vs TTL LOADS
(V_{CC} = 5 V)

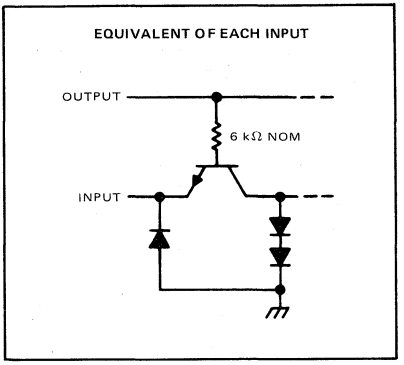
LOADS	MIN R_L (Ω)	MAX NO. WIRE-ANDS†	MAX NO. OF WORDS
1	442	58	3712
2	522	49	3136
3	639	39	2496
4	821	30	1920
5	1150	20	1280
6	1916	10	640
7	5750	2	128

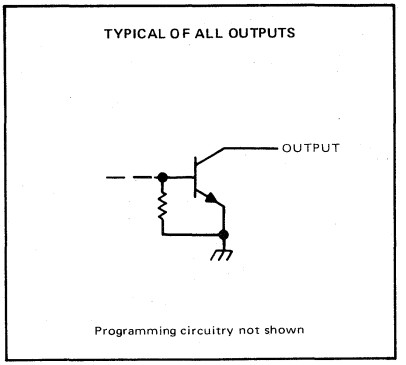
†Total number of '186 outputs connected to each common bus.

description (continued)

The SN54186 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74186 is characterized for operation from 0°C to 70°C.

schematics of input and outputs





step-by-step programming procedure

Programming the SN54186 or SN74186 is performed individually for each of the 512 bit locations and consists basically of applying a current pulse to each output terminal where a low logic level is to be changed to a high (off) level. The power supply and ground connections described below are designed to ensure that the alteration of the memory content occurs during the programming procedure only.

1. Connect the memory as shown in Figure 1. To address a particular word in the memory, set the input switches to the binary equivalent of that word where a low logic level (V_{IL}) is as specified under "recommended conditions for programming" and a high logic level (V_{IH}) is either an open circuit or connection to an open-collector TTL gate with no pull-up resistor.
2. Apply a current pulse as specified to the pin associated with the first bit to be changed from a low-level to a high-level output.
3. Repeat Step 2 for each high-level output desired in the word addressed (program only one bit at a time). Any bit that is to remain at a low level should have its respective output open-circuited during the entire programming cycle for the addressed word.
4. Set the next input address and repeat steps 2 and 3. This procedure is repeated for each input address for which a specific output word pattern is desired. Note that all addresses do not have to be programmed at the same time, nor do all output bits for a given address. A low logic level can always be changed to a high logic level simply by repeating Steps 1 and 2. Once programmed to provide a high logic level, the output cannot be changed to supply a low logic level.

recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltages (see Note 1)	V_{CC}	4.75	5	5.25	V
	GND 1	−5		−6†	
Input voltage (see Notes 2 and 3)	High level	Open circuit or equivalent			
	Low level	−5		−6†	V
Output voltage (see Note 4)				−7†	V
Output current		−110	−120	−130	mA
Duration of programming pulse (see Note 5)		700			ms
Case temperature (see Note 6)				75	°C

†Absolute maximum rating

NOTES: 1. Voltage values are with respect to the GND 2 terminals.
2. The high-level (off) output of a Series 54/74 open-collector gate with no pull-up resistor meets the requirements for a high-level input voltage.
3. The low-level input voltage must be within ±0.5 volts of the applied voltage at GND 1.
4. The output must be clamped to ensure that the output voltage will not be more negative than −7 V.
5. Programming is guaranteed if the pulse is applied to the output for 700 ms. Typically, programming occurs in less than 200 ms.
6. This refers to the temperature measured at the center of the bottom of the case.

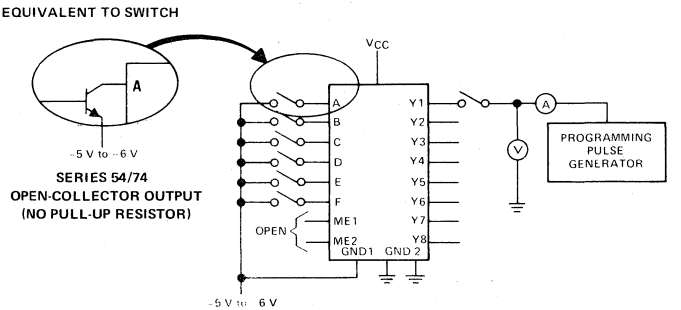


FIGURE 1–PROGRAMMING CONNECTIONS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 7) . . . . . 7 V
Input voltage (see Note 8) . . . . . 5.5 V
Operating free-air temperature range: SN54186 . . . . . −55°C to 125°C
SN74186 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 7. Voltage values are with respect to network ground terminals. Except during programming, GND 1 and both GND 2 terminals are all connected to system ground.
8. This rating applies at all times except during programming.

recommended operating conditions

	SN54186			SN74186			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			12	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			100	μA
			V_{OH} = 5.5 V			200	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 9.	Both ME at 0 V		47	95	mA
			Both ME at 4.5 V		80	120	
C_O	Off-state output capacitance	V_{CC} = 5 V, V_O = 2 V,	f = 1 MHz		5		pF

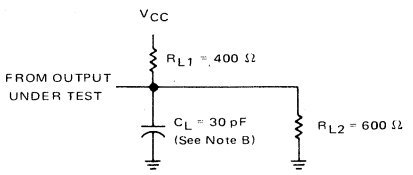
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 9: I_{CC} is measured with all outputs open and the select inputs at 4.5 V. Typical values are for 50% of the bits programmed.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

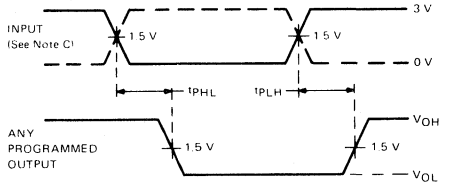
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF, R_{L1} = 400 Ω, R_{L2} = 600 Ω, See Figure 2	25	40	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable		25	55	75	
t_{PLH}	Propagation delay time, low-to-high-level output from select		25	55	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select		25	45	75	

3

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. The pulse generator is connected to the input under test. The other inputs, memory content permitting, are connected so that the input will switch the output under test.

FIGURE 2–PROPAGATION DELAY TIMES

SN54186, SN74186
FUNCTION TABLE/WORD-PATTERN WORKSHEET

WORD	INPUTS								OUTPUTS							
	BINARY SELECT						ENABLE		Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
	F	E	D	C	B	A	ME1	ME2								
ANY	X	X	X	X	X	X	X	L	H	H	H	H	H	H	H	H
ANY	X	X	X	X	X	X	L	X	H	H	H	H	H	H	H	H
0	L	L	L	L	L	L	H	H								
1	L	L	L	L	L	H	H	H								
2	L	L	L	L	H	L	H	H								
3	L	L	L	L	H	H	H	H								
4	L	L	L	H	L	L	H	H								
5	L	L	L	H	L	H	H	H								
6	L	L	L	H	H	L	H	H								
7	L	L	L	H	H	H	H	H								
8	L	L	H	L	L	L	H	H								
9	L	L	H	L	L	H	H	H								
10	L	L	H	L	H	L	H	H								
11	L	L	H	L	H	H	H	H								
12	L	L	H	H	L	L	H	H								
13	L	L	H	H	L	H	H	H								
14	L	L	H	H	H	L	H	H								
15	L	L	H	H	H	H	H	H								
16	L	H	L	L	L	L	H	H								
17	L	H	L	L	L	H	H	H								
18	L	H	L	L	H	L	H	H								
19	L	H	L	L	H	H	H	H								
20	L	H	L	H	L	L	H	H								
21	L	H	L	H	L	H	H	H								
22	L	H	L	H	H	L	H	H								
23	L	H	L	H	H	H	H	H								
24	L	H	H	L	L	L	H	H								
25	L	H	H	L	L	H	H	H								
26	L	H	H	L	H	L	H	H								
27	L	H	H	L	H	H	H	H								
28	L	H	H	H	L	L	H	H								
29	L	H	H	H	L	H	H	H								
30	L	H	H	H	H	L	H	H								
31	L	H	H	H	H	H	H	H								

—continued—

H = high-level input or high-voltage (off-level) output as defined by pull-up
L = low-level input or output voltage
X = irrelevant

SN54186, SN74186
FUNCTION TABLE/WORD-PATTERN WORKSHEET
(Continued)

32	H	L	L	L	L	L	H	H								
33	H	L	L	L	L	H	H	H								
34	H	L	L	L	H	L	H	H								
35	H	L	L	L	H	H	H	H								
36	H	L	L	H	L	L	H	H								
37	H	L	L	H	L	H	H	H								
38	H	L	L	H	H	L	H	H								
39	H	L	L	H	H	H	H	H								
40	H	L	H	L	L	L	H	H								
41	H	L	H	L	L	H	H	H								
42	H	L	H	L	H	L	H	H								
43	H	L	H	L	H	H	H	H								
44	H	L	H	H	L	L	H	H								
45	H	L	H	H	L	H	H	H								
46	H	L	H	H	H	L	H	H								
47	H	L	H	H	H	H	H	H								
48	H	H	L	L	L	L	H	H								
49	H	H	L	L	L	H	H	H								
50	H	H	L	L	H	L	H	H								
51	H	H	L	L	H	H	H	H								
52	H	H	L	H	L	L	H	H								
53	H	H	L	H	L	H	H	H								
54	H	H	L	H	H	L	H	H								
55	H	H	L	H	H	H	H	H								
56	H	H	H	L	L	L	H	H								
57	H	H	H	L	L	H	H	H								
58	H	H	H	L	H	L	H	H								
59	H	H	H	L	H	H	H	H								
60	H	H	H	H	L	L	H	H								
61	H	H	H	H	L	H	H	H								
62	H	H	H	H	H	L	H	H								
63	H	H	H	H	H	H	H	H								

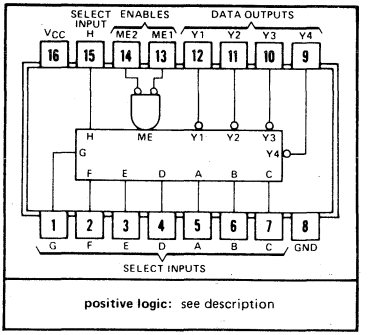
H = high-level input or high-voltage (off-level) output as defined by pull-up
L = low-level input or output voltage
X = irrelevant

TYPES SN54187, SN74187
1024-BIT READ-ONLY MEMORIES

BULLETIN NO. DL-S 7211397, FEBRUARY 1971—REVISED DECEMBER 1972

- Typical Access Time . . . 40 ns
- Typical Power Dissipation . . . 0.46 mW/Bit
- Organized as 256 Words by 4 Bits
- Ideal for Microprogramming, Reference Tables, and Code Converters
- Easily Expandable
- Fully Decoded, Buffered Inputs
- Diode-Clamped Inputs
- Full Fan-Out, Open-Collector Outputs
- Fully Compatible with Most TTL and DTL Circuits

SN54187 . . . J OR W PACKAGE
SN74187 . . . J, N, OR W PACKAGE
(TOP VIEW)



positive logic: see description

description

The SN54187 and SN74187 circuits are custom-programmed, 1024-bit, read-only memories organized as 256 words of four bits each. These monolithic, high-speed transistor-transistor logic (TTL) memory arrays are addressed in straight eight-bit binary with full on-chip decoding. Two overriding memory-enable inputs are provided which, when either one or both are taken high, will inhibit the function causing all four outputs to remain high (off). Data, as specified by the customer, are permanently programmed into the monolithic structure for the 1024 bit locations. This organization is expandable to 41,472 words of n-bits with no additional output buffering.

The address of a four-bit word is accomplished through the buffered binary select inputs in coincidence with low-level voltages at both enable inputs. The most significant binary select inputs, D through H, are decoded internally in the X plane to select one-of-32 lines, and the least significant bits, A, B, and C, are internally decoded in the Y plane to accomplish one-of-eight decoding to drive the four output buffers. Where multiple SN54187 or SN74187 devices are used in a memory system, the enable input allows easy decoding of additional address bits.

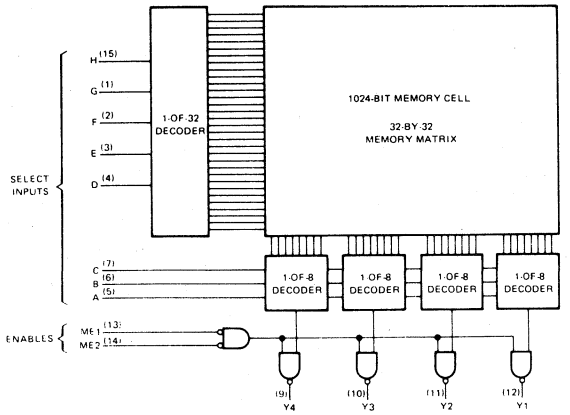
Data are programmed into the memory cell at the emitters of 1024 transistors. The memory cell consists of a 32-by-32 matrix of transistors. In the X plane each of the 32 address decoding gate outputs supply common base drive to 32 transistors. In the Y plane the 32 transistors are arranged into four groups of eight. This permits each of the bit lines to be terminated in four one-of-eight decoders which achieves the four-bit word length.

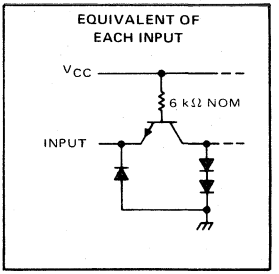
The open-collector outputs are capable of sinking 16 milliamperes of current and may be wire-AND connected to increase the number of words available. An external pull-up resistor is recommended for definition of the high (off) level output voltage.

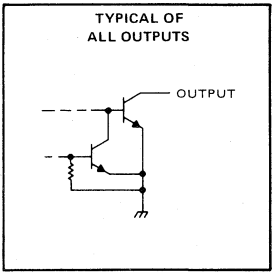
The customer can specify the output logic level desired at each of the 1024 bit locations by completing the supplementary ordering data and a set of data cards punched in accordance with the data format shown under ordering instructions. Upon receipt of the order, Texas Instruments will assign a special device number to the device programmed according to the customer's order. The completed device will be marked with the TI special device number (not SN54187 or SN74187). It is important that the customer specify not only the output levels desired at all 1024 bit locations, but also the other information requested.

Access propagation delay time is typically 40 nanoseconds and power dissipation is typically 0.46 milliwatt per bit. The SN54187 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74187 is characterized for operation from 0°C to 70°C.

functional block diagram and schematics of inputs and outputs







word selection

Word selection is accomplished in a conventional 8-bit positive-logic binary code with the A select input being the least-significant bit progressing alphabetically through the select inputs to H which is the most-significant bit.

WORD-SELECT TABLE

WORD	INPUTS							
	H	G	F	E	D	C	B	A
0	L	L	L	L	L	L	L	L
1	L	L	L	L	L	L	L	H
2	L	L	L	L	L	L	H	L
3	L	L	L	L	L	L	H	H
4	L	L	L	L	L	H	L	L
5	L	L	L	L	L	H	L	H
6	L	L	L	L	L	H	H	L
7	L	L	L	L	L	H	H	H
8	L	L	L	L	H	L	L	L
	Words 9 thru 250 omitted							
251	H	H	H	H	H	L	H	H
252	H	H	H	H	H	H	L	L
253	H	H	H	H	H	H	L	H
254	H	H	H	H	H	H	H	L
255	H	H	H	H	H	H	H	H

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54187 (see Note 2) . . . . . −55°C to 125°C
SN74187 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

	SN54187			SN74187			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A (see Note 2)	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, V_{OH} = 5.5 V			40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 3		92	130	mA
C_o	Off-state output capacitance	V_{CC} = 5 V, f = 1 MHz	V_O = 5 V,		6.5		pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF to GND, R_{L1} = 300 Ω to V_{CC}, R_{L2} = 600 Ω to GND, See Note 4		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from select			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from select			40	60	

NOTES: 1. Voltage values are with respect to network ground terminal.
2. An SN54187 in the W package operating at free-air temperatures above 111°C requires a heat sink that provides a thermal resistance from case-to-free-air, $R_{\theta CA}$, of not more than 46°C/W.
3. With outputs open and both ME inputs grounded, I_{CC} is measured first by selecting a word which contains the maximum number of programmed high-level outputs, then by selecting a word which contains the maximum number of programmed low-level outputs.
4. Load circuit is as described above; voltage waveforms are shown on page 148.

ORDERING INSTRUCTIONS

Programming instructions for the SN54187 or SN74187 are solicited in the form of a sequenced deck of 32 standard 80-column data cards providing the information requested under "data card format," accompanied by a properly sequenced listing of these cards, and the supplementary ordering data. Upon receipt of these items, a computer run will be made from the deck of cards which will produce a complete function table of the requested part. This function table, showing output conditions for each of the 256 words, will be forwarded to the purchaser as verification of the input data as interpreted by the computer-automated design (CAD) program. This single run also generates mask and test program data; therefore, verification of the function table should be completed promptly.

Each card in the data deck prepared by the purchaser identifies the eight words specified and describes the levels at the four outputs for each of the eight words. All addresses must have all outputs defined and columns designated as "blank" must not be punched. Cards should be punched according to the data card format shown.

SUPPLEMENTARY ORDERING DATA

Submit the following information with the data cards:

a) Customer's name and address
b) Customer's purchase order number
c) Customer's drawing number.

The following information will be furnished to the customer by Texas Instruments:

a) TI part number
b) TI sales order number
c) Date received.

DATA CARD FORMAT

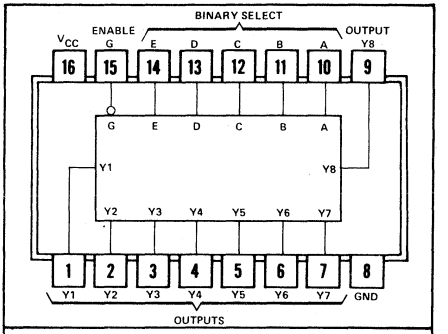
Column	
1- 3	Punch a right-justified integer representing the binary input address (000-248) for the first set of outputs described on the card.
4	Punch a "–" (Minus sign)
5- 7	Punch a right-justified integer representing the binary input address (007-255) for the last set of outputs described on the card.
8- 9	Blank
10-13	Punch "H", "L", or "X" for bits four, three, two, and one (outputs Y4, Y3, Y2, and Y1 in that order) for the first set of outputs specified on the card. H = high-voltage-level output, L = low-voltage-level output, X = output level irrelevant.
14	Blank
15-18	Punch "H", "L", or "X" for the second set of outputs.
19	Blank
20-23	Punch "H", "L", or "X" for the third set of outputs.
24	Blank
25-28	Punch "H" "L", or "X" for the fourth set of outputs.
29	Blank
30-33	Punch "H", "L", or "X" for the fifth set of outputs.
34	Blank
35-38	Punch "H", "L", or "X" for the sixth set of outputs.
39	Blank
40-43	Punch "H", "L", or "X" for the seventh set of outputs.
44	Blank
45-48	Punch "H", "L", or "X" for the eighth set of outputs.
49	Blank
50-51	Punch a right-justified integer representing the current calendar day of the month.
52	Blank
53-55	Punch an alphabetic abbreviation representing the current month.
56	Blank
57-58	Punch the last two digits of the current year.
59	Blank
60-61	Punch "SN"
62-66	Punch a left-justified integer representing the Texas Instruments part number. This is supplied by the factory through a TI sales representative.
67-68	Blank
69-80	Preferably these columns should be punched to reflect the customer's part or specification-control number. This information is not essential.

TYPE SN74188A
256-BIT PROGRAMMABLE READ-ONLY MEMORY

BULLETIN NO. DL-S 7211873, DECEMBER 1972

- Field Programmable for Custom or Prototype Memories
- Mask-Programmable SN7488A is a Direct Replacement for the SN74188A
- Typical Access Time . . . 30 ns
- Organized as 32 Words of 8 Bits Each
- Ideal for Microprogramming and Code Converters
- Open-Collector Outputs are Easily Expanded
- Fully-Decoded Buffered Inputs
- Fully Compatible with Most TTL and DTL Circuits

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: see description

description

The SN74188A is a field-programmable, 256-bit, read-only memory organized as 32 words of eight bits each. This monolithic, high-speed, transistor-transistor-logic (TTL) memory array is addressed in five-bit binary with full on-chip decoding. An overriding memory-enable input is provided which, when taken high, will inhibit the function causing all eight outputs to remain high. The organization is expandable to 1,856 words of n-bits with no additional output buffering.

The address of an eight-bit word is accomplished through the buffered binary select inputs in coincidence with a low logic level at the enable input. Where multiple SN74188A devices are used in a memory system, the enable input allows easy decoding of additional address bits.

Data can be electronically programmed, as desired, at any of the 256 bit locations of the SN74188A in accordance with the programming procedure specified. Prior to programming, the memory contains a low-logic-level output condition at all 256 bit locations. The programming procedure open-circuits metal links which results in a high-logic-level output at selected locations. The procedure is irreversible and, once altered, the output for that bit is permanently programmed to provide a high logic level. Outputs never having been altered may later be programmed to supply a high-level output. Operation of the unit within the recommended operating conditions will not alter the memory content.

The open-collector outputs are capable of sinking 12 milliamperes of current and may be wire-AND-connected to other memories to increase the number of words without additional output buffering. External pull-up resistors should be used to improve noise margin and dynamic response. The best low-to-high propagation delay time is achieved when using minimum R_L (see Table I).

The mask-programmable SN7488A can be used to replace the SN74188A as they are functionally and mechanically identical. Likewise, most applications currently using the SN7488A can utilize the SN74188A as a direct replacement where field programming is desired.

TABLE 1
WORD CAPACITY vs TTL LOADS
(V_{CC} = 5 V, T_A = 0°C to 70°C)

LOADS	MIN R_L (Ω)	MAX NO. WIRE-ANDS†	MAX NO. OF WORDS
1	442	58	1856
2	522	49	1568
3	639	39	1248
4	821	30	960
5	1150	20	640
6	1916	10	320
7	5750	2	64

† Total number of SN74188A outputs connected to each common bus.

TENTATIVE DATA SHEET

step-by-step programming procedure

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed with specified input voltage levels.
2. Disable the outputs by applying a high-logic-level voltage to the enable input.
3. Only one bit location is programmed at a time. Open-circuit all outputs except the one to be programmed as a high logic level. Apply −0.7 V to the output to be programmed.
4. Apply the program pulse (V_{CC} = 10 V) and after the 10-volt level is achieved, enable the outputs (enable low). The 10-volt level and the enabling of the outputs should occur within the first 10 milliseconds of the program pulse. Disable the outputs (enable high) prior to removing the program pulse. (See Figure 1). The power supply must be capable of supplying 100 milliamperes at 10 volts.
5. Repeat steps 2 through 4 for each output of this address to be programmed as a high level.
6. Address next location and repeat steps 2 through 5.

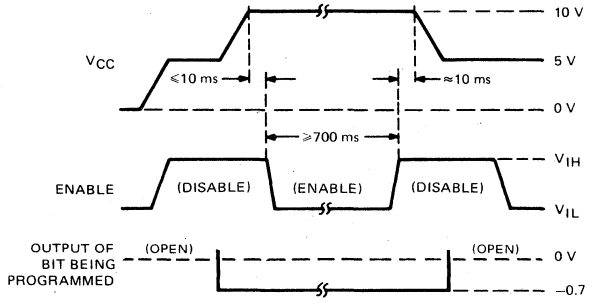
recommended conditions for programming

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 1)	Steady state	0	5	5.5	V
	Program pulse	9	10	11†	
Input voltage	Low level			0.5	V
	High level	2.4		5	
Output conditions for programming	To a low logic level	Open circuit			V
	To a high logic level	−0.6		−0.8	
Duration of programming pulse (see Note 2)		700			ms
Case temperature (see Note 3)				75	°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. Programming is guaranteed if the pulse is applied for 700 ms. Typically, programming occurs in less than 200 ms.
3. This refers to the temperature measured at the center of the bottom of the case.

†Absolute maximum rating.

programming pulses

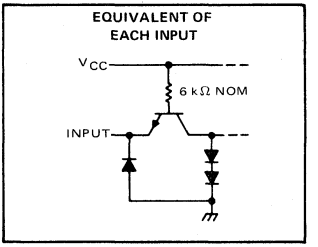


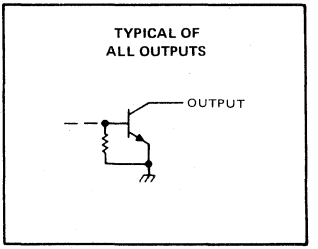
VOLTAGE WAVEFORMS

Location to be programmed must be addressed prior to enabling. Repeat pulses for each output at this address which is to be programmed to a high logic level.

FIGURE 1

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Notes 1 and 4) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.
4. This rating applies at all times except during programming.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5	V
Low-level output current, I_{OL}			12	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.45	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX	See Note 5		50	80	mA
I_{CCL}	Supply current, all outputs low	V_{CC} = MAX	See Note 6		82	110	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 5. I_{CCH} is measured with all inputs at 4.5 V, all outputs open.
6. I_{CCL} is measured with enable input grounded, all other inputs at 4.5 V, and all outputs open. The typical value shown is for the worst-case condition of all eight outputs low at one time. This condition may not be possible after the device has been programmed.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any	C_L = 30 pF to GND, R_{L1} = 400 Ω to V_{CC}, R_{L2} = 600 Ω to GND, See Note 7		23	50	ns
t_{PHL}					34	50	
t_{PLH}	Select	Any			28	50	ns
t_{PHL}					31	50	

§t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

NOTE 7: Load circuit is as described above; waveforms are shown on page 148.

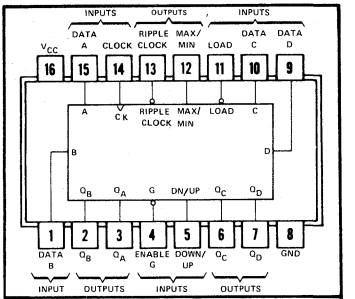
TYPES SN54190, SN54191, SN54LS190, SN54LS191, SN74190, SN74191, SN74LS190, SN74LS191
SYNCHRONOUS UP/DOWN COUNTERS WITH DOWN/UP MODE CONTROL

BULLETIN NO. DL-S 7211865, DECEMBER 1972

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications

TYPE	AVERAGE PROPAGATION DELAY	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'190, '191	20 ns	25 MHz	325 mW
'LS190, 'LS191	20 ns	25 MHz	90 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

description

The '190, 'LS190, '191, and 'LS191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The '191 and 'LS191 are 4-bit binary counters and the '190 and 'LS190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

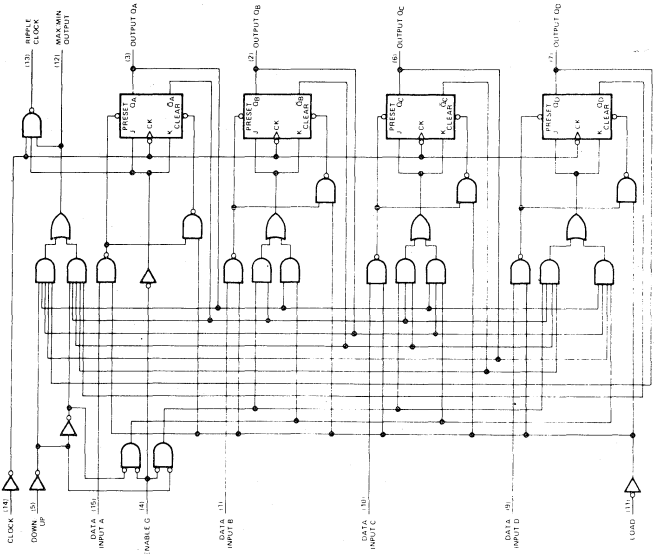
The clock, down/up, and load inputs are buffered to lower the drive requirement which significantly reduces the number of clock drivers, etc., required for long parallel words.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

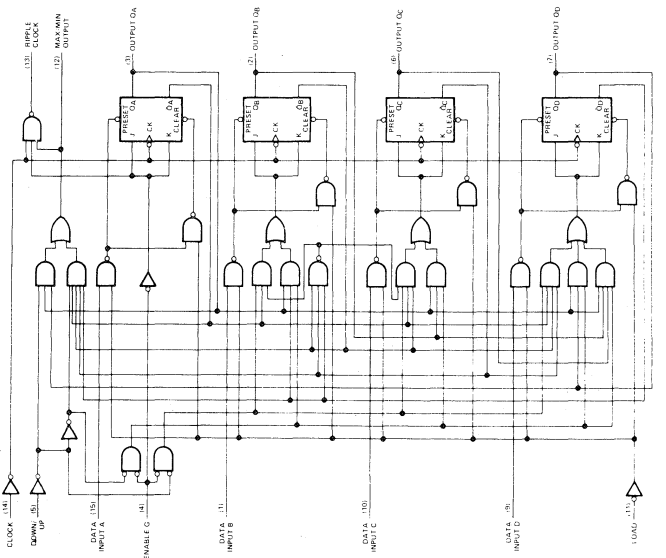
Series 54' and 54LS' are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74' and 74LS' are characterized for operation from 0°C to 70°C.

functional block diagrams

'191, 'LS191 BINARY COUNTERS



'190, 'LS190 DECADE COUNTERS

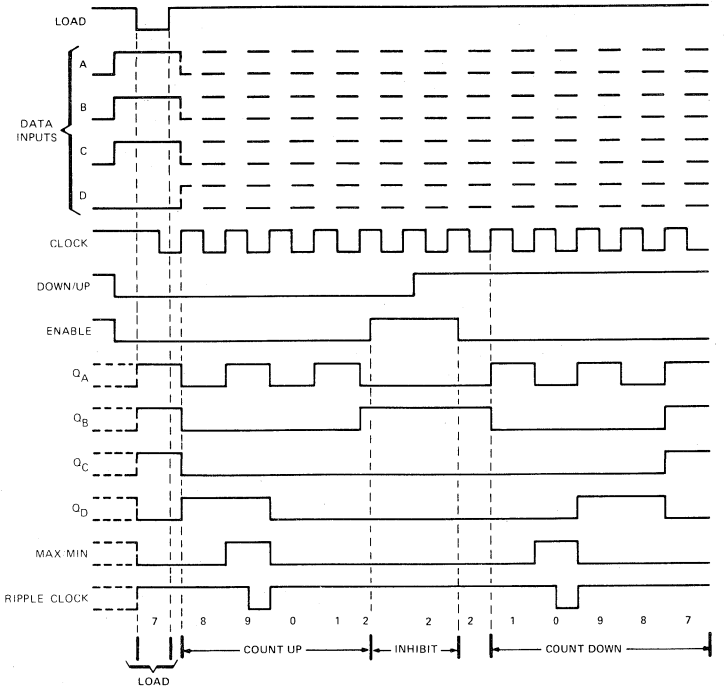


. . . Dynamic input activated by a transition from a high level to a low level.

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.

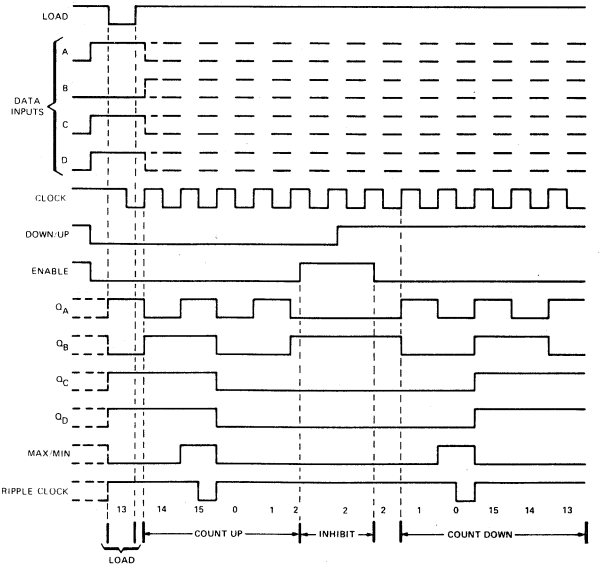


'191, 'LS191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage: SN54', SN74' Circuits . . . . . 5.5 V
SN54LS', SN74LS' Circuits . . . . . 7 V
Operating free-air temperature range: SN54', SN54LS' Circuits . . . . . −55°C to 125°C
SN74', SN74LS' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54190, SN54191			SN74190, SN74191			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Input clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	V_{CC} = MIN	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MIN			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	High-level input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current at any input except enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IH}	High-level input current at enable input				120			120	μA
I_{IL}	Low-level input current at any input except enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{IL}	Low-level input current at enable input				−4.8			−4.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	99		65	105	mA

† For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'190, '191			UNIT
				MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	

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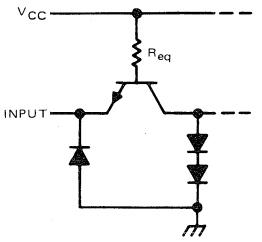
¶ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

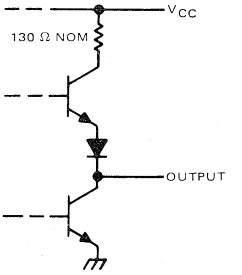
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Enable input: R_{eq} = 1.3 kΩ NOM
All other inputs: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



recommended operating conditions

	SN54LS190, SN54LS191			SN74LS190, SN74LS191			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Input clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$	25			25			ns
Width of load input pulse, $t_{w(load)}$	35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS190, SN54LS191			SN74LS190, SN74LS191			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
				I_{OL} = 8 mA					0.35	0.5	
I_I	High-level input current at maximum input voltage	Enable	V_{CC} = MAX, V_I = 5.5 V				0.3			0.3	mA
		Others					0.1			0.1	
I_{IH}	High-level input current	Enable	V_{CC} = MAX, V_I = 2.7 V				60			60	μA
		Others					20			20	
I_{IL}	Low-level input current	Enable	V_{CC} = MAX, V_I = 0.4 V				−1.08			−1.08	mA
		Others					−0.4			−0.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2			18	32		18	32	mA

†For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

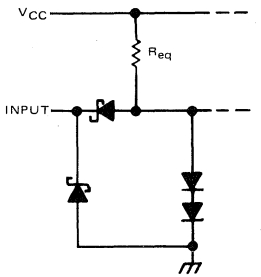
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS190, 'LS191 MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	

¶ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

3

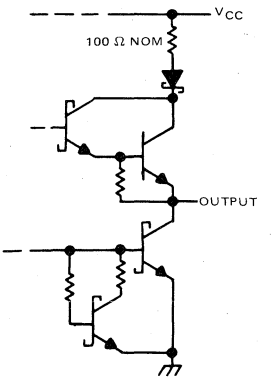
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Enable input: R_{eq} = 8.33 kΩ NOM
Load input: R_{eq} = 25 kΩ NOM
All other inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF ALL OUTPUTS



TENTATIVE DATA
This page provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

PARAMETER MEASUREMENT INFORMATION

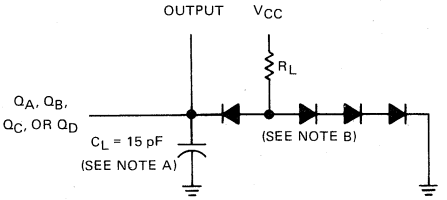


FIGURE 1–LOAD CIRCUIT
FOR SWITCHING TIME MEASUREMENT

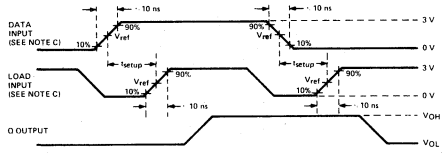
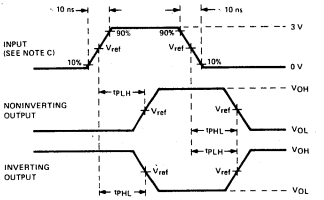


FIGURE 2–DATA SETUP TIME VOLTAGE WAVEFORMS



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

FIGURE 3–GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

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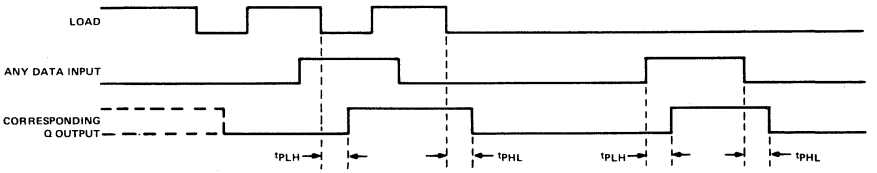
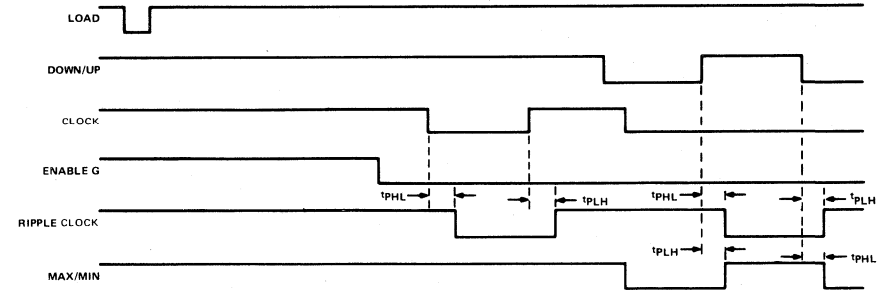
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, duty cycle ≤ 50%, PRR ≤ 1 MHz.
D. V_{ref} = 1.5 V for '190 and '191; 1.3 V for 'LS190 and 'LS191.



NOTE E: Conditions on other inputs are irrelevant.

FIGURE 4–LOAD TO OUTPUT AND DATA TO OUTPUT

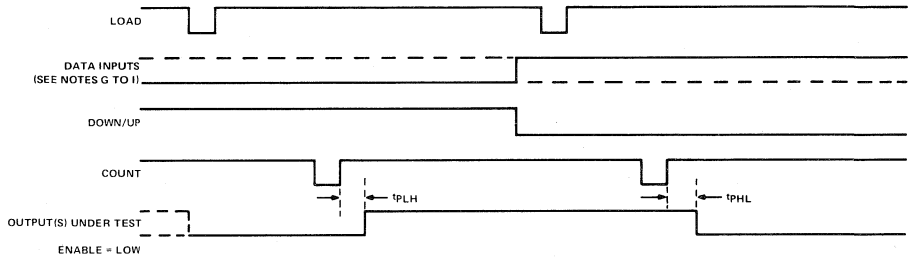


NOTE F: All data inputs are low.

FIGURE 5–ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

PARAMETER MEASUREMENT INFORMATION

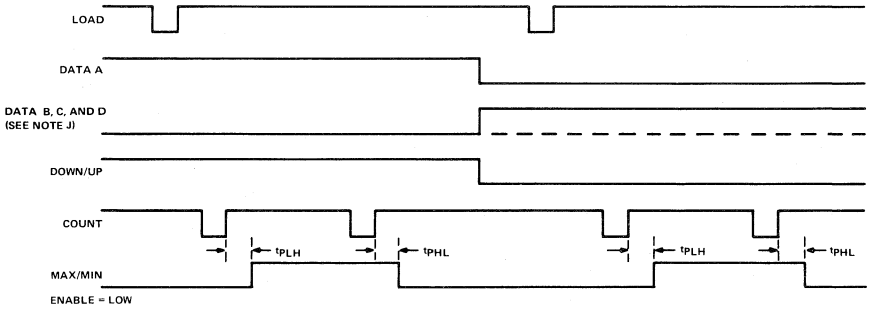
switching characteristics (continued)



NOTES: G. to test Q_A, Q_B, and Q_C outputs of '190 and 'LS190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
H. To test Q_D output of '190 and 'LS190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
I. To test Q_A, Q_B, Q_C, and Q_D outputs of '191 and 'LS191: All four data inputs are shown by the solid line.

3

FIGURE 6–CLOCK TO OUTPUT



NOTE J: Data inputs B and C are shown by the dashed line for the '190 and 'LS190 and the solid line for the '191 and 'LS191: Data input D is shown by the solid line for both devices.

FIGURE 7–CLOCK TO MAX/MIN

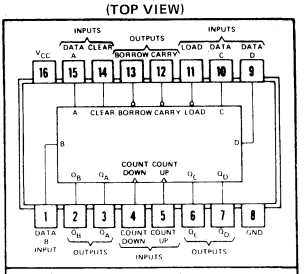
TYPES SN54192, SN54193, SN54L192, SN54L193, SN54LS192, SN54LS193 SN74192, SN74193, SN74L192, SN74L193, SN74LS192, SN74LS193 SYNCHRONOUS 4-BIT UP/DOWN COUNTERS (DUAL CLOCK WITH CLEAR)

BULLETIN NO. DL-S 7211828, DECEMBER 1972

- Cascading Circuitry Provided Internally
- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input

TYPES	TYPICAL MAXIMUM COUNT FREQUENCY	TYPICAL POWER DISSIPATION
'192, '193	32 MHz	325 mW
'L192, 'L193	7 MHz	43 mW
'LS192, 'LS193	32 MHz	85 mW

'192, '193 . . . J, N, OR W PACKAGE
'L192, 'L193 . . . J OR N PACKAGE
'LS192, 'LS193 . . . J, N, OR W PACKAGE
(TOP VIEW)



logic: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The '192, 'L192, and 'LS192 circuits are BCD counters and the '193, 'L193 and 'LS193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count inputs is pulsed while the other count input is high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements. This reduces the number of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

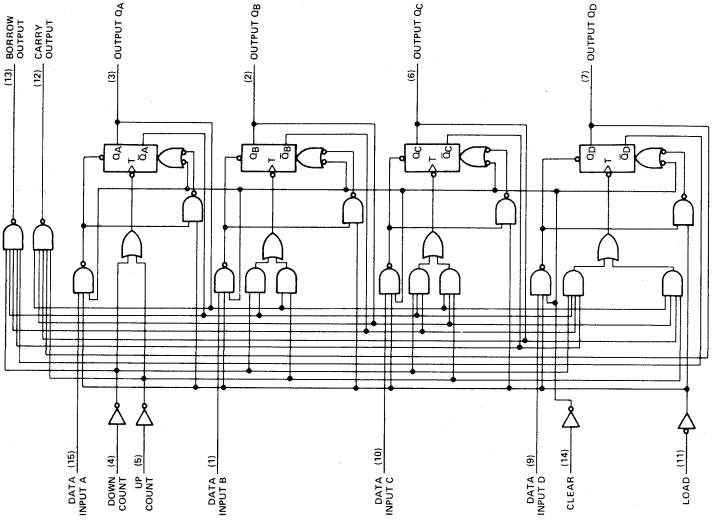
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54L'	SN54LS'	SN74'	SN74L'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	8	7	7	8	7	V
Input voltage	5.5	5.5	7	5.5	5.5	7	V
Operating free-air temperature range	−55 to 125			0 to 70			°C
Storage temperature range	−65 to 150			−65 to 150			°C

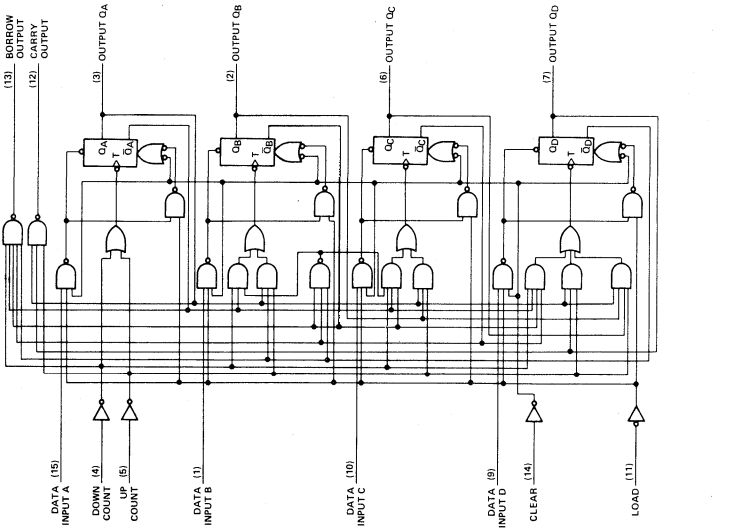
NOTE 1: Voltage values are with respect to network ground terminal.

functional block diagrams

'193, 'L193, 'LS193



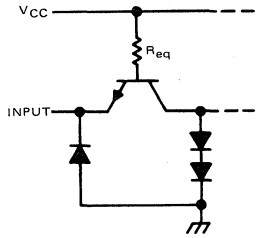
'192, 'L192, 'LS192



— Dynamic input activated by a transition from a high level to a low level.

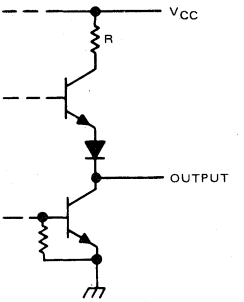
schematics of inputs and outputs

EQUIVALENT OF INPUTS
OF '192, '193, 'L192, 'L193



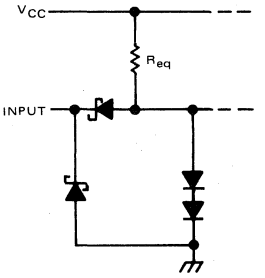
'192, '193: R_{eq} = 4 kΩ NOM
'L192, 'L193: R_{eq} = 40 kΩ NOM

TYPICAL OF OUTPUTS
OF '192, '193, 'L192, 'L193



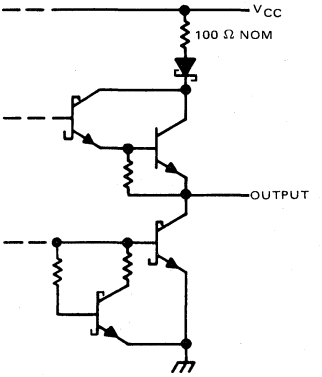
'192, '193: R = 130 Ω NOM
'L192, 'L193: R = 500 Ω NOM

EQUIVALENT OF INPUTS
OF 'LS192, 'LS193



Enable input: R_{eq} = 8.33 kΩ NOM
All other inputs: R_{eq} = 17 kΩ NOM

TYPICAL OF OUTPUTS
OF 'LS192, 'LS193

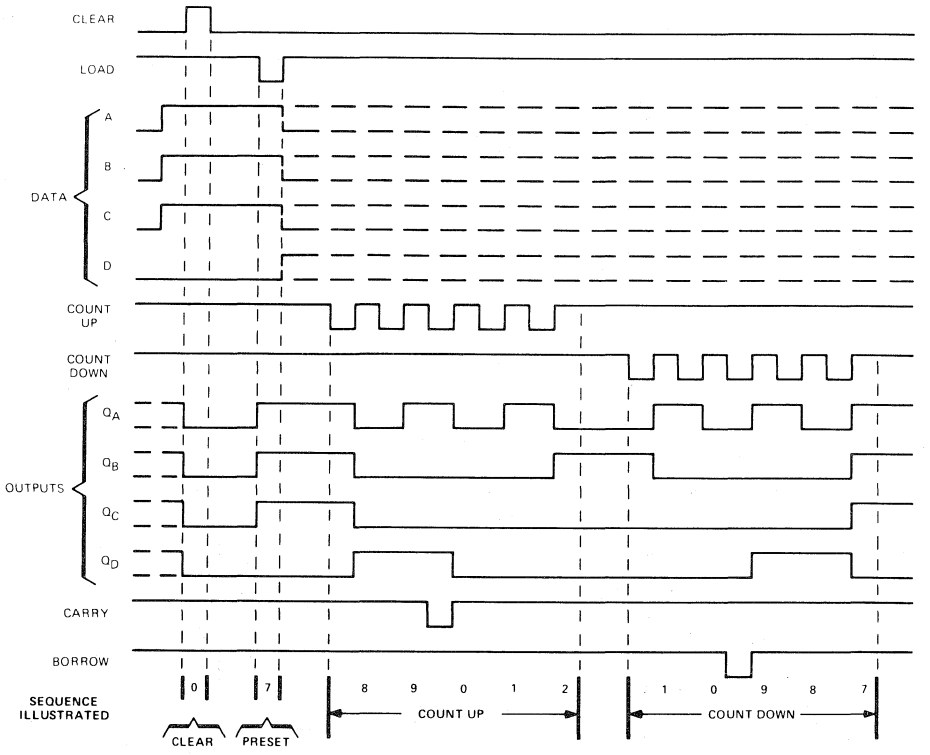


'192,'L192, 'LS192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.



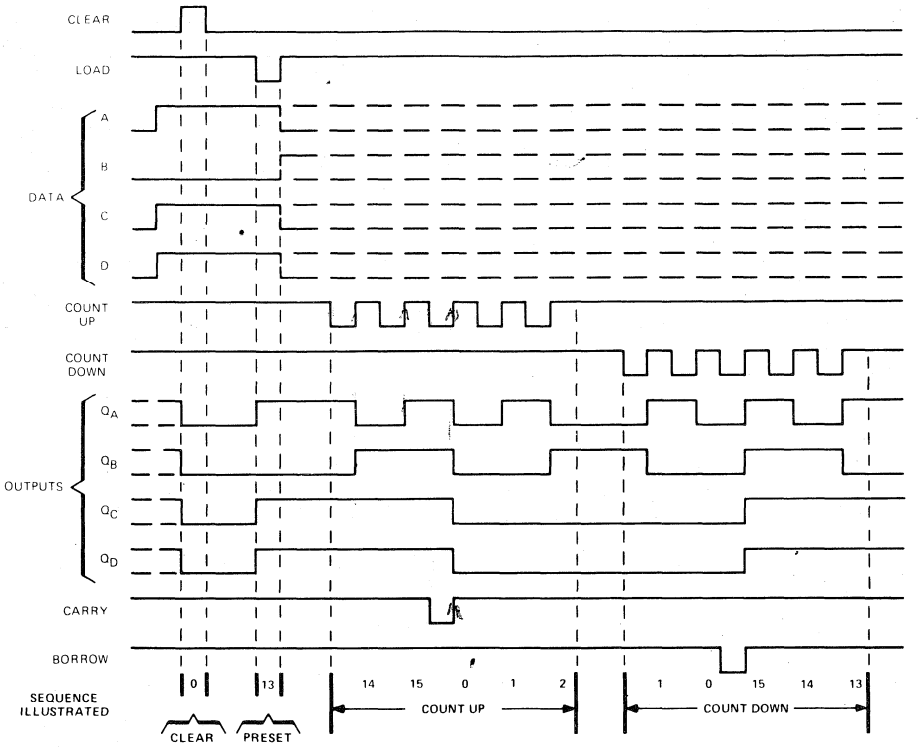
NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

'193, 'L193, 'LS193 BINARY COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditions

	SN54192 SN54193			SN74192 SN74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54192 SN54193			SN74192 SN74193			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	89		65	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figures 1 and 2	25	32		MHz
t_{PLH}	Count-up	Carry			17	26	ns
t_{PHL}					16	24	
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}					16	24	
t_{PLH}	Either Count	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	Load	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	Clear	Q			22	35	ns

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

recommended operating conditions

	SN54L192 SN54L193			SN74L192 SN74L193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Count frequency, f_{count}	0		3	0		3	MHz
Width of any input pulse, t_w	200			200			ns
Data setup time, t_{setup} (see Figure 1)	100			100			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature range, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L192 SN54L193			SN74L192 SN74L193			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.7 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		8.5	15		8.5	15	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 50 pF, R_L = 4 kΩ, See Figures 1 and 2	3	7		MHz
t_{PLH}	Count-up	Carry			65	130	ns
t_{PHL}					65	130	
t_{PLH}	Count-down	Borrow			65	130	ns
t_{PHL}					65	130	
t_{PLH}	Either Count	Q			104	200	ns
t_{PHL}					135	240	
t_{PLH}	Load	Q			130	240	ns
t_{PHL}					105	200	
t_{PHL}	Clear	Q			110	200	ns

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

recommended operating conditions

	SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Data hold time, t_{hold}	0			0			ns
Operating free-air temperature range, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS192 SN54LS193			SN74LS192 SN74LS193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			17	31		17	31	mA

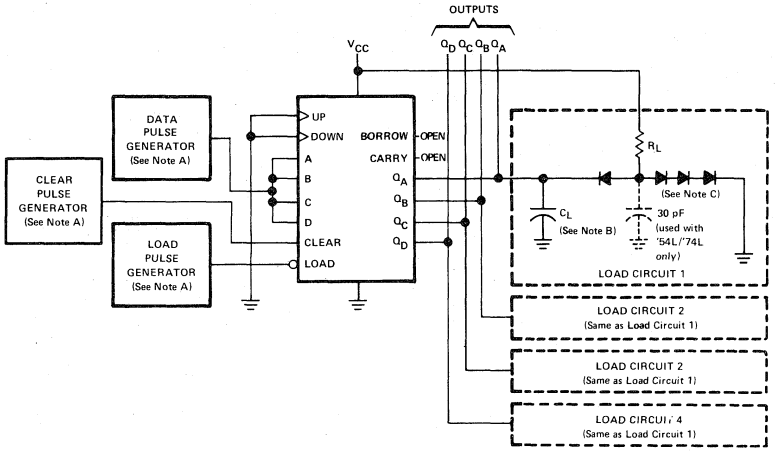
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all outputs open, clear and load inputs grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

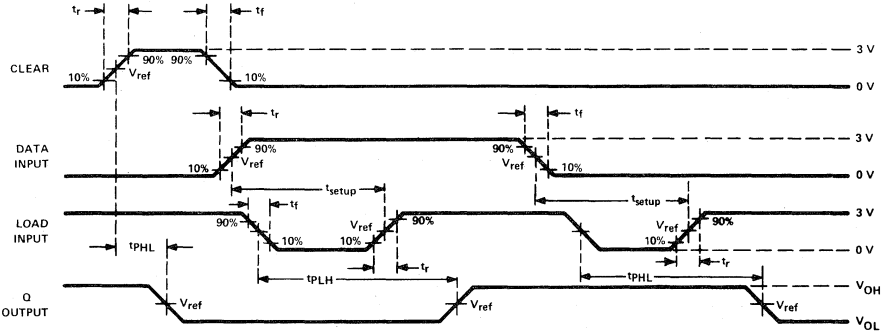
PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ, See Figures 1 and 2	25	32		MHz
t_{PLH}	Count-up	Carry			17	26	ns
t_{PHL}					16	24	
t_{PLH}	Count-down	Borrow			16	24	ns
t_{PHL}					16	24	
t_{PLH}	Either Count	Q			25	38	ns
t_{PHL}					31	47	
t_{PLH}	Load	Q			27	40	ns
t_{PHL}					29	40	
t_{PHL}	Clear	Q			22	35	ns

¶f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

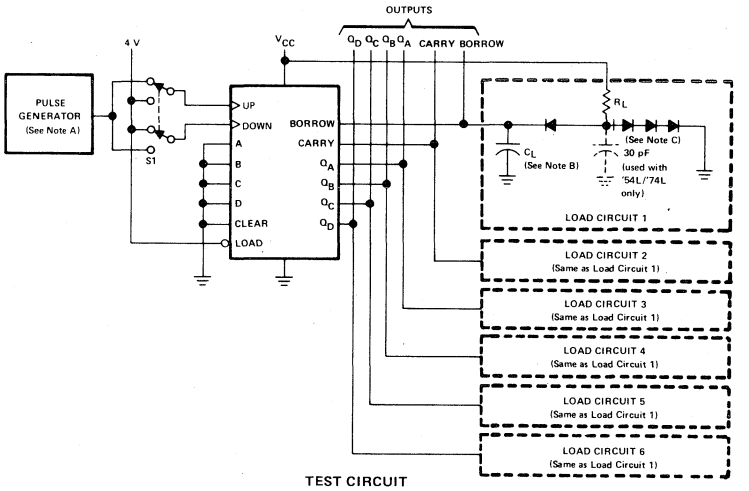


VOLTAGE WAVEFORMS

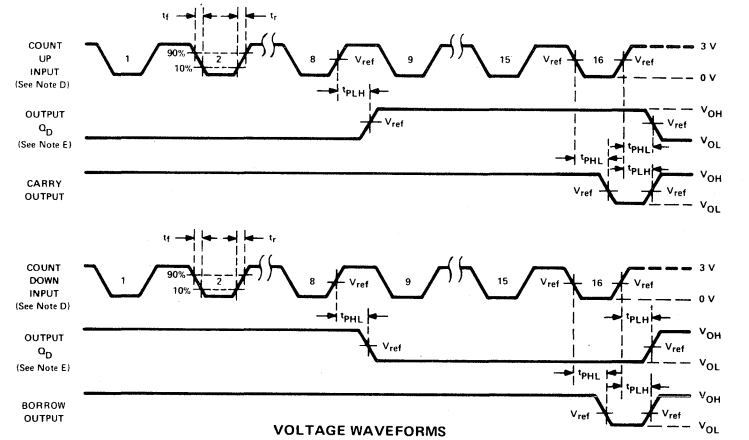
NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$ and for the data pulse generator PRR $\leqslant$ 500 kHz, duty cycle = 50%; for the load pulse generator PRR is two times data PRR, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 for '192, '193, 'LS192, and 'LS193; 1N916 for 'L192 and 'L193.
D. t_r and $t_f \leqslant 7$ ns for '192, '193, 'LS192, and 'LS193; $\leqslant 25$ ns for 'L192 and 'L193.
E. V_{ref} is 1.5 volts for '192, '193, 'LS192, and 'LS193; 1.3 volts for 'L192 and 'L193.

FIGURE 1–CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. Diodes are 1N3064 for '192, '193, 'LS192, and 'LS193; 1N916 for 'L192 and 'L193.
D. Count-up and count-down pulse shown are for the '193, 'L193, and 'LS193 binary counters. Count cycle for '192, 'L192, and 'LS192 decade counters is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.
F. t_r and $t_f \leq 7$ ns for '192, '193, 'LS192, and 'LS193; ≤ 25 ns for 'L192 and 'L193.
G. V_{ref} is 1.5 volts for '192, '193, 'LS192, and 'LS193; 1.3 volts for 'L192 and 'L193.

FIGURE 2—PROPAGATION DELAY TIMES

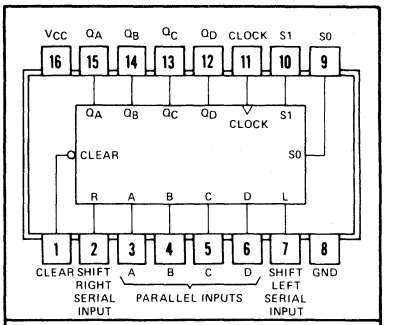
TYPES SN54194, SN54LS194, SN54S194, SN74194, SN74LS194, SN74S194
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

BULLETIN NO. DL-S 7211866, DECEMBER 1972

- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Right Shift
  - Left Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'194	36 MHz	195 mW
'LS194	28 MHz	60 mW
'S194	105 MHz	425 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_D)
Shift Left (In the direction Q_D toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

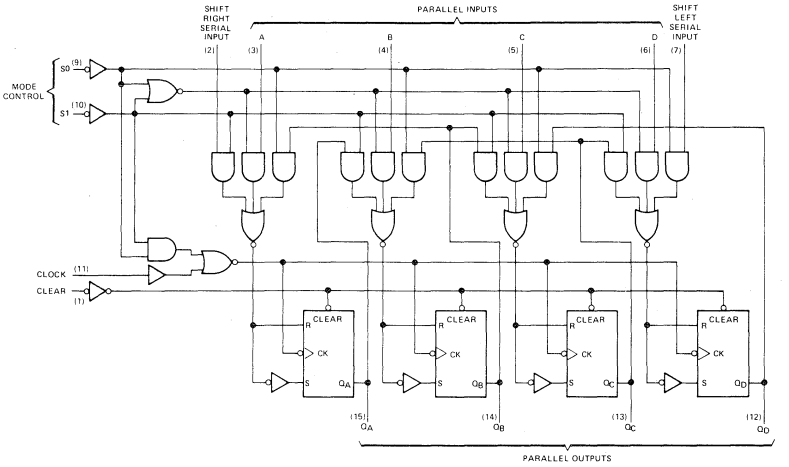
FUNCTION TABLE

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

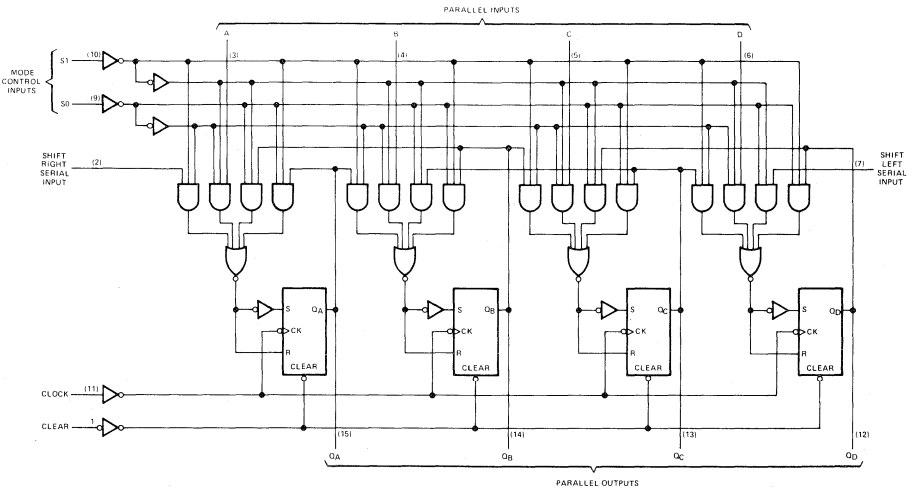
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, Q_D, respectively, before the most-recent ↑ transition of the clock.

functional block diagrams

'194

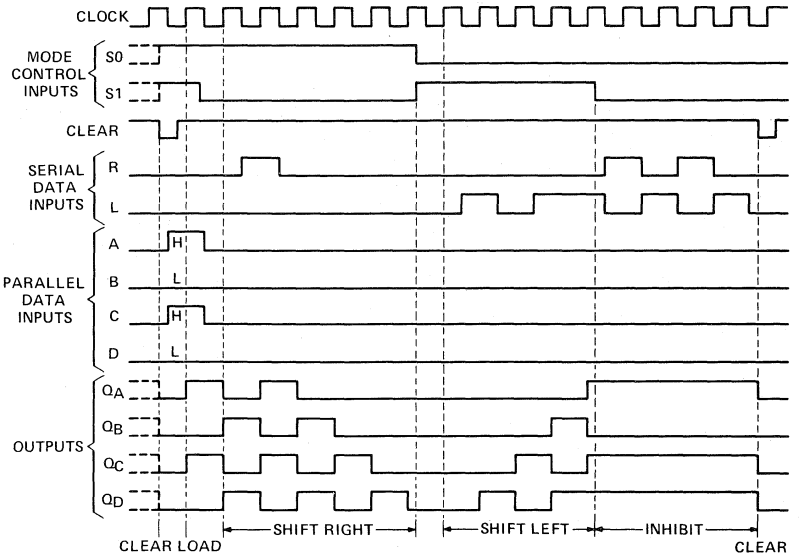


'LS194, 'S194

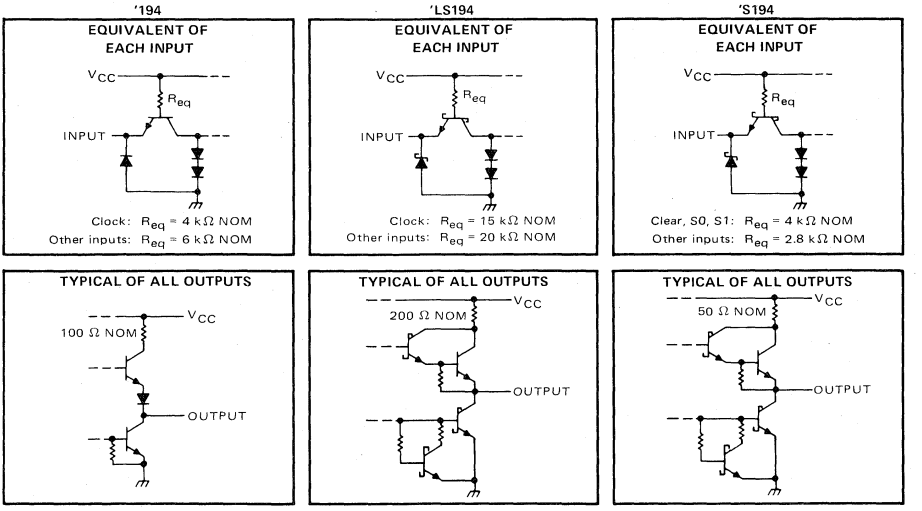


▷ . . . . dynamic input activated by a transition from a high level to a low level.

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54194 . . . . . −55°C to 125°C
SN74194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminat.

recommended operating conditions

		SN54194			SN74194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54194			SN74194			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		39	63		39	63	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS194 . . . . . −55°C to 125°C
SN74LS194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54LS194			SN74LS194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup}	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN54LS194			SN74LS194			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max	V_{IH} = 2 V,	I_{OL} = 4 mA		0.25	0.4				V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current, Clock input	V_{CC} = MAX,	V_I = 0.4 V				−0.44			−0.44	mA
	Low-level input current, Other inputs						−0.36			−0.36	
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2			12	20		12	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	20	28		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			36	54	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			27	41	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			31	47	ns

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S194 . . . . . −55°C to 125°C
SN74S194 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54S194			SN74S194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		70	0		70	MHz
Width of clock pulse, $t_{w(clock)}$		7			7			ns
Width of clear pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup}	Mode control	8			8			ns
	Serial and parallel data	5			5			ns
	Clear inactive-state	9			9			ns
Hold time at any input, t_{hold}		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

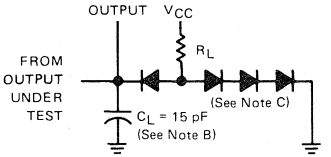
PARAMETER		TEST CONDITIONS†		SN54S194			SN74S194			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA			0.5			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			50			50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−2			−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		85	135		85	135	mA
		V_{CC} = MAX, T_A = 125°C, See Note 2	SN54S194N			99				
			SN54S194W			110				

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of short-circuit should not exceed one second.
NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 280 Ω, See Figure 1	70	105		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		4	8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		4	11	16.5	ns

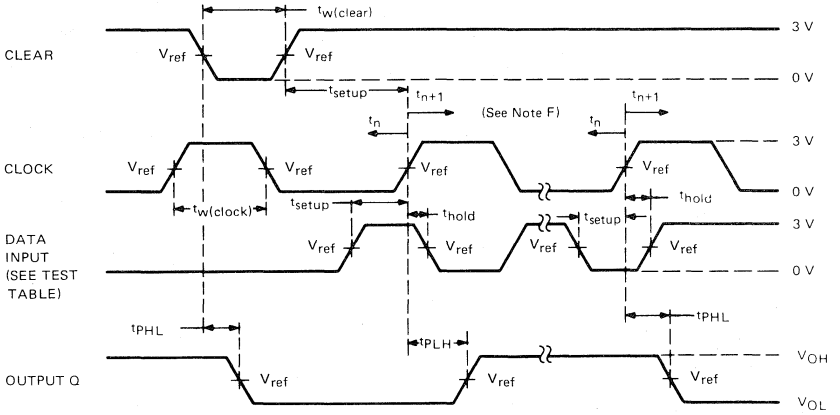
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ 1 MHz. For '194, $t_r \leq 7$ ns and $t_f \leq 7$ ns. For 'LS194, $t_r \leq 15$ ns and $t_f \leq 6$ ns. For 'S194, $t_r \leq 2.5$ ns and $t_f \leq 2.5$ ns. When testing f_{max}, vary PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. For '194 and 'S194, $V_{ref} = 1.5$ V; for 'LS194, $V_{ref} = 1.3$ V.

F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

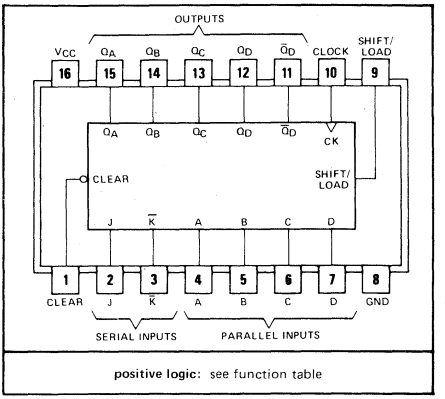
FIGURE 1—SWITCHING TIMES

TYPES SN54195, SN54LS195, SN54S195, SN74195, SN74LS195, SN74S195
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7211820, DECEMBER 1972

- Synchronous Parallel Load
- Positive-Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage
- For Use in High-Performance:
  Accumulators/Processors
  Serial-to-Parallel, Parallel-to-Serial Converters

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'195	39 MHz	195 mW
'LS195	28 MHz	50 mW
'S195	105 MHz	375 mW

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (Broadside) Load
Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

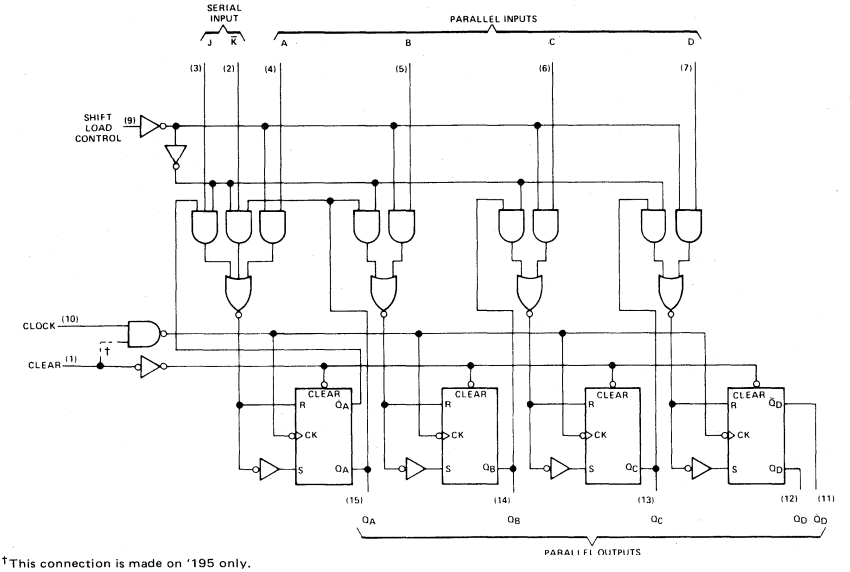
The high-performance 'S195, with a 105-megahertz typical maximum shift-frequency, is particularly attractive for very-high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock

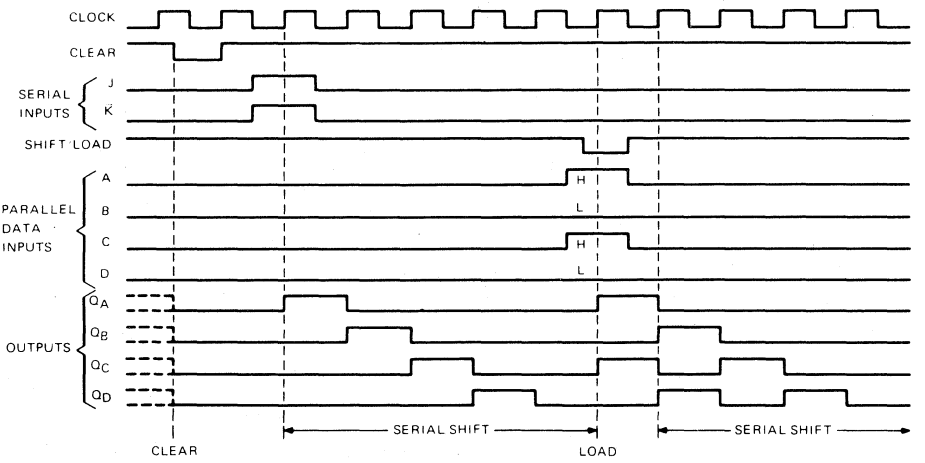
functional block diagram



†This connection is made on '195 only.

. . . dynamic input activated by a transition from a high level to a low level.

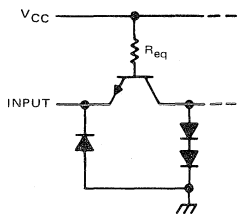
typical clear, shift, and load sequences



schematics of inputs and outputs

'195

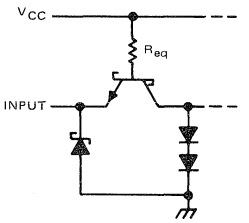
EQUIVALENT OF EACH INPUT



Clock input: R_{eq} = 4 kΩ NOM
All other inputs: R_{eq} = 6 kΩ NOM

'LS195

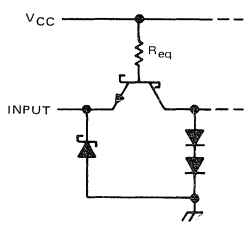
EQUIVALENT OF EACH INPUT



Clock input: R_{eq} = 15 kΩ NOM
All other inputs: R_{eq} = 20 kΩ NOM

'S195

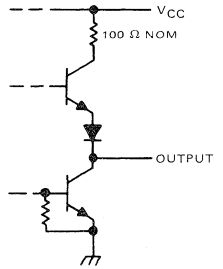
EQUIVALENT OF EACH INPUT



Clear, shift/load: R_{eq} = 4 kΩ NOM
All other inputs: R_{eq} = 2.8 kΩ NOM

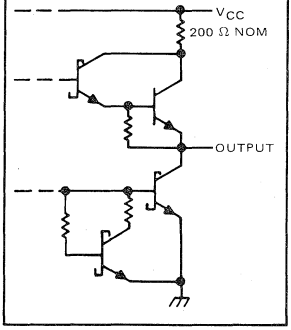
'195

TYPICAL OF ALL OUTPUTS



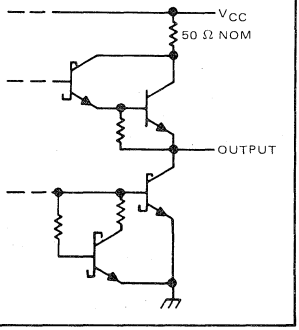
'LS195

TYPICAL OF ALL OUTPUTS



'S195

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN54', SN54LS', SN54S' Circuits	−55°C to 125°C
SN74', SN74LS', SN74S' Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54195			SN74195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				10			10	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54195	−20		−57	mA
			SN74195	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

NOTE: 2. With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	ns

recommended operating conditions

		SN54LS195			SN74LS195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock or clear pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (See Figure 1)				10			10	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS195			SN74LS195			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH} High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current, Clock input	V_{CC} = MAX, V_I = 0.4 V				−0.44			−0.44	mA
	Low-level input current, Other inputs					−0.36			−0.36	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 2			10	17		10	17	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear and then applying a momentary ground, followed by 4.5 V, to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Figure 1	20	28		MHz
t_{PHL} Propagation delay time, high-to-low-level output from clear			31	47	ns
t_{PLH} Propagation delay time, low-to-high-level output from clock			19	29	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			23	35	ns

recommended operating conditions

		SN54S195			SN74S195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}				20			20	mA
Clock frequency, f_{clock}		0		70	0		70	MHz
Width of clock input pulse, $t_{w(clock)}$		7			7			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	8			8			ns
	Serial and parallel data	5			5			
	Clear inactive-state	9			9			
Shift/load release time, $t_{release}$ (see Figure 1)				6			6	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		3			3			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

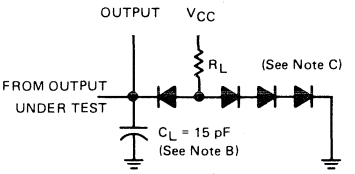
PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −1 mA	SN54S195	2.5	3.4		V
				SN74S195	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2	SN54S195		70	99	mA
				SN74S195		70	109	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

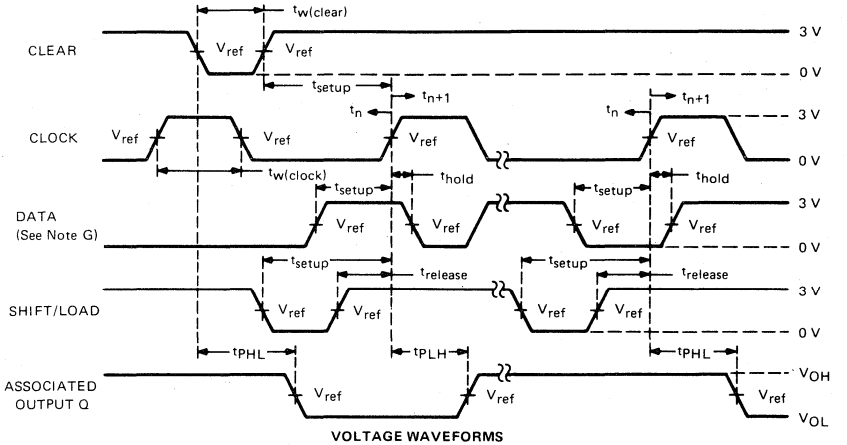
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 280 Ω, See Figure 1	70	105		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			12.5	18.5	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			11	16.5	ns

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES:
A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$ and PRR $\leq$ 1 MHz. For '195, $t_r \leq 7$ ns and $t_f \leq 7$ ns. For 'LS195, $t_r \leq 15$ ns and $t_f \leq 6$ ns. For 'S195, $t_r = 2.5$ ns and $t_f = 2.5$ ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. For '195 and 'S195, $V_{ref} = 1.5$ V; for 'LS195, $V_{ref} = 1.3$ V.
F. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.
G. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.
H. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 1–SWITCHING TIMES

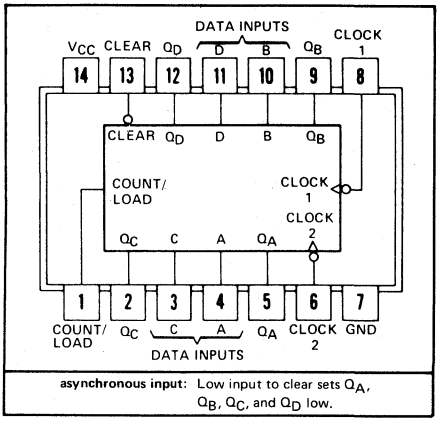
TYPES SN54196, SN54197, SN54LS196, SN54LS197, SN74196, SN74197, SN74LS196, SN74LS197
50/30-MHz PRESETTABLE DECADE OR BINARY COUNTERS/LATCHES

BULLETIN NO. DL-S 7211806, DECEMBER 1972

- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Input Clamping Diodes Simplify System Design
- Output Q_A Maintains Full Fan-out Capability In Addition to Driving Clock-2 Input

TYPES	GUARANTEED COUNT FREQUENCY		TYPICAL POWER DISSIPATION
	CLOCK 1	CLOCK 2	
'196, '197	0-50 MHz	0-25 MHz	240 mW
'LS196, 'LS197	0-30 MHz	0-15 MHz	60 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C, and Q_D low.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter ('196, 'LS196) or a divide-by-two and a divide-by-eight counter ('197, 'LS197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which when taken low sets all outputs low regardless of the states of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 60 milliwatts. Series 54 and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 and 74LS circuits are characterized for operation from 0°C to 70°C.

typical count configurations

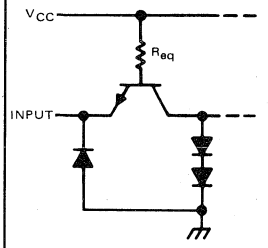
'196 and 'LS196 typical count configurations and function tables are the same as those for '176. See page 370.
'197 and 'LS197 typical count configurations and function tables are the same as those for '177. See page 370.

functional block diagrams

'196 and 'LS196 functional block diagram is the same as that for '176. See page 371.
'197 and 'LS197 functional block diagram is the same as that for '177. See page 371.

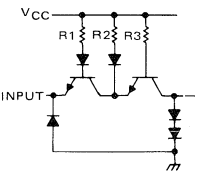
schematics of inputs and outputs

EQUIVALENT OF COUNT/LOAD, CLEAR, AND DATA INPUTS



Count/load, Data: R_{eq} = 4 kΩ NOM
Clear: R_{eq} = 2 kΩ NOM

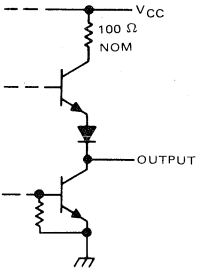
EQUIVALENT OF CLOCK INPUTS



NOMINAL VALUES OF R1, R2, and R3

INPUT	'196	'197
Clock 1	4 kΩ	4 kΩ
Clock 2	3 kΩ	6 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

3

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Intermitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54196, SN54197 Circuits . . . . . −55°C to 125°C
SN74196, SN74197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		SN54196, SN54197			SN74196, SN74197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency	Clock-1 input	0		50	0		50	MHz
	Clock-2 input	0		25	0		25	
Pulse width, t_w	Clock-1 input	10			10			ns
	Clock-2 input	20			20			
	Clear	15			15			
	Load	20			20			
Input hold time, t_{hold}	High-level data	$t_{w(load)}$			$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			$t_{w(load)}$			
Input setup time, t_{setup}	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{enable} (See Note 3)		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54196, SN74196			SN54197, SN74197			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		clear, clock 1					80			80	
		clock 2					120			80	
I_{IL}	Low-level input current	data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		clear					−3.2			−3.2	
		clock 1					−4.8			−4.8	
		clock 2					−6.4			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			48	59		48	59	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

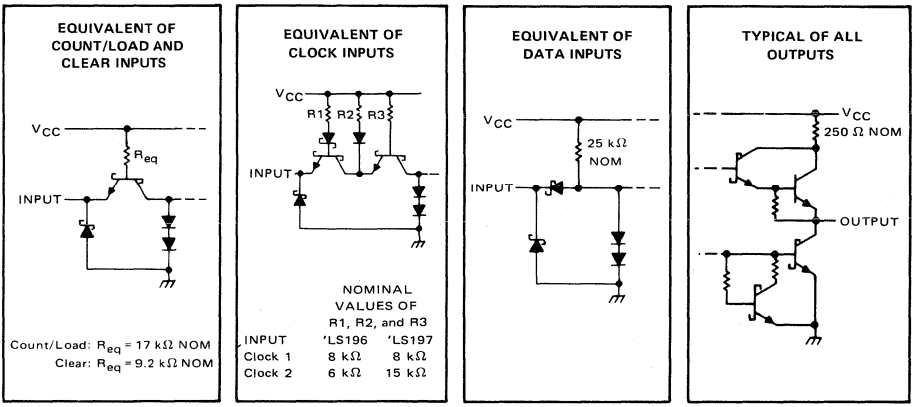
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54196 SN74196			SN54197 SN74197			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 5	50	70		50	70		MHz
t_{PLH}	Clock 1	Q_A			7	12		7	12	ns
t_{PHL}					10	15		10	15	
t_{PLH}	Clock 2	Q_B			12	18		12	18	ns
t_{PHL}					14	21		14	21	
t_{PLH}	Clock 2	Q_C			24	36		24	36	ns
t_{PHL}					28	42		28	42	
t_{PLH}	Clock 2	Q_D			14	21		36	54	ns
t_{PHL}					12	18		42	63	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D			16	24		16	24	ns
t_{PHL}					25	38		25	38	
t_{PLH}	Load	Any			22	33		22	33	ns
t_{PHL}					24	36		24	36	
t_{PHL}	Clear	Any			25	37		25	37	ns

◇f_{max} ≡ maximum input count frequency.
t_{PLH} ≡ propagation delay time, low-to-high-level output.
t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 5: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 (page 374) except that when testing f_{max}, V_{IL} = 0.3 V.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

3

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Intermitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54LS196, SN54LS197 Circuits . . . . . −55°C to 125°C
SN74LS196, SN74LS197 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		SN54LS196, SN54LS197			SN74LS196, SN74LS197			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Count frequency	Clock-1 input	0		30	0		30	MHz
	Clock-2 input	0		15	0		15	
Pulse width, t_w	Clock-1 input	10			10			ns
	Clock-2 input	20			20			
	Clear	15			15			
	Load	20			20			
Input hold time, t_{hold}	High-level data	$t_{w(load)}$			$t_{w(load)}$			ns
	Low-level data	$t_{w(load)}$			$t_{w(load)}$			
Input setup time, t_{setup}	High-level data	10			10			ns
	Low-level data	15			15			
Count enable time, t_{enable} (See Note 3)		20			20			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must both be high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS196 SN54LS197			SN74LS196 SN74LS197			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = $V_{IL\ max}$	I_{OL} = 4 mA¶			0.4				V
			I_{OL} = 8 mA¶						0.5	
I_I	Input current at maximum input voltage	Data, count/load	V_{CC} = MAX, V_I = 5.5 V			0.1			0.1	mA
		Clear, clock 1				0.2			0.2	
		Clock 2 of 'LS196				0.4			0.4	
		Clock 2 of 'LS197				0.2			0.2	
I_{IH}	High-level input current	Data, count/load	V_{CC} = MAX, V_I = 2.7 V			20			20	μA
		Clear, clock 1				40			40	
		Clock 2 of 'LS196				80			80	
		Clock 2 of 'LS197				40			40	
I_{IL}	Low-level output current	Data, count/load	V_{CC} = MAX, V_I = 0.4 V			−0.36			−0.36	mA
		Clear				−0.72			−0.72	
		Clock 1				−2.4			−2.4	
		Clock 2 of 'LS196				−2.8			−2.8	
		Clock 2 of 'LS197				−1.3			−1.3	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 4			12	20		12	20	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Q_A outputs are tested at specified I_{OL} plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while maintaining full fan-out capability.
NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54LS196 SN74LS196			SN54LS197 SN74LS196			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	Clock 1	Q_A	C_L = 15 pF, R_L = 2 kΩ, See Note 6	30	40		30	40		MHz
t_{PLH}	Clock 1	Q_A			8	15		8	15	ns
t_{PHL}					13	20		14	21	
t_{PLH}	Clock 2	Q_B			16	24		12	19	ns
t_{PHL}					22	33		23	35	
t_{PLH}	Clock 2	Q_C			38	57		34	51	ns
t_{PHL}					41	62		42	63	
t_{PLH}	Clock 2	Q_D			12	18		55	78	ns
t_{PHL}					30	45		63	95	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C Q_D			20	30		18	27	ns
t_{PHL}					29	44		29	44	
t_{PLH}	Load	Any			27	41		26	39	ns
t_{PHL}					30	45		30	45	
t_{PHL}	Clear	Any			34	51		34	51	ns

◇f_{max} ≡ maximum input count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 6: Load circuit, input conditions, and voltage waveforms are the same as those shown for the '176, '177 (page 374) except that $t_r \leq 15$ ns, $t_f \leq 6$ ns, and V_{ref} = 1.3 V (as opposed to 1.5 V)

TYPES SN54198, SN54199, SN74198, SN74199
8-BIT SHIFT REGISTERS

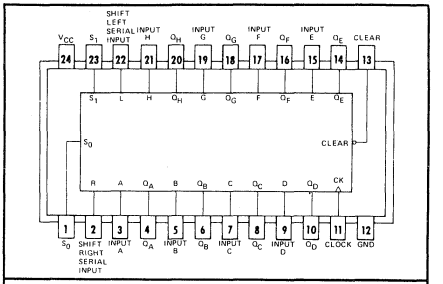
BULLETIN NO. DL-S 7211841, DECEMBER 1972

description

These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 devices are characterized for operation from 0°C to 70°C.

'198
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

SN54198 and SN74198

These bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contain 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

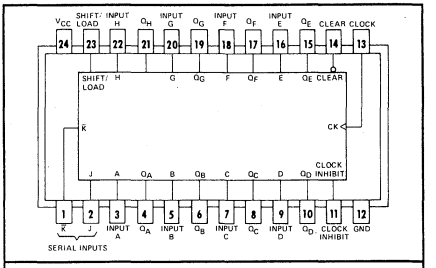
'198
FUNCTION TABLE

INPUTS							OUTPUTS
CLEAR	MODE		CLOCK	SERIAL		PARALLEL	Q_A Q_B ... Q_G Q_H
	S_1	S_0		LEFT	RIGHT	A ... H	
L	X	X	X	X	X	X	L L L L
H	X	X	L	X	X	X	Q_{A0} Q_{B0} Q_{G0} Q_{H0}
H	H	H	↑	X	X	a ... h	a b g h
H	L	H	↑	X	H	X	H Q_{An} Q_{Fn} Q_{Gn}
H	L	H	↑	X	L	X	L Q_{An} Q_{Fn} Q_{Gn}
H	H	L	↑	H	X	X	Q_{Bn} Q_{Cn} Q_{Hn} H
H	H	L	↑	L	X	X	Q_{Bn} Q_{Cn} Q_{Hn} L
H	L	L	X	X	X	X	Q_{A0} Q_{B0} Q_{G0} Q_{H0}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{G0}, Q_{H0} = the level of Q_A, Q_B, Q_G, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc., respectively, before the most-recent ↑ transition of the clock.

SN54199 and SN74199

'199
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

These registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the function table for levels required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

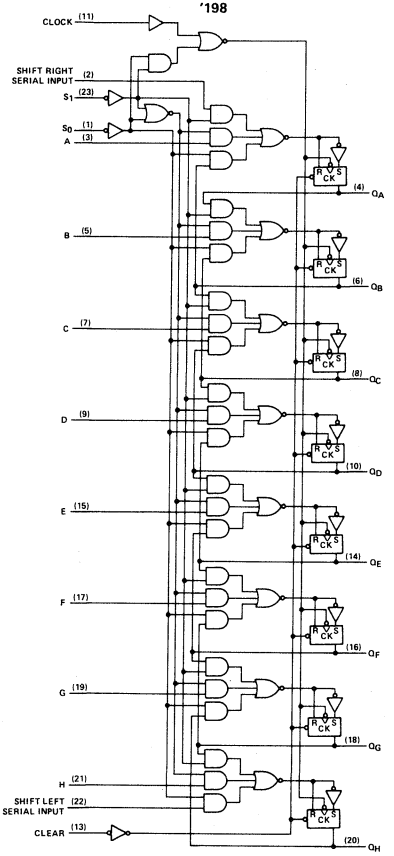
'199
FUNCTION TABLE

INPUTS							OUTPUTS			
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL J	SERIAL $\overline{K}$	PARALLEL A . . . H	Q_A	Q_B	Q_C . . .	Q_H
L	X	X	X	X	X	X	L	L	L	L
H	X	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{H0}
H	L	L	↑	X	X	a . . . h	a	b	c	h
H	H	L	↑	L	H	X	Q_{A0}	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	L	L	X	L	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	H	X	H	Q_{An}	Q_{Bn}	Q_{Gn}
H	H	L	↑	H	L	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Gn}
H	X	H	↑	X	X	X	Q_{A0}	Q_{B0}	Q_{B0}	Q_{H0}

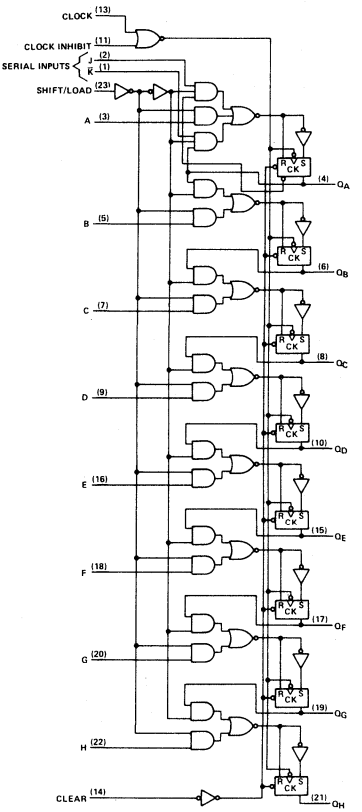
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0}, Q_{B0}, Q_{C0} . . . Q_{H0} = the level of Q_A, Q_B, or Q_C thru Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn} . . . Q_{Gn} = the level of Q_A or Q_B thru Q_G, respectively, before the most-recent ↑ transition of the clock.

functional block diagrams

'198

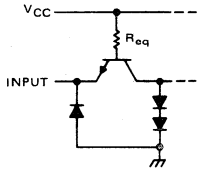


'199



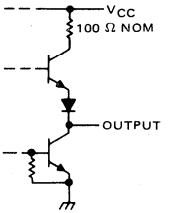
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



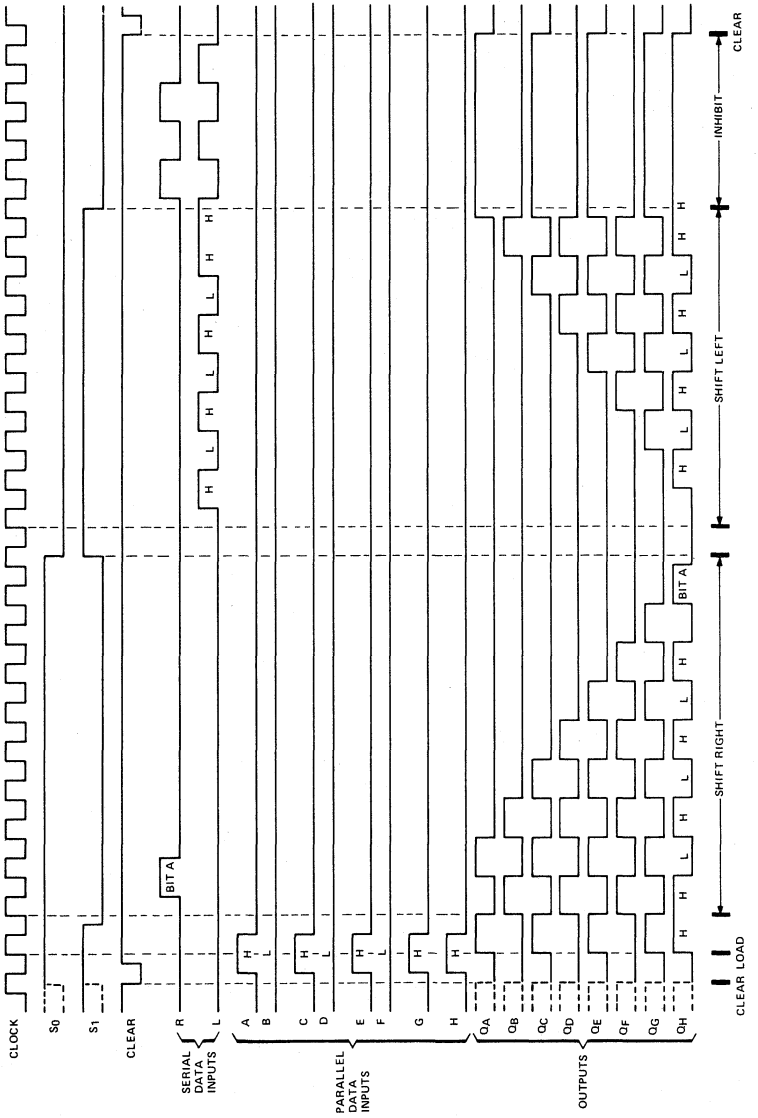
Clear, A thru H: R_{eq} = 6 kΩ NOM
All others: R_{eq} = 4 kΩ NOM

TYPICAL OF ALL OUTPUTS



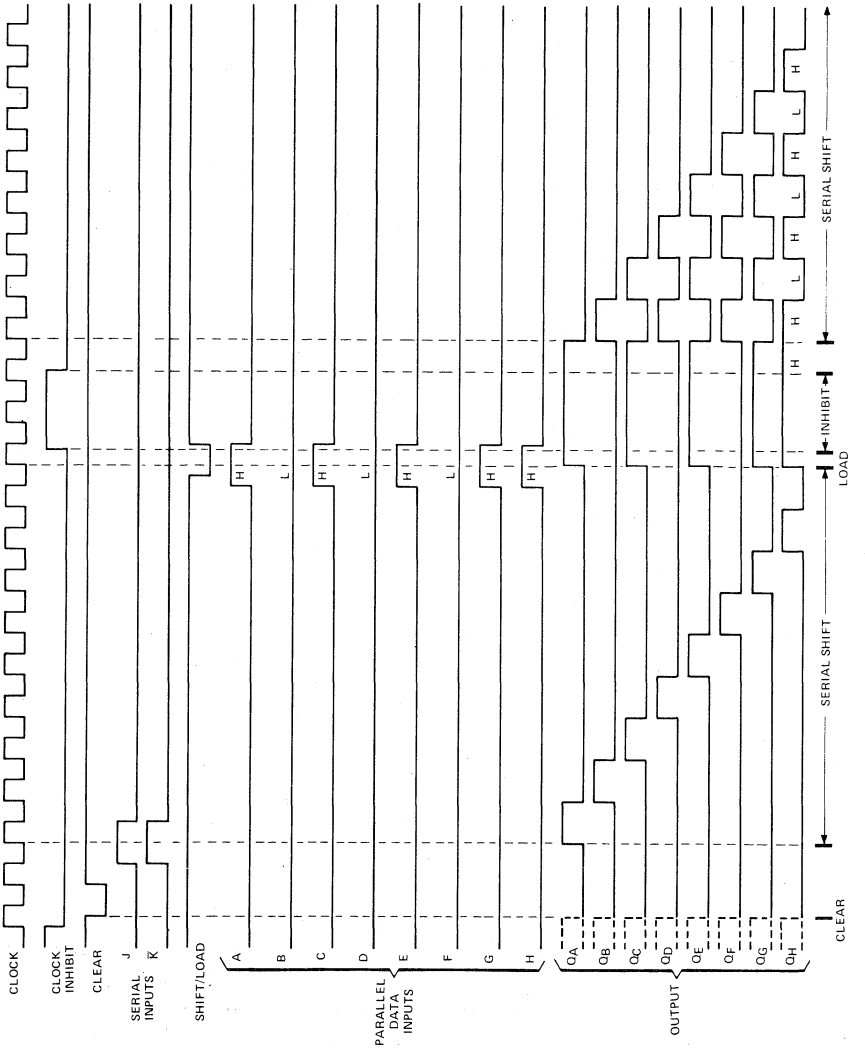
SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences



SN54199, SN74199

typical clear, shift, load, and inhibit sequences



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54198 SN54199			SN74198 SN74199			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)	20			20			ns
Mode-control setup time, t_{setup}	30			30			ns
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Hold time at any input, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54198 SN54199			SN74198 SN74199			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Table Below		72	104		72	116	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN)

TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54198, SN74198	Serial Input, S_0, S_1	Clock	Clear, Inputs A thru H
SN54199, SN74199	J, $\overline{K}$, Inputs A thru H	Clock	Clock inhibit, Clear, Shift/Load

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

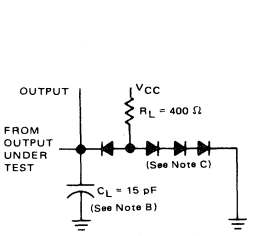
PARAMETER MEASUREMENT INFORMATION

SN54198, SN74198
TEST TABLE FOR SYNCHRONOUS INPUTS

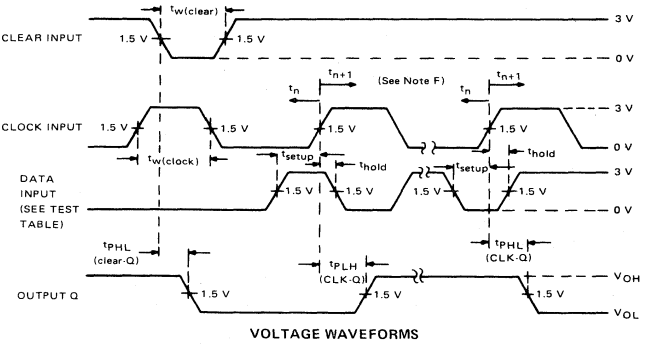
DATA INPUT FOR TEST	S_1	S_0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
E	4.5 V	4.5 V	Q_E at t_{n+1}
F	4.5 V	4.5 V	Q_F at t_{n+1}
G	4.5 V	4.5 V	Q_G at t_{n+1}
H	4.5 V	4.5 V	Q_H at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+8}
R Serial Input	0 V	4.5 V	Q_H at t_{n+8}

SN54199, SN74199
TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	SHIFT/LOAD	OUTPUT TESTED (SEE NOTE E)
A	0 V	Q_A at t_{n+1}
B	0 V	Q_B at t_{n+1}
C	0 V	Q_C at t_{n+1}
D	0 V	Q_D at t_{n+1}
E	0 V	Q_E at t_{n+1}
F	0 V	Q_F at t_{n+1}
G	0 V	Q_G at t_{n+1}
H	0 V	Q_H at t_{n+1}
J and $\overline{K}$	4.5 V	Q_H at t_{n+8}



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq$ 20 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq$ 20 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. A clear pulse is applied prior to each test.
E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.
F. t_n = bit time before clocking transition
t_{n+1} = bit time after one clocking transition
t_{n+8} = bit time after eight clocking transitions

FIGURE 1

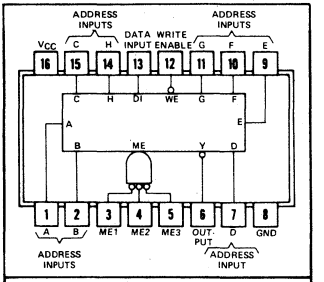
TEXAS INSTRUMENTS

TYPE SN74200
256-BIT READ/WRITE MEMORY WITH 3-STATE OUTPUT

BULLETIN NO. DL-S 7211735, MAY 1972 – REVISED DECEMBER 1972

- For High-Speed Memory Systems
  Access from Memory-Enable Inputs . . . 17 ns Typical
  Access from Address Inputs . . . 42 ns Typical
  Power Dissipation . . . 1.8 mW/Bit Typical
- For New Designs and/or Military Environments, SN54S200 and SN74S200 Are Recommended
- Fully Decoded, Organized as 256 Words of One Bit Each
- Compatible with Most TTL and DTL Logic Circuits
- Multiple Memory-Enable Inputs to Minimize External Decoding

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Data out is complement of data which was applied at data input. See description and function table.

description

This 256-bit active-element memory is a monolithic transistor-transistor logic (TTL) array organized as 256 words of one bit each. It is fully decoded and has three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The SN74200 features a three-state output and is functionally equivalent to the SN74S200.

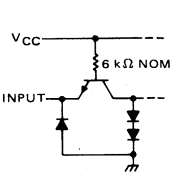
The drive capability of the three-state bus connectable output permits expansion up to 66,304 words of N-bits without additional buffering. See the table below.

WORD CAPACITY vs SERIES 54/74 TTL LOADS

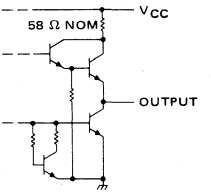
SERIES 54/74 TTL LOADS	MAXIMUM NUMBER OF COMMON OUTPUTS	MAXIMUM NUMBER OF WORDS
1	259	66,304
2	220	56,320
3	180	46,080
4	140	35,840
5	100	25,600
6	60	15,360
7	20	5,120

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



OUTPUT



write cycle

The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

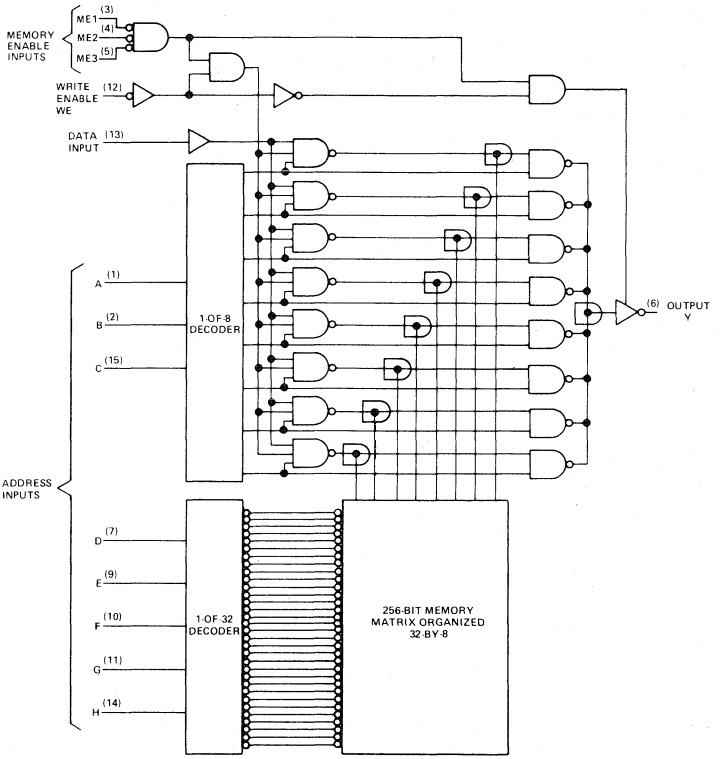
The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level, L = low level, X = irrelevant
†For memory enable: L = all ME inputs low, H = one or more ME input high.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state output voltage	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Width of write-enable pulse, t_w		40◇			ns
		65			
Setup time, t_{setup}	Address-to-write enable	0			ns
	Data-to-write enable	0			
	Memory-enable-to-write-enable	0			
Hold time, t_{hold}	Address-from-write-enable	15			ns
	Data-from-write-enable	15			
	Memory-enable-from-write-enable	0			
Operating free-air temperature, T_A		0		70	°C

◇This condition is recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −10.3 mA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 12 mA				0.4	V
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			40	μA
			V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			95	140	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short-circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all memory enable inputs grounded, all other inputs at 4.5 V, and the output open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Access times from address	C_L = 15 pF, R_L = 400 Ω, See Note 3		45	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output				39	70	
t_{ZH}	Output enable time to high level	Access times from memory enable			20	40	ns
t_{ZL}	Output enable time to low level				14	40	
t_{ZH}	Output enable time to high level	Sense recovery times from write enable			30	50	ns
t_{ZL}	Output enable time to low level				30	50	
t_{HZ}	Output disable time from high level	Disable times from memory enable	C_L = 5 pF, R_L = 400 Ω, See Note 3		7	20	ns
t_{LZ}	Output disable time from low level				8	20	
t_{HZ}	Output disable time from high level	Disable times from write enable			20	40	ns
t_{LZ}	Output disable time from low level				15	40	

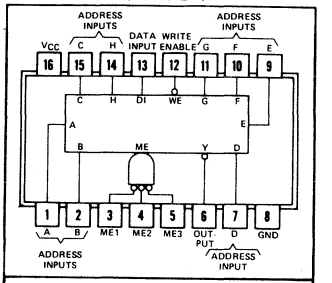
NOTE 3: Load circuit and voltage waveforms are the same as those shown for the SN54S200, SN74S200, except that for the input waveforms: $t_r \leq 7$ ns, $t_f \leq 7$ ns.

TYPES SN54S200, SN74S200
256-BIT READ/WRITE MEMORIES WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211838, DECEMBER 1972

- Schottky-Clamped for High-Speed Memory Systems:
  Access from Memory-Enable Inputs . . . 20 ns Typical
  Access from Address Inputs . . . 31 ns Typical
  Power Dissipation . . . 1.7 mW/Bit Typical
- Three-State Output for Driving Bus-Organized Systems and/or Highly Capacitive Loads
- Fully Decoded, Organized as 256 Words of One Bit Each
- Compatible with Most TTL and DTL Logic Circuits
- Multiple Memory-Enable Inputs to Minimize External Decoding

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)



positive logic: Data out is complement of data which was applied at data input. See description and function table.

description

These 256-bit active-element memories are monolithic transistor-transistor logic (TTL) arrays organized as 256 words of one bit each. They are fully decoded and have three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memories feature P-N-P input transistors which reduce the low-level input current requirement to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The three-state output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs, yet it retains the fast-rise-time characteristic of the TTL totem-pole output. To minimize the possibility that two outputs at opposite logic levels are applied simultaneously to a common bus, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

write cycle

The complement of the information at the data input is written into the selected location when all memory-enable inputs and write-enable input are low. While the write-enable input is low, the output is in the high-impedance state. When a number of outputs are bus-connected, this high-impedance output state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

read cycle

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any one of the memory enable inputs is high, the output will be in the high-impedance state.

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	High Impedance
Read	L	H	Stored Data
Inhibit	H	X	High Impedance

H = high level, L = low level, X = irrelevant
†For memory enable: L = all ME inputs low; H = one or more ME inputs high.

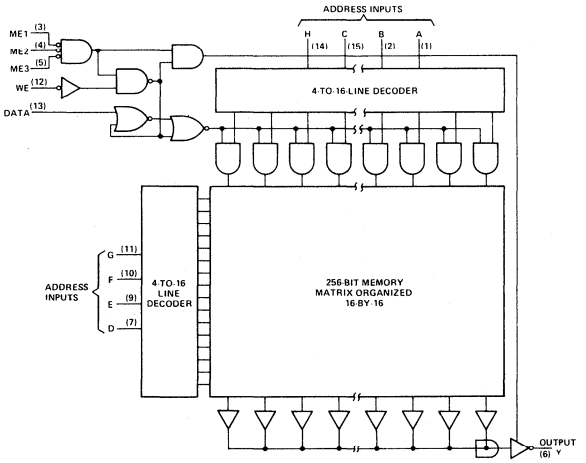
description (continued)

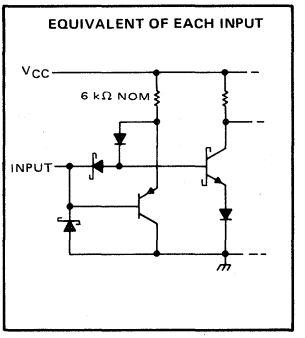
The fast access time of the 'S200 makes it particularly attractive for implementing high-performance memory functions requiring access times of the order of 25-30 nanoseconds. The high capacitive drive capability of the three-state bus-connectable output permits expansion up to 66,304 words of N-bits for the SN74S200 and 32,768 words of N-bits for the SN54S200 without additional output buffering (see table at right). The unique functional capability of the output being at a high impedance during writing and the data input being inhibited during reading means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

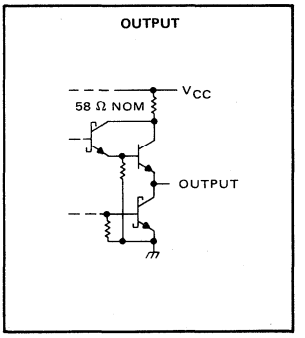
WORD CAPACITY vs SERIES 54/74 LOADS

54/74 TTL LOADS	MAXIMUM NUMBER OF COMMON OUTPUTS		MAXIMUM NUMBER OF WORDS	
	SN54S200	SN74S200	SN54S200	SN74S200
1	129	259	32,768	66,304
2	120	220	30,720	56,320
3	80	180	20,480	46,080
4	40	140	10,240	35,840
5	1	100	256	25,600
6		60		15,360
7		20		5,120

functional block diagram and schematics of inputs and outputs







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S200 . . . . . −55°C to 125°C
SN74S200 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S200			SN74S200			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−5.2			−10.3	mA
Low-level output current, I_{OL}				8			12	mA
Width of write-enable pulse, t_w		50			40			ns
Setup time, t_{setup}	Address-to-write enable	0			0			ns
	Data-to-write enable	0			0			
	Memory-enable-to-write-enable	0			0			
Hold time, t_{hold}	Address-from-write-enable	10			10			ns
	Data-from-write-enable	10			10			
	Memory-enable-from-write-enable	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5	V
						0.5	
$I_{O(off)}$	Off-state (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V,	V_O = 2.4 V			50	μA
			V_O = 0.5 V			−50	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			87	130	mA
		V_{CC} = MAX, T_A = 125°C, See Note 2	SN54S200N			99	
			SN54S200W			110	

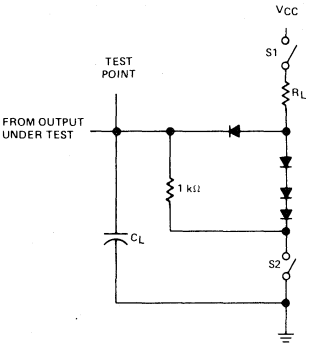
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Duration of the short-circuit should not exceed one second.
NOTES: 1. All voltage values are with respect to network ground terminal.
2. I_{CC} is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5 V, and the output open.

switching characteristics over recommended operating ranges of T_A and V_{CC} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN54S200 TYP‡	SN54S200 MAX	SN74S200 TYP‡	SN74S200 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Access times		33	70	33	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output	from address	C_L = 15 pF,	29	70	29	50	
t_{ZH}	Output enable time to high level	Access times from	R_L = 560 Ω (SN54S'),	21	45	21	35	ns
t_{ZL}	Output enable time to low level	memory enable	400 Ω (SN74S'),	20	45	20	35	
t_{ZH}	Output enable time to high level	Sense recovery times	See Figure 1	19	50	19	40	ns
t_{ZL}	Output enable time to low level	from write enable		17	50	17	40	
t_{HZ}	Output disable time from high level	Disable times from	C_L = 5 pF,	7	30	7	20	ns
t_{LZ}	Output disable time from low level	memory enable	R_L = 560 Ω (SN54S'),	9	30	9	20	
t_{HZ}	Output disable time from high level	Disable times	400 Ω (SN74S'),	13	40	13	30	ns
t_{LZ}	Output disable time from low level	from write enable	See Figure 1	16	40	16	30	

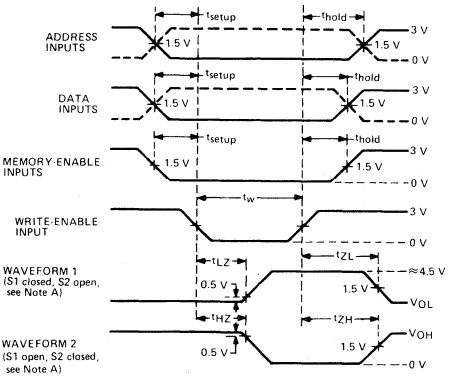
‡*All typical values are at* V_{CC} = 5 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION

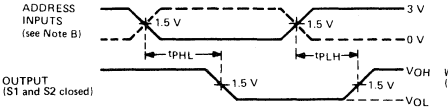


C_L includes probe and jig capacitance.
All diodes are 1N3064.

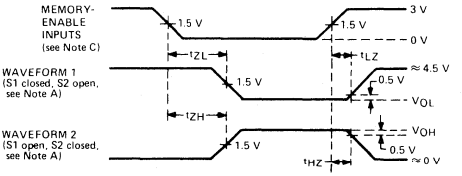
LOAD CIRCUIT



WRITE-CYCLE VOLTAGE WAVEFORMS



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM MEMORY ENABLE VOLTAGE WAVEFORMS

NOTES: A. Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.
B. When measuring delay times from address inputs, the memory-enable inputs are low and the write-enable input is high.
C. When measuring delay times from memory-enable inputs, the address inputs are steady-state and the write-enable input is high.
D. *Input waveforms are supplied by pulse generators having the following characteristics:* $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

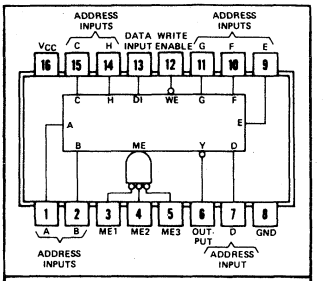
FIGURE 1

TYPES SN54S206, SN74S206
256-BIT READ/WRITE MEMORIES WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7211845, DECEMBER 1972

- Schottky-Clamped for High-Speed Memory Systems
  Access from Memory Enable . . . 16 ns Typical
  Access from Address Inputs . . . 33 ns Typical
  Power Dissipation . . . 1.7 mW/Bit Typical
- P-N-P Inputs Reduce or Eliminate Need for Address Buffers
- Open-Collector Output for Word Expansion
- Guaranteed Operation from −55°C to 125°C (SN54S206)
- Multiple Memory-Enable Inputs to Minimize External Decoding

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE
(TOP VIEW)



positive logic: Data out is complement of data which was applied at data input. See description and function table.

FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	MEMORY ENABLE†	WRITE ENABLE	
Write (Store Complement of Data)	L	L	H
Read	L	H	Stored Data
Inhibit	H	X	H

H = high level, L = low level, X = irrelevant
† For memory enable, L = all ME inputs low; H = one or more ME inputs high.

3

description

This 256-bit active-element memory is a Schottky-clamped TTL array organized as 256 words of one bit each. It is fully decoded and has three gated memory-enable inputs to simplify decoding required to achieve the desired system organization. The memory-enable circuitry is implemented with minimal delay times to compensate for added system decoding which permits the total system read time to closely approach the read cycle time of the 'S206, typically 33 nanoseconds. The read-then-write cycle time is typically 83 nanoseconds. The open-collector output can be bus-connected to other similar outputs to provide word expansion.

The complement of the information at the data input is written into the selected location when all memory-enable inputs and the write-enable input are low. While the write enable input is low, the output is off.

The stored information (complement of information applied at the data input during the write cycle) is available at the output when the write-enable input is high and the three memory-enable inputs are low. When any of the memory-enable inputs are high, the output will be off.

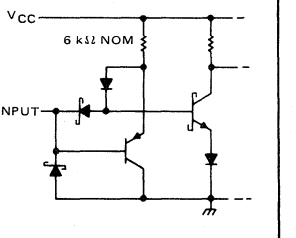
These memories feature P-N-P input transistors which reduce the low-level input current to a maximum of −0.25 milliamperes, only one-eighth that of a normalized Series 54S/74S load factor. Another feature is the unique functional capability of the output being off during writing and the data input being inhibited during reading. This permits the data input and the output to be connected commonly to the input/output data line of a bus-organized system without the need for interface circuits.

functional block diagram

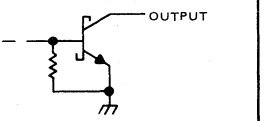
See SN54S200, SN74S200, page 467.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



OUTPUT



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
High-level output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S206 . . . . . −55°C to 125°C
SN74S206 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		SN54S206			SN74S206			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}				5.5			5.5	V
Low-level output current, I_{OL}				8			12	mA
Width of write-enable pulse, t_w		50			40			ns
Setup time, t_{setup}	Address-to-write enable	0			0			ns
	Data-to-write enable	0			0			
	Memory-enable-to-write-enable	0			0			
Hold time, t_{hold}	Address-from-write-enable	10			10			ns
	Data-from-write-enable	10			10			
	Memory-enable-from-write-enable	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			40	μA
			V_{OH} = 5.5 V			250	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−0.25	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			87	130	mA
		V_{CC} = MAX, T_A = 125°C, See Note 2	SN54S206N			99	
			SN54S206W			110	

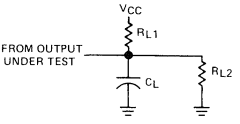
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTES: 1. Voltage values are with respect to network ground terminal.
2. I_{CC} is measured with all memory enable inputs grounded, all other inputs at 4.5 V, and the output open.

switching characteristics over recommended operating ranges of V_{CC} and T_A (unless otherwise noted)

PARAMETER§		TEST CONDITIONS	SN54S206			SN74S206			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH} / t_{PHL}	Access times from address	C_L = 15 pF, R_{L1} = 560 Ω for SN54S', 400 Ω for SN74S', R_{L2} = 1 kΩ, See Figure 1		37 / 29	75 / 75		37 / 29	55 / 55	ns
t_{PLH}	Disable time from memory enable			9	35		9	25	ns
t_{PHL}	Enable time from memory enable			16	45		16	35	ns
t_{PLH}	Disable time from write enable			16	45		16	35	ns
t_{SR}	Sense-recovery time			18	50		18	40	ns

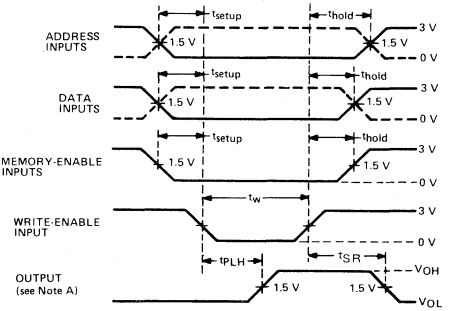
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output, t_{SR} ≡ recovery time for valid data after writing.

PARAMETER MEASUREMENT INFORMATION

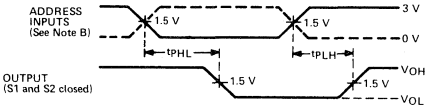


C_L includes probe and jig capacitance.

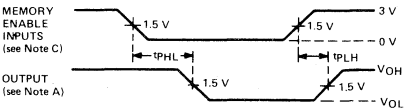
LOAD CIRCUIT



WRITE-CYCLE VOLTAGE WAVEFORMS



ACCESS TIME FROM ADDRESS INPUTS VOLTAGE WAVEFORMS



ACCESS (ENABLE) TIME AND DISABLE TIME FROM MEMORY ENABLE VOLTAGE WAVEFORMS

NOTES: A. Waveform shown is for the output with internal conditions such that the output is low except when disabled.
B. When measuring delay times from address inputs, the memory-enable inputs are low and the write-enable input is high.
C. When measuring delay times from memory-enable inputs, the address inputs are steady-state and the write-enable input is high.
D. Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz, and $Z_{out} \approx 50\ \Omega$.

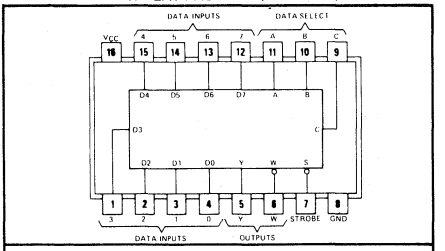
TYPES SN54251, SN54LS251, SN54S251, SN74251, SN74LS251, SN74S251
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211834, DECEMBER 1972

- Three-State Versions of '151, 'LS151, 'S151
- Three-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Permit Multiplexing from N-lines to One Line
- Complementary Outputs Provide True and Inverted Data
- Fully Compatible with Most TTL and DTL Circuits

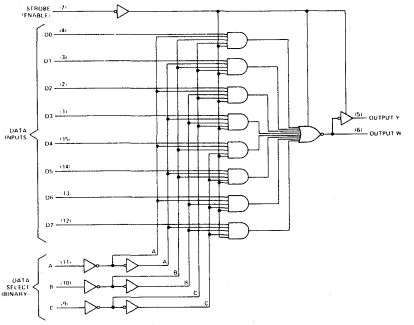
TYPE	MAX NO. OF COMMON OUTPUTS	TYPICAL AVG PROP DELAY TIME (D TO Y)	TYPICAL POWER DISSIPATION
SN54251	49	17 ns	250 mW
SN74251	129	17 ns	250 mW
SN54LS251	19	17 ns	35 mW
SN74LS251	19	17 ns	35 mW
SN54S251	39	8 ns	275 mW
SN74S251	129	8 ns	275 mW

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

functional block diagram



description

These monolithic data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time. The SN54251 and SN74251 have output clamp diodes to attenuate reflections on the bus line.

FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = low logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54251 . . . . . −55°C to 125°C
SN74251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54251			SN74251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−5.2	mA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			40	μA
			V_O = 0.4 V			−40	
V_O	Output clamp voltage	V_{CC} = MAX, V_{IH} = 4.5 V	I_O = −12 mA			−1.5	V
			I_O = 12 mA			V_{CC}+1.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open	All inputs at 4.5 V,		38	62	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 50 pF, R_L = 400 Ω, See Note 2		29	45	ns
t_{PHL}					28	45	
t_{PLH}	A, B, or C (3 levels)	W			20	33	ns
t_{PHL}					21	33	
t_{PLH}	Any D	Y			17	28	ns
t_{PHL}					18	28	
t_{PLH}	Any D	W			10	15	ns
t_{PHL}					9	15	
t_{ZH}	Strobe	Y			17	27	ns
t_{ZL}					26	40	
t_{ZH}	Strobe	W			17	27	ns
t_{ZL}					24	40	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 400 Ω, See Note 2		5	8	ns
t_{LZ}					15	23	
t_{HZ}	Strobe	W			5	8	ns
t_{LZ}					15	23	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 2: See load circuits and waveforms on page 148.

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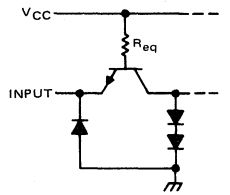
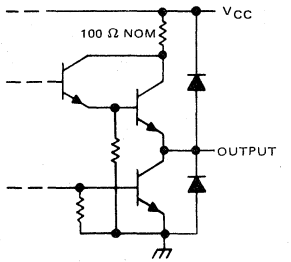
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Select: R_{eq} = 6 kΩ NOM
Other inputs: R_{eq} = 4 kΩ NOM

TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS251 . . . . . 55°C to 125°C
SN74LS251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS251			SN74LS251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS251			SN74LS251			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OH} = MAX	2.5	3.4		2.7	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = MAX,	V_{IH} = 2 V, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 3	Condition A		6.1	10		6.1	10	mA
			Condition B		7.1	12		7.1	12	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the outputs open and all data and select inputs at 4.5 V under the following conditions:
A. Strobe grounded.
B. Strobe at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 4		29	45	ns
t_{PHL}					28	45	
t_{PLH}	A, B, or C (3 levels)	W			20	33	ns
t_{PHL}					21	33	
t_{PLH}	Any D	Y			17	28	ns
t_{PHL}					18	28	
t_{PLH}	Any D	W			10	15	ns
t_{PHL}					9	15	
t_{ZH}	Strobe	Y			17	27	ns
t_{ZL}					26	40	
t_{ZH}	Strobe	W			17	27	ns
t_{ZL}					24	40	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 2 kΩ, See Note 4		30	45	ns
t_{LZ}					15	25	
t_{HZ}	Strobe	W			30	45	ns
t_{LZ}					15	25	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 4: See load circuits and waveforms on page 149.

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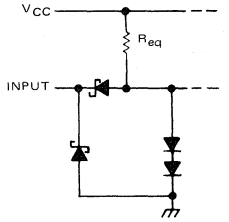
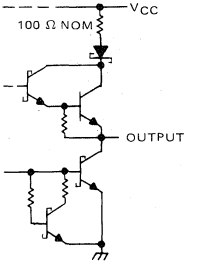
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



A, B, C, S: R_{eq} = 20 kΩ NOM
D0 thru D7: R_{eq} = 17 kΩ NOM

TYPICAL OF BOTH OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S251 . . . . . −55°C to 125°C
SN74S251 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S251			SN74S251			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA					−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		SN54S'	2.4	3.4		V
				SN74S'	2.4	3.2		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA					0.5	V
$I_{O(off)}$	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V				50	μA
			V_O = 0.5 V				−50	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V					50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V					−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX			−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, All outputs open	All inputs at 4.5 V,			55	85	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

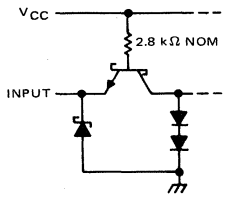
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A, B, or C (4 levels)	Y	C_L = 15 pF, R_L = 280 Ω, See Note 2		12	18	ns
t_{PHL}					13	19.5	
t_{PLH}	A, B, or C (3 levels)	W			10	15	ns
t_{PHL}					9	13.5	
t_{PLH}	Any D	Y			8	12	ns
t_{PHL}					8	12	
t_{PLH}	Any D	W			4.5	7	ns
t_{PHL}					4.5	7	
t_{ZH}	Strobe	Y	C_L = 50 pF, R_L = 280 Ω, See Note 2		13	19.5	ns
t_{ZL}					14	21	
t_{ZH}	Strobe	W			13	19.5	ns
t_{ZL}					14	21	
t_{HZ}	Strobe	Y	C_L = 5 pF, R_L = 280 Ω, See Note 2		5.5	8.5	ns
t_{LZ}					9	14	
t_{HZ}	Strobe	W			5.5	8.5	ns
t_{LZ}					9	14	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 2: See load circuits and waveforms on page 148.

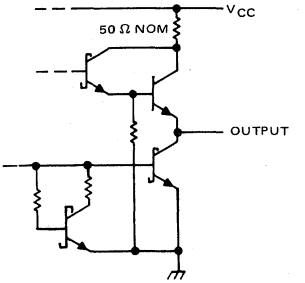
3

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF BOTH OUTPUTS

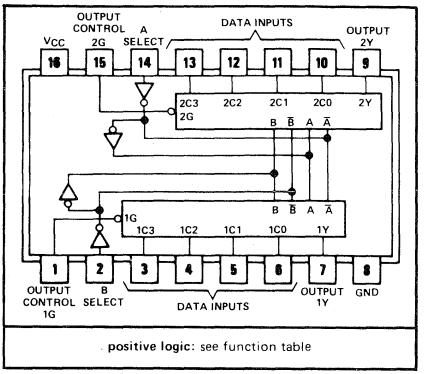


TYPES SN54LS253, SN74LS253
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211790, SEPTEMBER 1972

- Three-State Version of SN54LS153/SN74LS153
- Schottky-Diode-Clamped Transistors
- Permits Multiplexing from N Lines to 1 Line
- Performs Parallel-to-Serial Conversion
- Typical Average Propagation Delay Times:
  Data Input to Output . . . 12 ns
  Control Input to Output . . . 16 ns
  Select Input to Output . . . 21 ns
- Fully Compatible with Most TTL and DTL Circuits
- Low Power Dissipation . . . 35 mW Typical (Enabled)

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

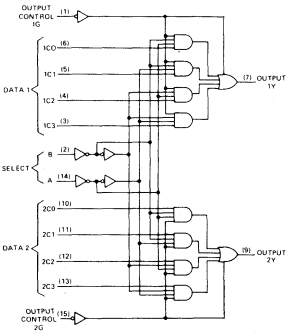
logic

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant, Z = high impedance (off)

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS253 . . . . . −55°C to 125°C
SN74LS253 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS253			SN74LS253			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS253			SN74LS253			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.6			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA			0.4				V
			I_{OL} = 8 mA						0.5	
$I_{O(off)}$	Off-State (high-impedance state) output current	V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.36			−0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	Condition A		7	12		7	12	mA
			Condition B		8.5	14		8.5	14	

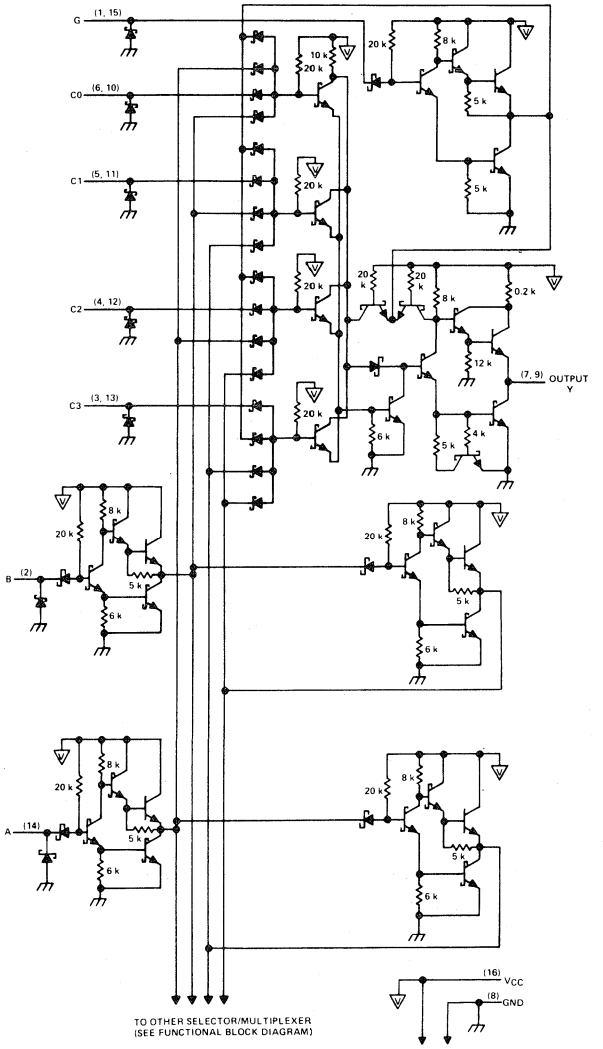
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the outputs open under the following conditions:
A. All inputs grounded.
B. Output control at 4.5 V, all inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	C_L = 15 pF, R_L = 2 kΩ, See Note 3		11	18	ns
t_{PHL}					13	20	
t_{PLH}	Select	Y			20	30	ns
t_{PHL}					21	32	
t_{ZH}	Output Control	Y			11	18	ns
t_{ZL}					15	23	
t_{HZ}	Output Control	Y	C_L = 5 pF, R_L = 2 kΩ, See Note 3		27	41	ns
t_{LZ}					12	19	

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{ZH} ≡ Output enable time to high level
t_{ZL} ≡ Output enable time to low level
t_{HZ} ≡ Output disable time from high level
t_{LZ} ≡ Output disable time from low level
NOTE 3: Load circuit and waveforms are shown on page 149.

schematic (each selector/multiplexer, and the common select section)



▽ . . . V_{CC} bus

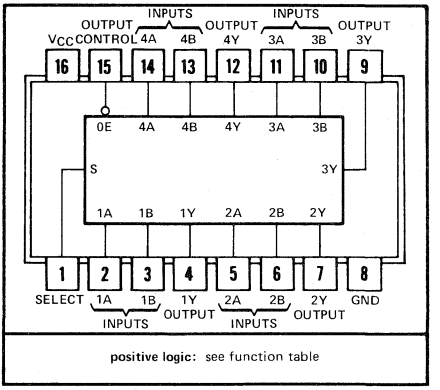
Resistor values shown are nominal and in ohms.

TYPES SN54S257, SN54S258, SN74S257, SN74S258
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211734, MAY 1972 – REVISED DECEMBER 1972

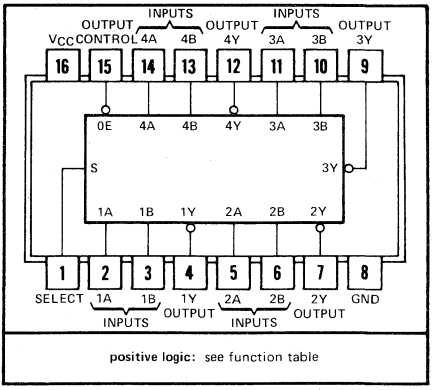
- Three-State Outputs Interface Directly with System Bus
- Schottky-Clamped for Significant Improvement in A-C Performance
- Fully Compatible with Most TTL Functions Including MSI
- Same Pin Assignments as SN54S157, SN74S157 and SN54S158, SN74S158
- Provides Bus Interface from Multiple Sources in High-Performance Systems
- SN54S257 and SN54S258 are Guaranteed for Operation Over the Full Military Temperature Range of −55°C to 125°C

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)
SN54S257, SN74S257



positive logic: see function table

SN54S258, SN74S258



positive logic: see function table

description

These Schottky-clamped high-performance multiplexers feature three-state outputs which can interface directly with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at a high-impedance state) the low impedance of the single enabled output will drive the bus line to a high or low logic level.

This three-state output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

The typical propagation delay times from data input to output average only 4.8 nanoseconds for the SN54S257, SN74S257 and only 4 nanoseconds for the SN54S258, SN74S258. Also, to minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output-enable circuitry is designed such that the output disable times are shorter than the output enable times.

FUNCTION TABLE

INPUTS				OUTPUT Y	
OUTPUT CONTROL	SELECT	A	B	SN54S257 SN74S257	SN54S258 SN74S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Off-state output voltage . . . . . 5.5 V
Operating free-air temperature range: SN54S257, SN54S258 Circuits . . . . . −55°C to 125°C
SN74S257, SN74S258 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. All voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S257, SN54S258			SN74S257, SN74S258			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−2			−6.5	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54S257, SN74S257			SN54S258, SN74S258			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX,	SN54S'	2.4	3.4		2.4	3.4		V
				SN74S'	2.4	3.2		2.4	3.2		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = 20 mA				0.5			0.5	V
$I_{O(off)}$	Off-state (high-impedance state) output current		V_{CC} = MAX, V_{IH} = 2 V	V_O = 2.4 V			50			50	μA
				V_O = 0.5 V			−50			−50	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	S input	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
		Any other					50			50	
I_{IL}	Low-level input current	S input	V_{CC} = MAX, V_I = 0.5 V				−4			−4	mA
		Any other					−2			−2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−40		−100	−40		−100	mA
I_{CC}	Supply current	All outputs high	V_{CC} = MAX, See Note 2			44	68		36	56	mA
		All outputs low				60	93		52	81	
		All outputs off				64	99		56	87	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTE 2: I_{CC} is measured with all outputs open and all possible inputs grounded while achieving the stated output conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 280 Ω

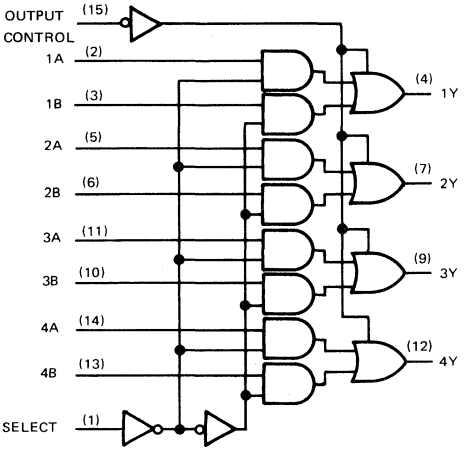
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54S257, SN74S257			SN54S258, SN74S258			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Data	Any	C_L = 15 pF, See Note 3		5	7.5		4	6	ns
t_{PHL}					4.5	6.5		4	6	
t_{PLH}	Select	Any			8.5	15		8	12	ns
t_{PHL}					8.5	15		7.5	12	
t_{ZH}	Output Control	Any			13	19.5		13	19.5	ns
t_{ZL}					14	21		14	21	
t_{HZ}	Output Control	Any	C_L = 5 pF, See Note 3		5.5	8.5		5.5	8.5	ns
t_{LZ}					9	14		9	14	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
t_{ZH} ≡ output enable time to high level
t_{ZL} ≡ output enable time to low level
t_{HZ} ≡ output disable time from high level
t_{LZ} ≡ output disable time from low level

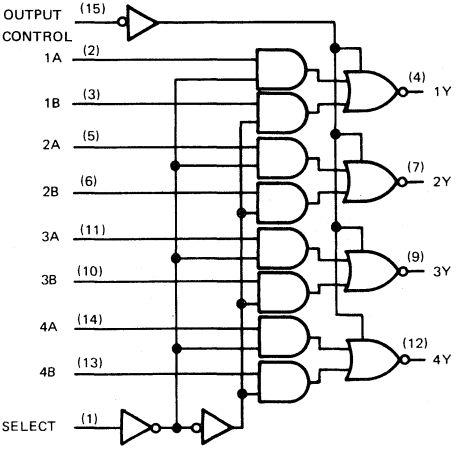
NOTE 3: Load circuit and waveforms are shown on page 148.

functional block diagrams

SN54S257, SN74S257

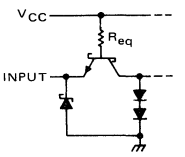


SN54S258, SN74S258



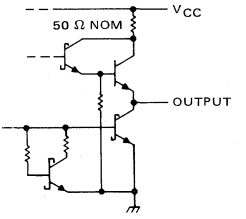
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Select: R_{eq} = 1.4 kΩ NOM
All other inputs: R_{eq} = 2.8 kΩ NOM

TYPICAL OF ALL OUTPUTS

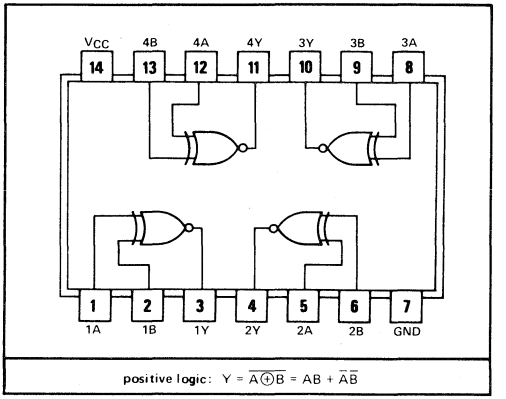


TYPES SN54LS266, SN74LS266
QUADRUPLE 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

BULLETIN NO. DL-S 7211843, DECEMBER 1972

- Can Be Used as a 4-Bit Digital Comparator
- Input Clamping Diodes Simplify System Design
- Fully Compatible with Most TTL and DTL Circuits

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

H = high level, L = low level

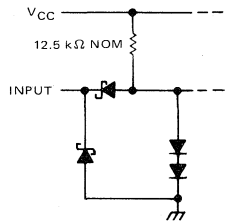
description

The 'LS266 is comprised of four independent 2-input exclusive-NOR gates with open-collector outputs. The open-collector outputs permit tying outputs together for multiple-bit comparisons.

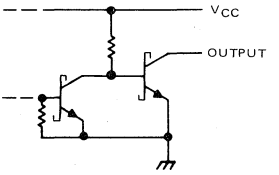
3

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Operating free-air temperature range: SN54LS266 . . . . . −55°C to 125°C
SN74LS266 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS266			SN74LS266			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS266			SN74LS266			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, V_{OH} = 5.5 V			100			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OL} = MAX		0.25	0.4		0.35	0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			0.2			0.2	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−0.6			−0.6	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		8	13		8	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is measured with one input of each gate at 4.5 V, the other inputs grounded, and the outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Other input low	C_L = 15 pF, R_L = 2 kΩ, See Note 3		18	30	ns
t_{PHL}					18	30	
t_{PLH}	A or B	Other input high			18	30	ns
t_{PHL}					18	30	

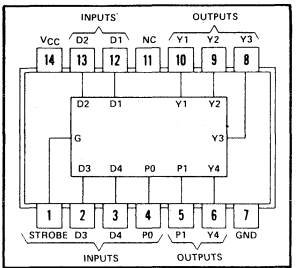
¶t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 149.

TYPES SN54278, SN74278
4-BIT CASCADABLE PRIORITY REGISTERS

BULLETIN NO. DL-S 7211729, MAY 1972–REVISED DECEMBER 1972

- **Latched Data Inputs Serve as Buffer Register and Can also:**
  Synchronize Data Acquisition
  "Debounce" Mechanical Switch Input
- **Cascading Input P0 and Output P1 Provides "Busy"Signal Inhibiting All Lower-Order Bits**
- **Full TTL Compatibility**
- **Use for:**
  Priority Interrupt
  Synchronous Priority Line Selection

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC–No internal connection

description

The SN54278 and SN74278 each consist of four data latches, full priority output gating, and a cascading gate. The highest-order data applied at a D latch input is transferred to the appropriate Y output while the strobe input is high, and when the strobe goes low all data is latched. The cascading input P0 is fully overriding and on the highest-order package this input must be held at a low logic level. The P1 output is intended for connection to the P0 input of the next lower-order package and will provide a "busy" (high-level) signal to inhibit all subsequent lower-order packages.

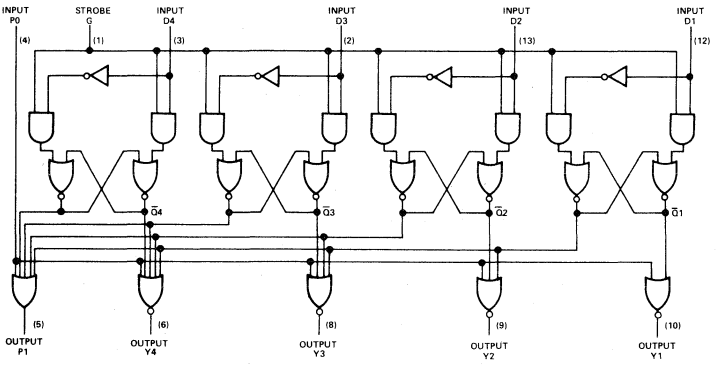
After the overriding P0 input, the order of priority is D1, D2, D3, and D4, respectively, within the package.

FUNCTION TABLE

INPUTS						INTERNAL LATCH NODES				OUTPUTS				
P0	G	D1	D2	D3	D4	$\bar{Q}1$	$\bar{Q}2$	$\bar{Q}3$	$\bar{Q}4$	Y1	Y2	Y3	Y4	P1
L	H	H	X	X	X	L	X	X	X	H	L	L	L	H
L	H	L	H	X	X	H	L	X	X	L	H	L	L	H
L	H	L	L	H	X	H	H	L	X	L	L	H	L	H
L	H	L	L	L	H	H	H	H	L	L	L	L	H	H
L	H	L	L	L	L	H	H	H	H	L	L	L	L	L
L	L	X	X	X	X	Latched when G goes low				Same function of $\bar{Q}$ nodes as on 1st 5 lines				
H	L	X	X	X	X					L	L	L	L	H
H	H	Internal $\bar{Q}$ levels are same function of D inputs as on first 5 lines								L	L	L	L	H

H = high level, L = low level, X = irrelevant

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54278 Circuits . . . . . −55°C to 125°C
SN74278 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the strobe input and any of the four data inputs.

recommended operating conditions

	SN54278			SN74278			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Data setup time, t_{setup} (see Figure 1)	20			20			ns
Data hold time, t_{hold} (see Figure 1)	5			5			ns
Strobe pulse width, t_w (see Figure 1)	20			20			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	Any D input	V_{CC} = MAX, V_I = 2.4 V				80	μA
		P0 input					200	
		G input					320	
I_{IL}	Low-level input current	Any D input	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
		P0 input					−8	
		G input					−12.8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54278	−18		−55	mA
				SN74278	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			55	80	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the P0 input grounded, all other inputs at 4.5 V, and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

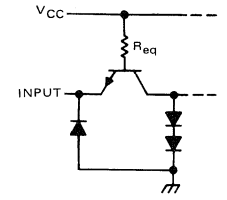
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORMS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	A and C (with strobe high)	C_L = 15 pF, R_L = 400 Ω, See Figure 1			30	ns
t_{PHL}							39	
t_{PLH}	Data	Y	A and D (with strobe high)				38	ns
t_{PHL}							31	
t_{PLH}	Data	P1	A and E (with strobe high)				46	ns
t_{PHL}							39	
t_{PLH}	Strobe	Any Y	B and C or B and D				30	ns
t_{PHL}							31	
t_{PLH}	Strobe	P1	B and E				38	ns
t_{PHL}							42	
t_{PLH}	P0	P1	F and G				23	ns
t_{PHL}							30	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

schematics of inputs and outputs

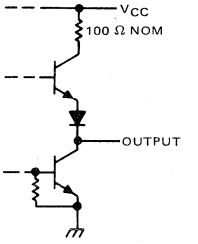
3

EQUIVALENT OF EACH INPUT

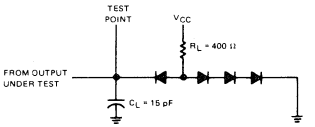


Any D: R_{eq} = 2.5 kΩ NOM
P0: R_{eq} = 1 kΩ NOM
G: R_{eq} = 0.6 kΩ NOM

TYPICAL OF ALL OUTPUTS

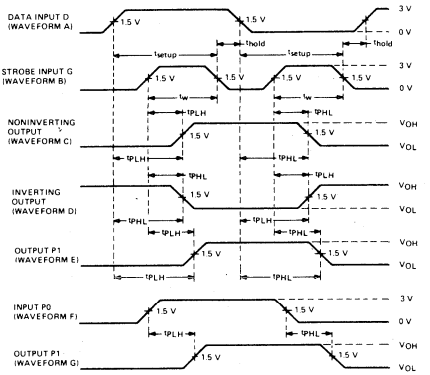


PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance.
All diodes are 1N3064.

LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTE: Input pulses are supplied by a generator having the following characteristics: $t_r \leq 7$ ns, $t_f \leq 7$ ns, PRR ≤ 1 MHz, $Z_{out} \approx 50\ \Omega$.

FIGURE 1–SWITCHING TIMES

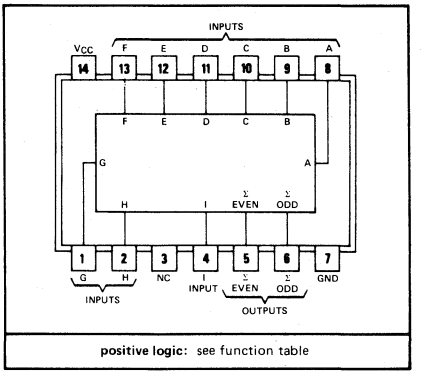
TEXAS INSTRUMENTS

TYPES SN54S280, SN74S280
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

BULLETIN NO. DL-S 7211829, DECEMBER 1972

- Generates Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bits
- Can Be Used to Upgrade Existing Systems using MSI Parity Circuits
- Typical Data-to-Output Delay of Only 14 ns

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC—No internal connection

FUNCTION TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

description

These universal, monolithic, nine-bit parity generators/checkers utilize Schottky-clamped Series 54S/74S TTL high-performance circuitry and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading as shown under typical application data.

The 'S280 can be used to upgrade the performance of most systems utilizing the '180 parity generator/checker. Although the 'S280 is implemented without expander inputs, the corresponding function is provided by the availability of an input at pin 4 and the absence of any internal connection at pin 3. This permits the 'S280 to be substituted for the '180 in existing designs to produce an identical function even if 'S280's are mixed with existing '180's.

The 'S280 is fully compatible with most other TTL and DTL circuits. Input buffers are provided so that each input represents only one normalized Series 54S/74S load, and full fan-out to 10 normalized Series 54S/74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normalized Series 54S/74S loads is provided at high logic levels to facilitate connection of unused inputs to used inputs. Typical power dissipation is 335 milliwatts.

The SN54S280 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74S280 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Operating free-air temperature range:	SN54S280	−55°C to 125°C
	SN74S280	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54S280			SN74S280			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−1	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −1 mA	SN54S'	2.5	3.4		V
			SN74S'	2.7	3.4		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−2	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	SN54S280		67	99	mA
			SN74S280		67	105	
		V_{CC} = MAX, T_A = 125°C, See Note 2	SN54S280N			94	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

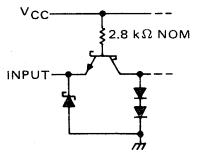
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Σ Even	C_L = 15 pF, R_L = 180 Ω, See Note 3		14	21	ns
t_{PHL}					11.5	18	
t_{PLH}	Data	Σ Odd			14	21	ns
t_{PHL}					11.5	18	

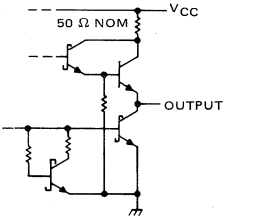
¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

schematics of inputs and outputs

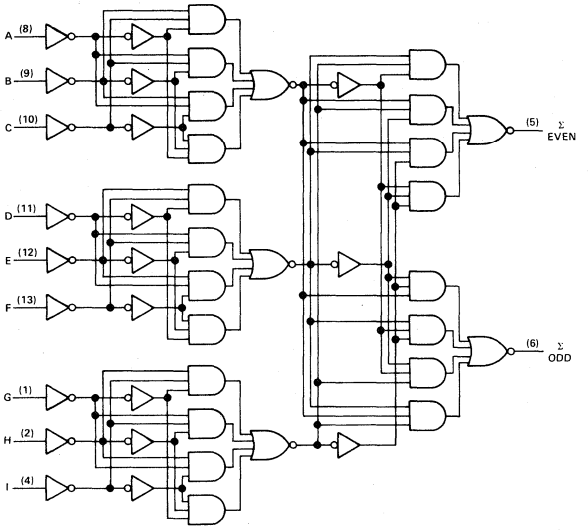
EQUIVALENT OF EACH INPUT



TYPICAL OF BOTH OUTPUTS



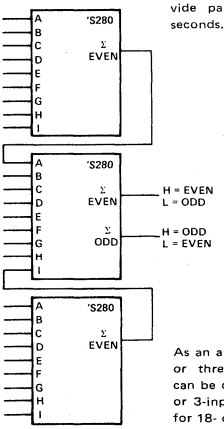
functional block diagram



TYPICAL APPLICATION DATA

25-LINE PARITY/GENERATOR CHECKER

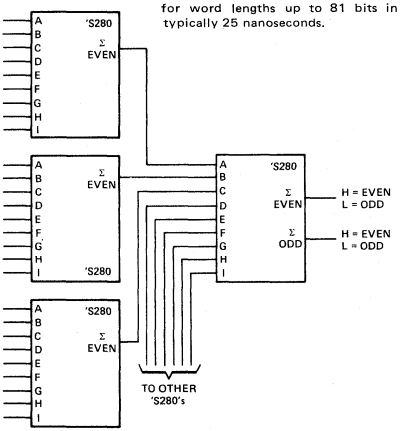
Three 'S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 nanoseconds.



As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input ('S86) or 3-input ('S135) exclusive-OR gate for 18- or 27-line parity applications.

81-LINE PARITY/GENERATOR CHECKER

Longer word lengths can be implemented by cascading 'S280's. As shown here, parity can be generated for word lengths up to 81 bits in typically 25 nanoseconds.



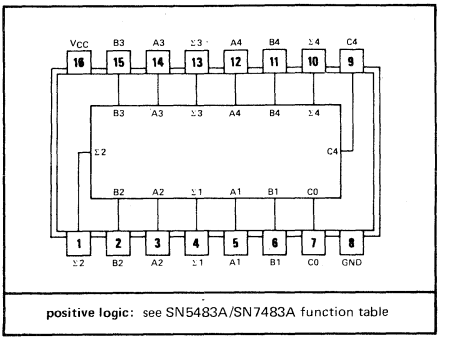
TEXAS INSTRUMENTS

TYPES SN54283, SN74283
4-BIT BINARY FULL ADDERS WITH FAST CARRY

BULLETIN NO. DL-S 7211832, DECEMBER 1972

- Full-Carry Look-Ahead across the Four Bits
- Typical Add or Subtract Times:
  23 ns (Two 8-bit Words)
  43 ns (Two 16-Bit Words)
- Systems Achieve Partial Look-Ahead Performance with the Economy of Ripple Carry
- Supply Voltage and Ground on Corner Pins to Simplify P-C Board Layout

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see SN5483A/SN7483A function table

description

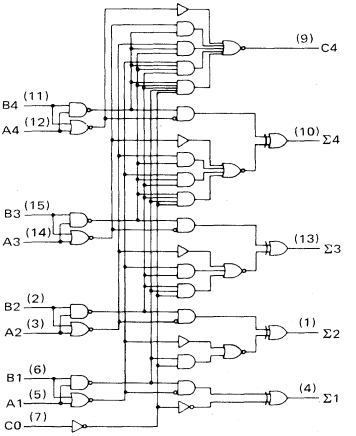
The SN54283 and SN74283 adders are electrically and functionally identical to the SN5483A and SN7483A, respectively. Only the arrangement of the terminals has been changed in the SN54283 and SN74283.

These improved 4-bit full adders/subtractors feature full look-ahead across four bits to generate the carry term in typically 10 nanoseconds. This capability provides the system designer with parital look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

These full adders are designed so that levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Power dissipation is typically 310 mW. Delay times through the package are 10 ns and 16 ns respectively from carry-in to carry-out and data-in to data-out. The SN54283 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74283 is characterized for 0°C to 70°C operation.

functional block diagram



function table and schematics of inputs and outputs

Same as SN5483A/SN7483A, see pages 198 and 199.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54283	−55°C to 125°C
SN74283	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the following pairs: A1 and B1, A2 and B2, A3 and B3, A4 and B4.

recommended operating conditions

		SN54283			SN74283			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Any output except C4			−800			−800	μA
	Output C4			−400			−400	
Low-level output current, I_{OL}	Any output except C4			16			16	mA
	Output C4			8			8	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54283			SN74283			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = MAX		2.4	3.6		2.4	3.6		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	Any output except C4	V_{CC} = MAX		−20		−55	−18		−55	mA
		Output C4			−20		−70	−18		−70	
I_{CC}	Supply current		V_{CC} = MAX, Outputs open	All B low, other inputs at 4.5 V		56			56		mA
				All inputs at 4.5 V		66	99		66	110	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Only one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Any Σ	C_L = 15 pF, R_L = 400 Ω, See Note 3		14	21	ns
t_{PHL}					12	21	
t_{PLH}	A_i or B_i	Σ_i			16	24	ns
t_{PHL}					16	24	
t_{PLH}	C0	C4	C_L = 15 pF, R_L = 780 Ω, See Note 3		9	14	ns
t_{PHL}					11	16	
t_{PLH}	A_i or B_i	C4			9	14	ns
t_{PHL}					11	16	

¶t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN54284, SN54285, SN74284, SN74285
4-BIT-BY-4-BIT PARALLEL BINARY MULTIPLIERS

BULLETIN NO. DL-S 7211741, MAY 1972—REVISED DECEMBER 1972

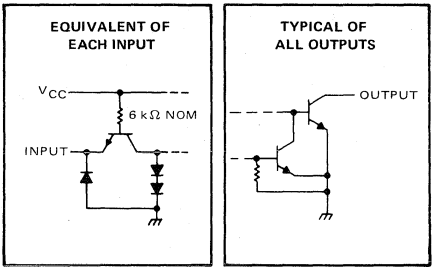
- Fast Multiplication of Two Binary Numbers 8-Bit Product in 40 ns Typical
- Expandable for N-Bit-by-n-Bit Applications: 16-Bit Product in 70 ns Typical 32-Bit Product in 103 ns Typical
- Fully Compatible with Most DTL and TTL Circuits
- Diode-Clamped Inputs Simplify System Design

description

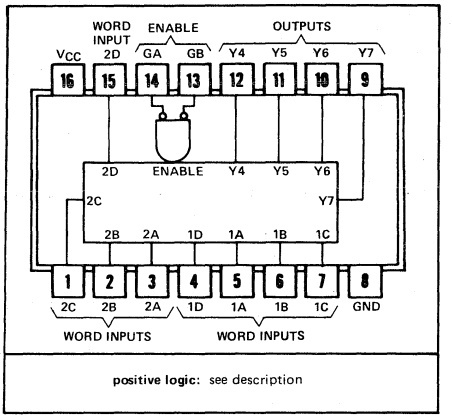
These high-speed TTL circuits are designed to be used in high-performance parallel multiplication applications. When connected as shown in Figure A, these circuits perform the positive-logic multiplication of two 4-bit binary words. The eight-bit binary product is generated with typically only 40 nanoseconds delay.

This basic four-by-four multiplier can be utilized as a fundamental building block for implementing larger multipliers. For example, the four-by-four building blocks can be connected as shown in Figure B to generate submultiple partial products. These results can then be summed in a Wallace tree, and, as illustrated, will produce a 16-bit product for the two eight-bit words typically in 70 nanoseconds. SN54H183/SN74H183 carry-save adders and SN54S181/SN74S181 arithmetic logic units with the SN54S182/SN74S182 look-ahead generator are used to achieve this high performance. The scheme is expandable for implementing N X M bit multipliers.

schematics of inputs and outputs

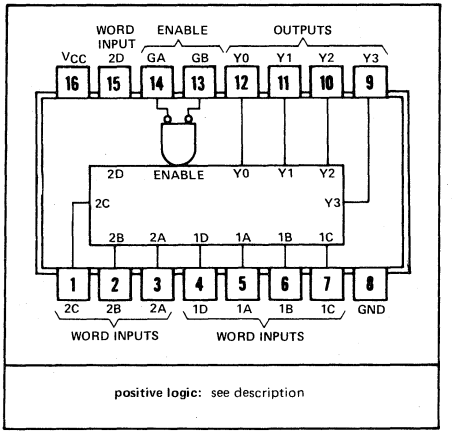


SN54284, SN74284
J OR N DUAL-IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



positive logic: see description

SN54285, SN74285
J OR N DUAL-IN-LINE OR W FLAT PACKAGE
(TOP VIEW)



positive logic: see description

The SN54284 and SN54285 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74284 and SN74285 are characterized for operation from 0°C to 70°C.

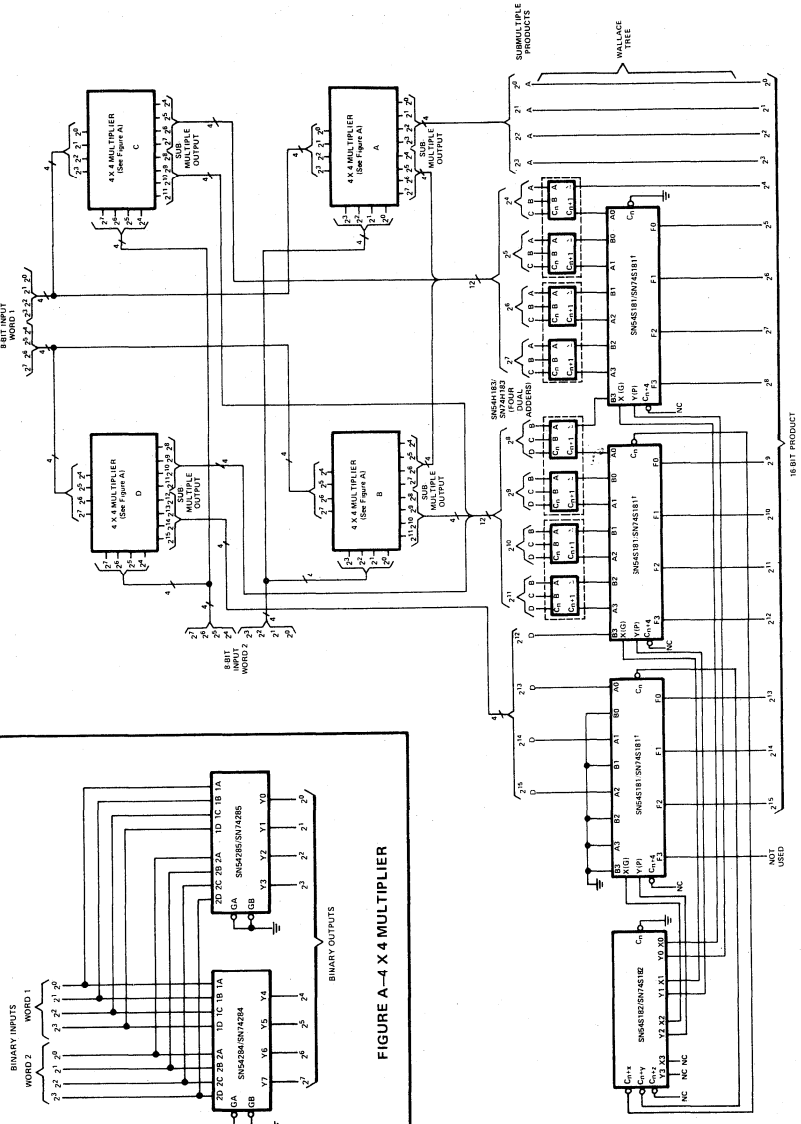


FIGURE B–8 X 8 MULTIPLIER

†Other terminals of the three SN54S181/SN74S181 ALU's are connected as follows: S3 = H, S2 = L, S1 = L, S0 = H, M = L. Output A = B is not used for this application.

FIGURE A–4 X 4 MULTIPLIER

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54284 SN54285			SN74284 SN74285			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
			I_{OL} = 16 mA			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	mA
I_{CC}	Supply current	V_{CC} = MAX, T_A = 125°C, See Note 2	SN54284, SN54285 N package only			99	mA
		V_{CC} = MAX, See Note 2	SN54284, SN54285		92	110	
			SN74284, SN74285		92	130	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: With outputs open and both enable inputs grounded, I_{CC} is measured first by selecting an output product which contains three or more high-level bits, then by selecting an output product which contains four low-level bits.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable	C_L = 30 pF to GND, R_{L1} = 300 Ω to V_{CC}, R_{L2} = 600 Ω to GND, See Note 3		20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable			20	30	
t_{PLH}	Propagation delay time, low-to-high-level output from word inputs			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output from word inputs			40	60	

NOTE 3: Load circuit is as described above; waveforms are shown on page 148.

TYPES SN54290, SN54293, SN74290, SN74293
DECADE AND 4-BIT BINARY COUNTERS

BULLETIN NO. DL-S 7211833, DECEMBER 1972

'290 . . . DECADE COUNTERS
'293 . . . 4-BIT BINARY COUNTERS

- GND and V_{CC} on Corner Pins (Pins 7 and 14 Respectively)

description

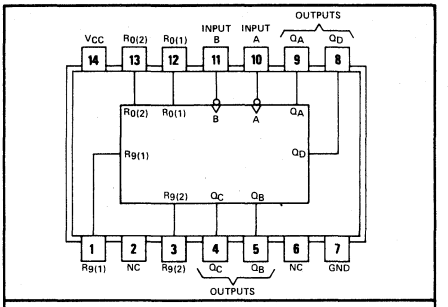
The SN54290/SN74290 and the SN54293/SN74293 counters are electrically and functionally identical to the SN5490A/SN7490A and the SN5493A/SN7493A, respectively. Only the arrangement of the terminals has been changed for the '290 and '293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the '290 and divide-by-eight for the '293.

Both of these counters have a gated zero reset and the '290 also has gated set-to-nine inputs for use in BCD nine's complement applications.

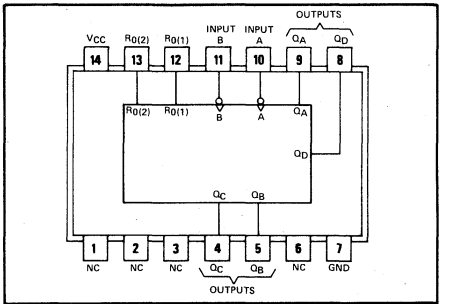
To use the maximum count length (decade or four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the '290 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

'290
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



positive logic: see '90A function tables

'293
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



positive logic: see '93A function table

NC—No internal connection

'290
BCD COUNT SEQUENCE
(See Note A)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

'290
BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

'290
RESET/COUNT FUNCTION TABLE

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

'293
RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

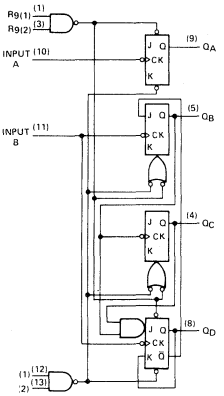
'293
COUNT SEQUENCE
(See Note C)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

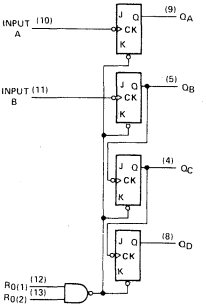
NOTES: A. Output Q_A is connected to input B for BCD count.
B. Output Q_D is connected to input A for bi-quinary count.
C. Output Q_A is connected to input B.
D. H = high level, L = low level, X = irrelevant

functional block diagram and schematics of inputs and outputs

'290

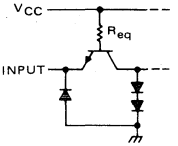


'293



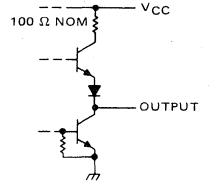
. . . dynamic input activated by a transition from a high level to a low level.

EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
A	2.5 kΩ
B ('290)	1.25 kΩ
B ('293)	2.5 kΩ
All resets	6 kΩ

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN54' Circuits . . . . . −55°C to 125°C
SN74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the two R_0 inputs, and for the '290 circuit, it also applies between the two R_9 inputs.

recommended operating conditions

		SN54'			SN74'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Count frequency, f_{count}	A input	0		32	0		32	MHz
	B input	0		16	0		16	
Pulse width, t_w	A input	15			15			ns
	B input	30			30			
	Reset inputs	15			15			
Reset inactive-state setup, t_{setup}		25			25			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		'290			'293			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶			0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	Any reset	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		A input					80			80	
		B input					120			80	
I_{IL}	High-level input current	Any reset	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		A input					−3.2			−3.2	
		B input					−4.8			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54'	−20		−57	−20		−57	mA
				SN74'	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			29	42		26	39	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
¶Outputs are tested at I_{OL} = 16 mA plus the limit value for I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.
NOTE 3: I_{CC} is measured with all outputs open, both R_0 inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

3

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'290			'293			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}	A	Q_A	C_L = 15 pF, R_L = 400 Ω, See Note 4	32	42		32	42		MHz
	B	Q_B		16			16			
t_{PLH}	A	Q_A			10	16		10	16	ns
t_{PHL}					12	18		12	18	
t_{PLH}	A	Q_D			32	48		46	70	ns
t_{PHL}					34	50		46	70	
t_{PLH}	B	Q_B			10	16		10	16	ns
t_{PHL}					14	21		14	21	
t_{PLH}	B	Q_C			21	32		21	32	ns
t_{PHL}					23	35		23	35	
t_{PLH}	B	Q_D			21	32		34	51	ns
t_{PHL}					23	35		34	51	
t_{PHL}	Set-to-0	Any			26	40		26	40	ns
t_{PLH}	Set-to-9	Q_A, Q_D			20	30				ns
t_{PHL}		Q_B, Q_C			26	24				

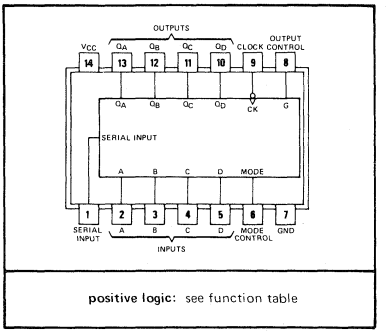
◇f_{max} ≡ maximum count frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are the same as those shown for the '90A and '93A, page 229.

TYPES SN54LS295, SN74LS295
4-BIT RIGHT-SHIFT LEFT-SHIFT REGISTERS
WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 7211780, SEPTEMBER 1972—REVISED DECEMBER 1972

- Three-State Versions of SN54LS95A/SN74LS95A Parallel-In, Parallel-Out Registers
- Schottky-Diode-Clamped Transistors
- Low Power Dissipation . . . 60 mW Typical (Enabled)
- Applications
  - N-Bit Serial-To-Parallel Converter
  - N-Bit Parallel-To-Serial Converter
  - N-Bit Storage Register

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, mode, and output control inputs. The registers have three modes of operation:

Parallel (Broadside) Load
Shift Right (the direction Q_A toward Q_D)
Shift Left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

Shift right is accomplished when the mode control is low; shift left is accomplished when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D.

When the output control is high, the normal logic levels of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a low logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected.

The SN54LS295 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS295 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS							OUTPUTS			
MODE CONTROL	CLOCK	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
			A	B	C	D				
H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	a	b	c	d	a	b	c	d
H	↓	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}

When the output control is low, the outputs are disabled to the high-impedance state; however, sequential operation of the registers is not affected.

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level.
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54LS295 . . . . . −55°C to 125°C
SN74LS295 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54LS295			SN74LS295			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$	25			25			ns
Setup time, high-level or low-level data, t_{setup}	20			20			ns
Hold time, high-level or low-level data, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54LS295			SN74LS295			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}max, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4				V
				I_{OL} = 8 mA					0.35	0.5	
$I_{O(off)}$	Off-state (high-impedance state) output current		V_{CC} = MAX, V_{IL} = V_{IL}max	V_O = 2.7 V			20			20	μA
				V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				0.1			0.1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	Clock input	V_{CC} = MAX, V_I = 0.4 V				−0.44			−0.44	mA
		Other inputs					−0.36			−0.36	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−6		−40	−5		−42	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition A		12	20		12	20	mA
				Condition B		13	21		13	21	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

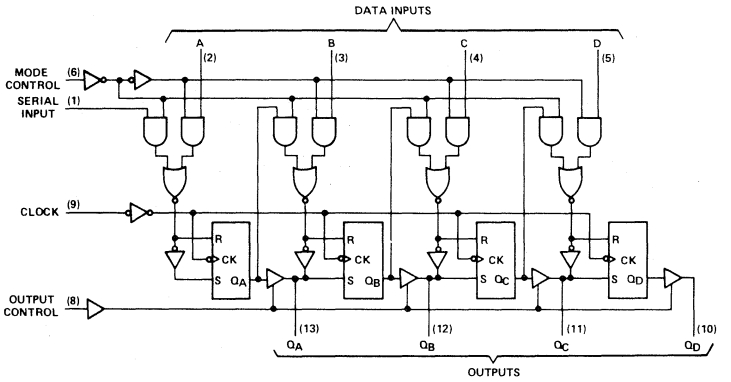
NOTE 2: I_{CC} is measured with the outputs open, the serial input and mode control at 4.5 V, and the data inputs grounded under the following conditions:
A. Output control at 4.5 V and a momentary 3 V, then ground, applied to clock input.
B. Output control and clock input grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, R_L = 2 kΩ

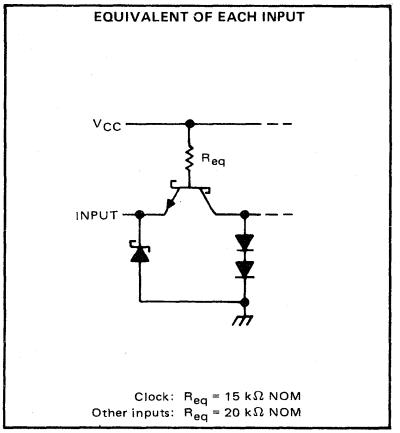
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, See Note 3	20	28		MHz
t_{PLH}	Propagation delay time, low-to-high-level output			40	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			47	70	ns
t_{ZH}	Output enable time to high level			15	25	ns
t_{ZL}	Output enable time to low level			21	30	ns
t_{HZ}	Output disable time from high level	C_L = 5 pF, See Note 3		39	60	ns
t_{LZ}	Output disable time from low level			32	50	ns

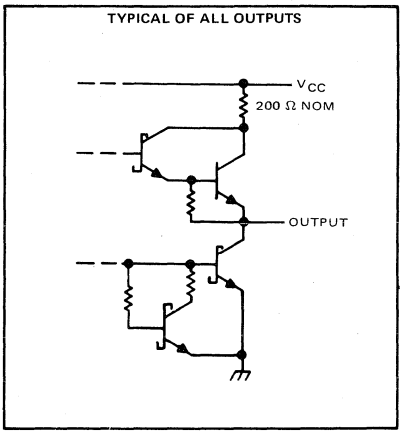
NOTE 3: Load circuit and voltage waveforms are shown on page 149.

functional block diagram



schematics of inputs and outputs





TYPES SN54298, SN74298
QUADRUPLE 2-INPUT MULTIPLEXERS WITH STORAGE

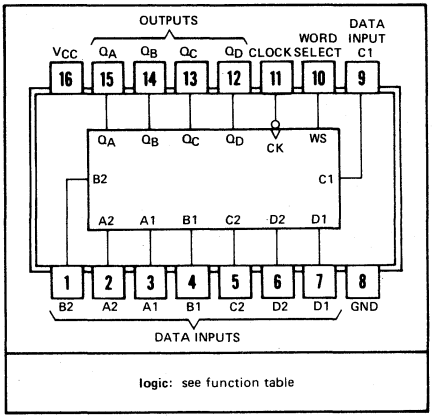
BULLETIN NO. DL-S 7211747, MAY 1972 – REVISED DECEMBER 1972

- **Selects One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock**
- **Applications:**
  Dual Source for Operands and Constants in Arithmetic Processor; Can Release Processor Register Files for Acquiring New Data

  Implement Separate Registers Capable of Parallel Exchange of Contents Yet Retain External Load Capability

  Universal Type Register for Implementing Various Shift Patterns; Even Has Compound Left-Right Capabilities

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)



logic: see function table

description

These monolithic quadruple two-input multiplexers with storage provide essentially the equivalent functional capabilities of two separate MSI functions (SN54157/SN74157 and SN54175/SN74175) in a single 16-pin package.

When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

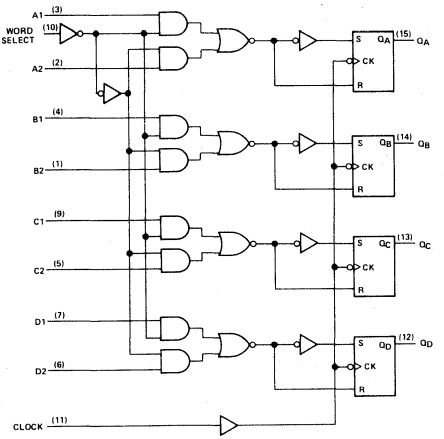
Typical power dissipation is 195 milliwatts. The SN54298 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74298 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

functional block diagram



. . . Dynamic input activated by a transit on from a high level to a low level

3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN54298 Circuits . . . . . −55°C to 125°C
SN74298 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54298			SN74298			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Width of clock pulse, high or low level, t_w		20			20			ns
Setup time, t_{setup}	Data	15			15			ns
	Word select	25			25			
Hold time, t_{hold}	Data	5			5			ns
	Word select	0			0			
Operating free-air temperature, T_A		−55		125	0		70	°C

3

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54298	−20		−57	mA
			SN74298	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	65	mA

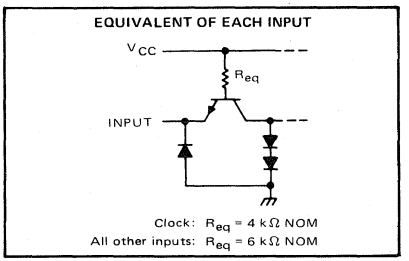
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With all outputs open and all inputs except clock low, I_{CC} is measured after applying a momentary 4.5 V, followed by ground, to the clock input.

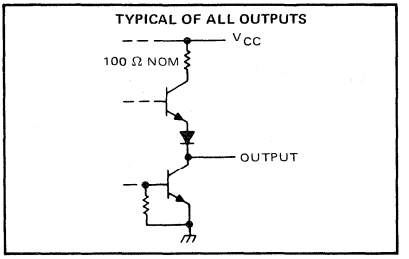
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω, See Note 3		18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output			21	32	

NOTE 3: Load circuit and waveforms are shown on page 148.

schematics of inputs and outputs

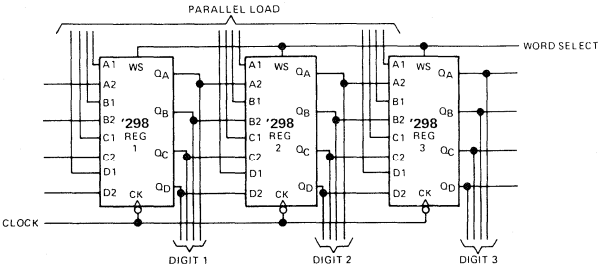




TYPICAL APPLICATION DATA

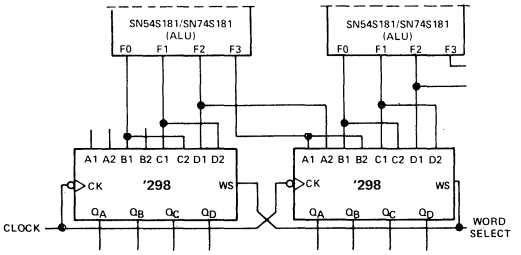
This versatile multiplexer/register can be connected to operate as a shift register which can shift N-places in a single clock pulse.

The following figure illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.



When the word-select input is high and the registers are clocked, the contents of register 1 is transferred (shifted) to register 2 and etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered in the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

Another function that can be implemented with the '298 is a register that can be designed specifically for supporting multiplier or division operations. The example below is a one-place/two-place shift register.



When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.

3

Series 29000
SSI Circuits

4

SERIES 29000
TRANSISTOR-TRANSISTOR LOGIC

BULLETIN NO. DL-S 7211869, DECEMBER 1972

description

Series 29000 devices are designed to be used in existing systems as replacments for 9000-type circuits. Series 29000 circuits offer several significant advantages over 9000 type circuits, some of which are:

- Output short-circuit current specified to guarantee the high-level impedance.
- Power dissipation of Series 29000 circuits is in most cases lower than that for the equivalent 9000 type.

Series 29000 circuits are characterized for operation over the industrial temperature range of 0°C to 75°C.

For new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Included are ten series of compatible TTL circuits offering a choice of specific performance ranges. All 54/74 family circuits are entirely compatible and are designed to serve any application from industrial numerical controllers or high-speed computers to sophisticated high-reliability aerospace and defense systems. Series 54/74 pin-for-pin equivalents are available for the following Series 29000 SSI types:

SERIES 29000	EQUIVALENT SERIES 74
SN29002	SN7400J, N
SN29003	SN7410J, N
SN29004	SN7420J, N
SN29005	SN7450J, N
SN29009	SN7440J, N
SN29012	SN7403J, N
SN29016	SN7404J, N
SN29024	SN74109J, N

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

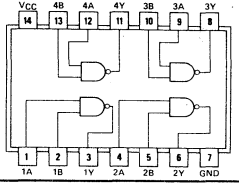
Supply voltage, V_{CC} (see Notes 1 and 2)	8 V
Input voltage	5.5 V
Interemitter voltage (see Note 3)	5.5 V
Steady-state input current range	−30 mA to 5 mA
High-level output voltage	V_{CC}
Low-level output current: SN29009	100 mA
Other circuit types	50 mA
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. The maximum V_{CC} value of 8 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a high output is approximately two forward-biased-diode drops below the V_{CC} voltage, so the primary limit on V_{CC} is that the voltage at any input may not go above 5.5 volts. This effectively limits the system V_{CC} to approximately 7 volts.
3. This is the voltage between two emitters of a multiple-emitter transistor. For these SSI circuits, this rating applies between inputs that go directly into the same AND or NAND gate in the functional block diagram.

SERIES 29000 GATES AND INVERTERS

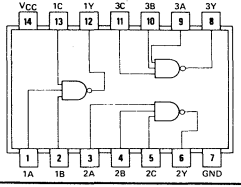
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

SN29002
QUADRUPLE 2-INPUT NAND GATE
SN29012
QUADRUPLE 2-INPUT NAND GATE
WITH OPEN-COLLECTOR OUTPUTS



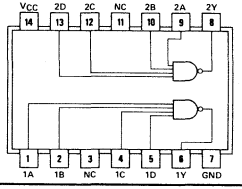
positive logic: $Y = \overline{AB}$

SN29003
TRIPLE 3-INPUT NAND GATE



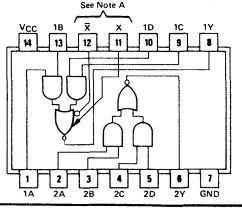
positive logic: $Y = \overline{ABC}$

SN29004
DUAL 4-INPUT NAND GATE
SN29009
DUAL 4-INPUT NAND BUFFER



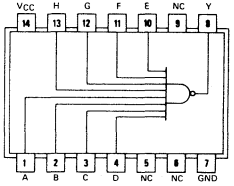
positive logic: $Y = \overline{ABCD}$

SN29005
EXPANDABLE DUAL 2-WIDE
2-INPUT AND-OR-INVERT GATE



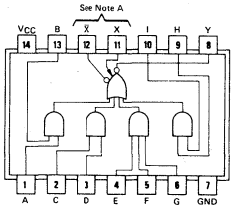
positive logic: $Y = \overline{AB+CD+\bar{X}}$
X = Output of expander

SN29007
8-INPUT NAND GATE



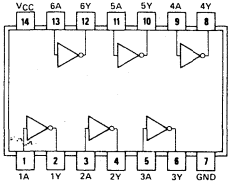
positive logic: $Y = \overline{ABCDEFGH}$

SN29008
EXPANDABLE 4-WIDE 2-2-3-2-INPUT
AND-OR-INVERT GATE



positive logic: $Y = \overline{AB+CD+EFG+HI+\bar{X}}$
X = Output of expander

SN29016
HEX INVERTER



positive logic: $Y = \overline{A}$

NOTE A: X is the emitter terminal and $\bar{X}$ is the collector terminal of the expander circuit (e.g. SN5460/SN7460).

NC—No internal connection

recommended operating conditions

		SN29002, SN29003, SN29004, SN29005, SN29007, SN29008, SN29016			SN29009			SN29012			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
High-level output voltage, V_{OH}										5.5	V
Normalized fan-out from each output, N	High logic level			20			60				
	Low logic level			10			30			10	
Operating free-air temperature, T_A		0		75	0		75	0		75	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS			SN29002 SN29003 SN29004 SN29007 SN29016		SN29005 EXPANDABLE GATE		SN29005 NON-EXPANDABLE GATE		SN29008		SN29009		SN29012		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage			0°C	1.9		1.9		1.9		1.9		1.9		1.9		V
				25°C	1.8		1.8		1.8		1.8		1.8		1.8		
				75°C	1.6		1.6		1.6		1.6		1.6		1.6		
V_{IL}	Low-level input voltage			0°C to 75°C		0.85		0.85		0.85		0.85		0.85		0.85	V
V_I	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −12 mA	0°C to 75°C		−1.5		−1.5		−1.5		−1.5		−1.5		−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.85 V	I_{OH} = −1.2 mA	0°C to 75°C	2.4		2.4		2.4		2.4						V
			I_{OH} = −3.6 mA										2.4				
V_{OL}	Low-level output voltage	V_{CC} = 5.25 V, V_{IH} = V_{IH} min	I_{OL} = 16 mA	0°C to 75°C		0.45		0.45		0.45		0.45				0.45	V
			I_{OL} = 48 mA										0.45				
		V_{CC} = 4.75 V, V_{IH} = V_{IH} min	I_{OL} = 14.1 mA			0.45		0.45		0.45		0.45				0.45	
			I_{OL} = 42.3 mA										0.45				
I_{OH}	High-level output current	V_{CC} = 4.75 V, V_{OH} = 5.5 V	V_{IL} = 0.85 V,	0°C to 75°C												250	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V, Other inputs at ground	V_I = 4.5 V,	0°C to 75°C		60		90		60		90		120		60	μA
I_{IL}	Low-level input current	V_I = 0.45 V, Other inputs at 5.25 V	V_{CC} = 5.25 V	0°C to 75°C		−1.6		−2.4		−1.6		−1.6		−1.6		−1.6	mA
			V_{CC} = 4.75 V			−1.41		−2.12		−1.41		−1.41		−1.41		−1.41	
I_{OS}	Short-circuit output current†	V_{CC} = 5.25 V		0°C to 75°C	−18	−55	−20	−70	−20	−70	−18	−55	−20	−70			mA
I_{CCH}	Supply current, all outputs high (average per gate)	V_{CC} = 5 V, See Figure 7 on page 145		0°C to 75°C		1.7		5.1		3.4		8		3.4		8	mA
I_{CCL}	Supply current, all outputs low (average per gate)	V_{CC} = 5 V, See Figure 7 on page 145		0°C to 75°C		5.5		13.6		7.7		9.5		13.5		9.5	mA

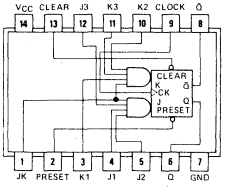
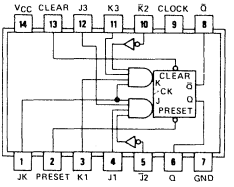
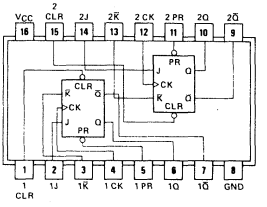
switching characteristics, V_{CC} = 5 V, T_A = 25°C

t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω,‡ See Note 4	3	13	15	12	15	17	3	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output		3	15	12	14	12	13	3	15	

†Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
‡For testing t_{PLH} of SN29012, R_L = 4 kΩ.
NOTE 4: Expander inputs of SN29005 and SN29008 are open. Load circuit, input characteristics, and voltage waveforms are the same as those shown for Series 54/74, page 148.

SERIES 29000 FLIP-FLOPS

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)

SN29000 (FORMERLY SN74104) GATED J-K MASTER-SLAVE FLIP-FLOP	SN29001 (FORMERLY SN74105) GATED J-K ($\overline{J}$-$\overline{K}$) MASTER-SLAVE FLIP-FLOP	SN29024 DUAL $\overline{J}$-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOP
		
positive logic: see function table	**positive logic:** see function table	**positive logic:** see function table

SN29000, SN29001
FUNCTION TABLE

INPUTS						OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	JK	Q	$\overline{Q}$
L	H	X	X	X	X	H	L
H	L	X	X	X	X	L	H
L	L	X	X	X	X	H*	H*
H	H	⊓	X	X	L	Q_0	$\overline{Q}_0$
H	H	⊓	L	L	X	Q_0	$\overline{Q}_0$
H	H	⊓	H	L	H	H	L
H	H	⊓	L	H	H	L	H
H	H	⊓	H	H	H	TOGGLE	

SN29024
FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	Q_0

SN29000: J = J1•J2•J3; K = K1•K2•K3
SN29001: J = J1•$\overline{J2}$•J3; K = K1•$\overline{K2}$•K3
H = high level (steady state), L = low level (steady state), X = irrelevant
⊓ = low-level pulse; other inputs should be held constant while clock is low.
↑ = transition from low to high level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
*This configuration is nonstable. That is, it will not persist when preset and clear inputs return to their inactive (high) level.

recommended operating conditions

		SN29000			SN29001			SN29024			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20			20	
	Low logic level			10			10			10	
Clock frequency, f_{clock}		0		15	0		30	0		25	MHz
Width of clock pulse, t_w	High level	30			18			20			ns
	Low level	35			15			20			
Width of preset or clear pulse, t_w		25			25			20			ns
Input setup time, t_{setup}	J, K, or JK	35			15						ns
	J or $\overline{K}$							10			
	$\overline{J}$ or $\overline{K}$				17						
Input hold time, t_{hold}								6			ns
Input release time, $t_{release}$	J, K, or JK			10			1				ns
	$\overline{J}$ or $\overline{K}$						4				
Operating free-air temperature, T_A		0		75	0		75	0		75	°C

electrical characteristics at specified free-air temperature

PARAMETER		TEST CONDITIONS			SN29000 MIN	SN29000 MAX	SN29001 MIN	SN29001 MAX	SN29024 MIN	SN29024 MAX	UNIT
V_{IH}	High-level input voltage			0°C	1.9		1.9		1.9		V
				25°C	1.8		1.8		1.8		
				75°C	1.6		1.6		1.6		
V_{IL}	Low-level input voltage			0°C to 75°C		0.85		0.85		0.85	V
V_I	Input clamp voltage	V_{CC} = 4.75 V, I_I = −12 mA		0°C to 75°C		−1.5		−1.5		−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, V_{IH} = V_{IH} min, V_{IL} = 0.85 V, I_{OH} = −1.2 mA		0°C to 75°C	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, V_{IH} = V_{IH} min, V_{IL} = 0.85 V, I_{OL} = 14.1 mA		0°C to 75°C		0.45		0.45		0.45	V
		V_{CC} = 5.25 V, V_{IH} = V_{IH} min, V_{IL} = 0.85 V, I_{OL} = 16 mA				0.45		0.45		0.45	
I_{IH}	High-level input current	J, K, $\overline{J}$ or $\overline{K}$	V_{CC} = 5.25 V, V_I = 4.5 V, Other inputs at ground	25°C and 75°C		60		60		60	μA
		JK				120		120			
		Clock				60		60		120	
		Preset				160		160		120	
		Clear				160		160		240	
I_{IL}	Low-level input current	J, K, $\overline{J}$, or $\overline{K}$,	V_I = 0.45 V, Other inputs at 5.25 V	V_{CC} = 5.25 V, 0°C to 75°C		−1.6		−1.6		−1.6	mA
		JK				−3.2		−3.2			
		Clock				−1.6		−1.6		−3.2	
		Preset				−4.32		−4.32		−3.2	
		Clear				−4.32		−4.32		−6.4†	
		J, K, $\overline{J}$, or $\overline{K}$		V_{CC} = 4.75 V, 0°C to 75°C		−1.41		−1.41		−1.24	mA
		JK				-2.82		−2.82			
		Clock				−1.41		−1.41		−2.82	
		Preset				−3.78		−3.78		−2.82	
		Clear				−3.78		−3.78		−4.96‡	
I_{OS}	Short-circuit output current§	V_{CC} = 5.25 V		0°C to 75°C	−30	−100	−30	−100	−30	−100	mA
I_{CC}	Supply current	V_{CC} = 5 V, See Note 5		0°C to 75°C		28		33		28	mA

†This current will be a maximum of −4.8 mA if J or $\overline{K}$ input is grounded.
‡This current will be a maximum of −3.72 mA if J or $\overline{K}$ input is grounded.
§ Not more than than one output should be shorted at a time and duration of the short circuit should not exceed one second.
NOTE 5: I_{CC} is measured with all outputs open, first with preset at 4.5 V and all other inputs grounded, then with clear at 4.5 V and all other inputs grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN29000 MIN	SN29000 TYP	SN29000 MAX	SN29001 MIN	SN29001 TYP	SN29001 MAX	SN29024 MIN	SN29024 TYP	SN29024 MAX	UNIT
f_{max}				15	20		30	50		25	32		MHz
t_{PLH}	Clock	Q or $\overline{Q}$	C_L = 15 pF, R_L = 400 Ω, See Note 6		12	20		12	30	4	10	16	ns
t_{PHL}					20	30		20	30	9	18	28	
t_{PLH}	Preset	Q			12	20		12	20		10	15	ns
t_{PHL}		$\overline{Q}$				35			35		23	35	
t_{PLH}	Clear	$\overline{Q}$			12	20		12	20		10	15	ns
t_{PHL}		Q				35			35		17	25	

¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
NOTE 6: Load circuit, input characteristics, and voltage waveforms are the same as those shown for Series 54/74, page 148.

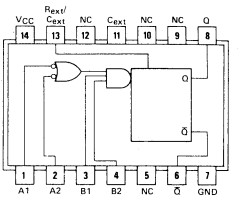
TYPE SN29601
MONOSTABLE MULTIVIBRATOR

- Direct Replacement for Fairchild 9601C
- For New Designs, SN74122 Is Recommended

FUNCTION TABLE
(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

J OR N DUAL-IN-LINE
PACKAGE (TOP VIEW)
(See Notes B and C)



positive logic: see function table

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = No internal connection.
C. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

4

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Input data setup time, t_{setup}		40◇			ns
Input data hold time, t_{hold}		40◇			ns
Width of clear pulse, $t_{w(clear)}$		40◇			ns
External timing resistance		5		50	kΩ
External capacitance		No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50	pF
Operating free-air temperature, T_A		0		75	°C

◇These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 7	I_{OH} = −800 μA,	2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 7	I_{OL} = 16 mA,		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		clear input					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	See Note 7	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX,	See Notes 8 and 9		23	28	mA

†For conditions shown as MIN or MAX, use the value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 7. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
8. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, C_{ext} = 0.02 μF, R_{ext} = 25 kΩ, R_{int} and all outputs open.
9. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, C_{ext} = 0.02 μF, R_{ext} = 25 kΩ, R_{int} and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input	C_{ext} = 0, C_L = 15 pF, See Note 10	R_{ext} = 5 kΩ, R_L = 400 Ω,		22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input				30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 400 Ω	3.08	3.42	3.76	μs

NOTE 10: Load circuit, input characteristics, and voltage waveforms are the same as those shown for Series 54/74, page 148.

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4

Series 29300/39300
MSI Circuits

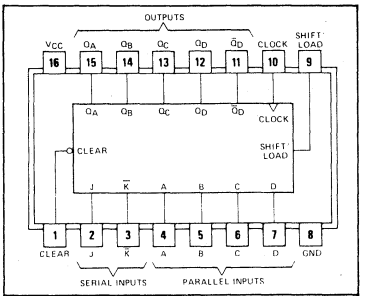
5

TYPES SN29300, SN39300
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

BULLETIN NO. DL-S 7211817, DECEMBER 1972

- Direct Replacement for Fairchild 9300
- 30% Lower Power Consumption
- Typical Power Dissipation . . . 195 mW
- Typical Maximum Shift Frequency . . . 39 MHz
- For New Designs, SN74195 or SN54195 is Recommended
- Synchronous Parallel Load
- Positive Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Fully Buffered Inputs

SN29300 . . . J OR N DUAL-IN-LINE PACKAGE
SN39300 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see description

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (Broadside) Load
Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

The SN29300 and SN39300 shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 29/39 load. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The SN29300 is characterized for operation over the temperature range of 0°C to 75°C, and the SN29300 is characterized for operation over the full military temperature range of −55°C to 125°C.

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FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent ↑ transition of the clock

functional block diagram and schematics of inputs and outputs

Same as SN54195, SN75195. See pages 445 and 446.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature: SN29300 . . . . . 0°C to 75°C
SN39300 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN29300			SN39300			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup}	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$				10			10	ns
Serial and parallel data hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		39	63	mA

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, See Note 3	R_L = 400 Ω,	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear				19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			7	17	26	ns

NOTE 3: Load circuit, voltage waveforms, and input conditions are the same as those for the SN54195, SN74195. See page 450

TYPES SN29301, SN39301
4-LINE-TO-10-LINE BCD-TO-DECIMAL DECODERS (1-OF-10)

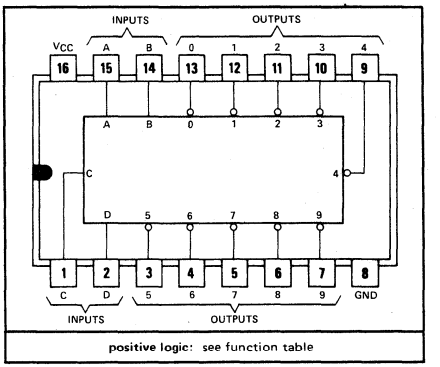
BULLETIN NO. DL-S 7211818, DECEMBER 1972

- Direct replacement for Fairchild 9301 and Signetics 8252
- For New Designs, SN7442A and SN5442A are Recommended
- Diode-Clamped Inputs
- All Outputs Are High for Invalid BCD Input Conditions

FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

SN29301 . . . J OR N DUAL-IN-LINE PACKAGE
SN39301 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

This monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

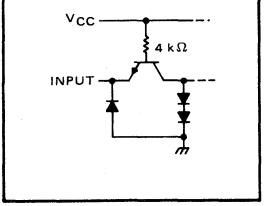
Both the SN29301 and SN39301 BCD-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 145 milliwatts. The diode-clamped, buffered inputs represent only one normalized Series 29/39 load. The SN29301 is characterized for operation over the temperature range of 0°C to 75°C, and the SN39301 is characterized for operation over the full military temperature range of −55°C to 125°C.

functional block diagram

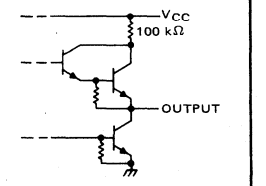
Same as SN5442A and SN7442A except for pin assignments. See page 168.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN29301 . . . . . 0°C to 75°C
SN39301 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN29301			SN39301			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−18		−70	mA
I_{CC}	Supply Current	V_{CC} = MAX, Outputs open, All inputs grounded		29	43	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level, any output from A, B, C, or D	C_L = 15 pF, R_L = 400 Ω, See Note 2		20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level, any output from A, B, C, or D			20	30	ns

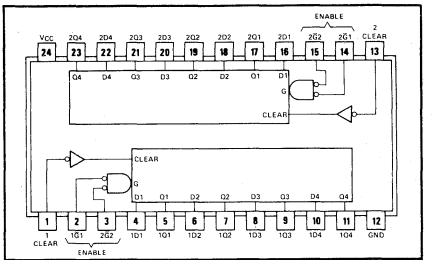
†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions for the applicable device type.
§Not more than one output should be shorted at a time.
NOTE 2: Load circuit and voltage waveforms are shown on page 148.

TYPES SN29308, SN39308
DUAL 4-BIT LATCHES WITH CLEAR

BULLETIN NO. DL-S 7211839, DECEMBER 1972

- Direct Replacement for Fairchild 9308
- For New Design, SN74116 or SN54116 Is Recommended
- Two Independent 4-Bit Latches in a Single Package
- Separate Clear Inputs Provide One-Step Clearing Operation
- Dual Gated Enable Inputs Simplify Cascading and Register Implementations

SN29308 . . . J OR N DUAL-IN-LINE PACKAGE
SN39308 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see function table

description

These monolithic TTL circuits utilize D-type bistables to implement two independent four-bit latches in a single package. Each four-bit latch has an independent asynchronous clear input and a gated two-input enable circuit. When both enable inputs are low, the output levels will follow the data input levels. When either or both of the enable inputs are taken high, the outputs remain at the last levels setup at the inputs prior to the low-to-high-level transition at the enable input(s). After this, the data inputs are locked out.

The clear input is overriding and when taken low will reset all four outputs low regardless of the levels of the enable inputs.

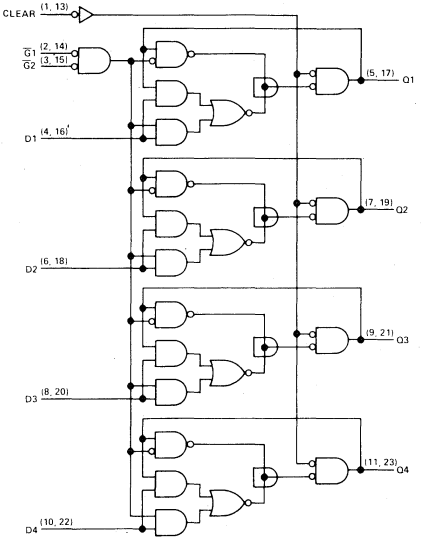
The SN39308 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN29308 is characterized for operation from 0°C to 75°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS				OUTPUT
CLEAR	ENABLE $\overline{G1}$	ENABLE $\overline{G2}$	DATA	Q
H	L	L	L	L
H	L	L	H	H
H	X	H	X	Q_0
H	H	X	X	Q_0
L	X	X	X	L

H = high level, L = low level, X = irrelevant
Q_0 = the level of Q before these input conditions were established.

functional block diagram (each 4-bit latch)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN29308 . . . . . 0°C to 75°C
SN39308 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN29308			SN39308			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Input pulse width, t_w	Enable	18			18			ns
	Clear	18			18			
Data setup time, t_{setup}	High logic level	8			8			ns
	Low logic level	14			14			
Clear inactive-state setup time, t_{setup}		8			8			ns
Data release time, high-level data, $t_{release}$				2			2	ns
Data hold time, low-level data, t_{hold}		8			8			
Operating free-air temperature, T_A		0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level input current		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Any D					60	
I_{IL}	Low-level input current	$\overline{G}1$, $\overline{G}2$, or clear	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Any D, initial peak					−2.4	
		Any D, steady-state					−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN29308	−18		−57	mA
				SN39308	−20		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 2	Condition A		60	100	mA
				Condition B		40	70	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: With outputs open, I_{CC} is measured for the following conditions:
A. All inputs grounded.
B. All $\overline{G}$ inputs are grounded and all other inputs are at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Enable	Any Q	C_L = 15 pF, R_L = 400 Ω, See Note 3		19	30	ns
t_{PHL}					15	22	
t_{PLH}	Data	Q			10	15	ns
t_{PHL}					12	18	
t_{PHL}	Clear	Any Q			15	22	ns

¶t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.
NOTE 3: See Figure 1 for SN54116/SN74116, page 263.

schematics of inputs and outputs

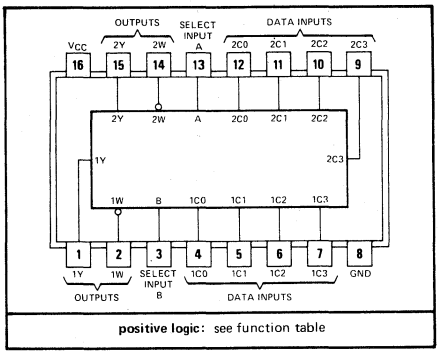
Same as SN54116/SN74116, see page 263.

TYPES SN29309, SN39309
DUAL 4-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7211860, DECEMBER 1972

- Direct Replacement for Fairchild 9309
- For New Designs, SN74153 and SN54153 Are Recommended
- Permits Multiplexing from N Lines to 1 Line
- Complementary Data Outputs
- Typical Average Propagation Delay Times:
  Data Input to Output . . .13 ns
  Select Input to Output . . . 19 ns

SN29309 . . . J OR N DUAL-IN-LINE PACKAGE
SN39309 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see function table

description

Each of these monolithic data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gates. Each of the 4-line multiplexers have complementary W and Y outputs; however, both sections share a common binary address input select circuit controlled by the A and B inputs.

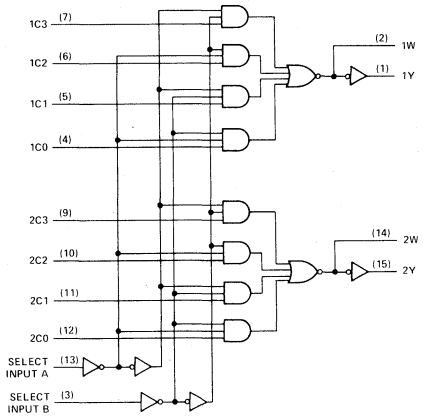
The SN29309 is characterized for operation over the temperature range of 0°C to 75°C, and the SN39309 is characterized for operation over the full military temperature range of −55°C to 125°C.

FUNCTION TABLE
4-LINE-TO-1-LINE
DATA SELECTOR/MULTIPLEXER

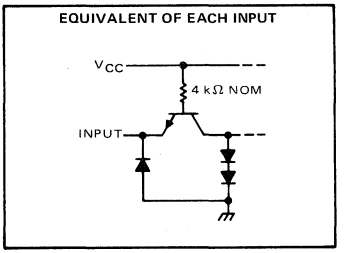
INPUTS						OUTPUTS	
SELECT		DATA					
B	A	C0	C1	C2	C3	Y	W
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	H	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

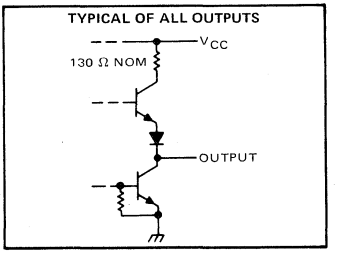
Select inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

functional block diagram



schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN29309 . . . . . 0°C to 75°C
SN39309 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN29309			SN39309			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−18		−55	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		19	35	mA

5

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with the outputs open and all inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Either Y	C_L = 15 pF, R_L = 400 Ω, See Note 3		22	36	ns
t_{PHL}					23	36	
t_{PLH}	A or B	Either W			17	24	ns
t_{PHL}					14	21	
t_{PLH}	C0, C1, C2, or C3	Y			16	24	ns
t_{PHL}					18	24	
t_{PLH}	C0, C1, C2, or C3	W			10	14	ns
t_{PHL}					8.5	13	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

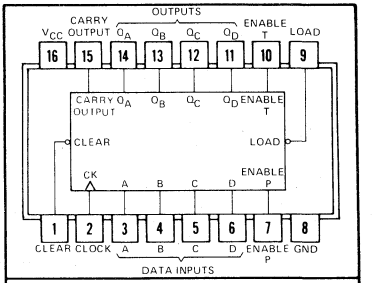
TYPES SN29310, SN29316, SN39310, SN39316
SYNCHRONOUS 4-BIT COUNTERS WITH DIRECT CLEAR

BULLETIN NO. DL-S 7211842, DECEMBER 1972

SN29310/SN39310 . . . DECADE COUNTERS
SN29316/SN39316 . . . 4-BIT BINARY COUNTERS

- Direct Replacement for Fairchild 9310 and 9316 in Most Applications
- For New Design, SN74160/SN54160 or SN74161/SN54161 Is Recommended
- Internal Look-Ahead for Fast Counting Schemes
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs
- Typical Maximum Clock Frequency . . . 32 MHz

SN29' . . . J OR N DUAL-IN-LINE PACKAGE
SN39' . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see description

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The SN29310 and SN39310 are decade counters and the SN29316 and SN39316 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform. The descriptions of SN54160/SN74160 and SN54161/SN74161 are applicable for the SN29310/SN39310 and SN29316/SN39316, respectively.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN29' Circuits . . . . . 0°C to 75°C
SN39' Circuits . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN29310 SN29316			SN39310 SN39316			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}				−800			−800	μA
Low-level output current, I_{OL}				16			16	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Note 3)	Data inputs A, B, C, D	15			15			ns
	Enable P	20			20			
	Load	25			25			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		0		75	−55		125	°C

NOTE 3: See Figure 2 for SN54160/SN74160 and SN54161/SN74161 on page 332.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN29310 SN29316			SN39310 SN39316			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−18		−57	−20		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 4		59	94		59	85	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 5		63	101		63	91	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 4. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
5. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Note 6	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock (count mode)			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock (count mode)			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T			10	14	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T			10	14	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear			20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock (load mode)			17	25	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock (load mode)			19	29	ns

NOTE 6: See Figures 1 and 2 for SN54160/SN74160 and SN54161/SN74161 on pages 331 and 332. Load circuit shown on page 148.

functional block diagram; clear, preset, count, and inhibit sequences; schematics of inputs and outputs; and typical application data

Same as SN54160/SN74160 and SN54161/SN74161, see pages 326, 327, 328, 330, and 333.

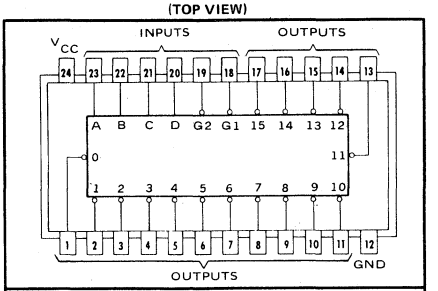
TYPES SN29311, SN39311
4-LINE-TO-16-LINE DECODERS/DEMULTIPLEXERS

BULLETIN NO. DL-S 7211844, DECEMBER 1972

FOR APPLICATIONS IN COMMUNICATIONS EQUIPMENT, COMPUTERS, AND ELECTRONIC INSTRUMENTATION

- Direct Replacement for Fairchild 9311
- For New Designs, SN74154 and SN54154 Are Recommended
- Decodes 4 Binary-Coded Inputs into One of 16 Mutually Exclusive Outputs
- Performs the Demultiplexing Function by Distributing Data from One Input Line to Any One of 16 Outputs
- Input Clamping Diodes Simplify System Design
- High Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits

SN29311 . . . J OR N DUAL-IN-LINE PACKAGE
SN39311 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)

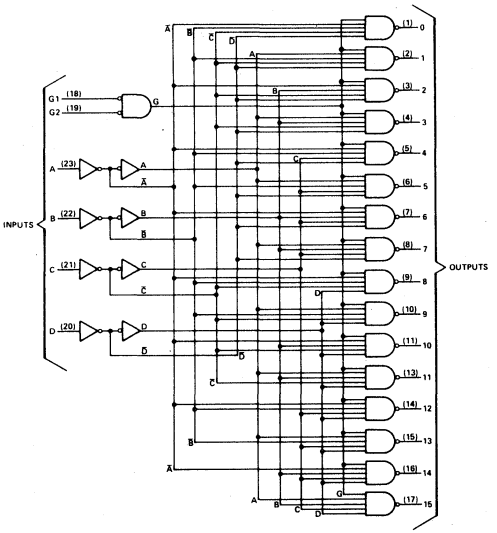


positive logic: see SN54154/SN74154 function table

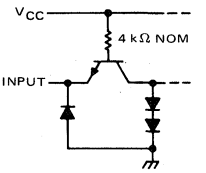
description

This monolithic, 4-line-to-16-line decoder utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

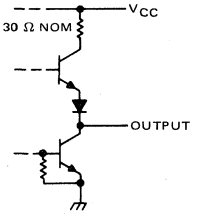
functional block diagram and schematics of inputs and outputs



EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN29311 . . . . . 0°C to 75°C
SN39311 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN29311			SN39311			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN29311			SN39311			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−18		−57	−20		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		34	56		34	49	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	C_L = 15 pF, R_L = 400 Ω, See Note 3		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic			22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input			20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input			18	27	ns

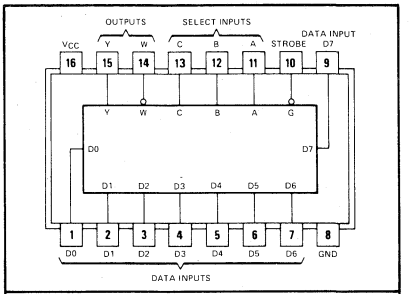
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN29312, SN39312
DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7211857, DECEMBER 1972

- Direct Replacement for Fairchild 9312
- For New Designs, SN74151A and SN54151A Are Recommended
- Selects One-of-Eight Data Sources
- Performs Parallel to Serial Conversion
- Permits Multiplexing from N lines to One Line
- Typical Propagation Delay Times:
  Select to Y Output . . . 22 ns
  Data Input to Y Output . . . 12 ns

SN29312 . . . J OR N DUAL-IN-LINE PACKAGE
SN39312 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



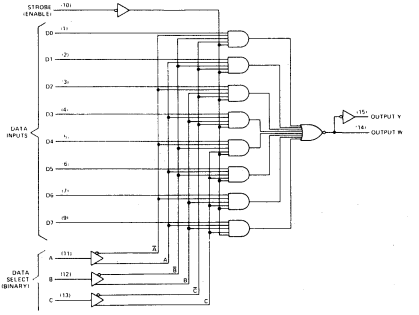
positive logic: see function table

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. Each SN29312/SN39312 has complementary outputs and a strobe. When the strobe is low, the function is enabled. A high level at the strobe forces the W output high, and the Y output low.

These improved data selectors/multiplexers feature select decoding gates which have symmetrical delay times through their complementary paths. This virtually eliminates transients from occurring at the outputs when the select inputs are changed with the outputs enabled (i.e., strobe low).

functional block diagram

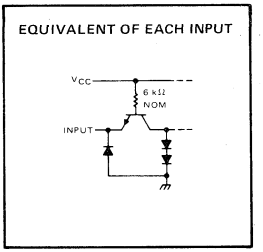


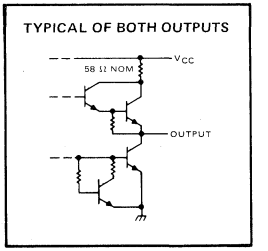
FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	G		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the respective D input

schematics of inputs and outputs





absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN29312 . . . . . 0°C to 75°C
SN39312 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN29312			SN39312			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		30	47	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with the strobe and data select inputs at 4.5 V, all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Strobe	Y	C_L = 15 pF, R_L = 400 Ω, See Note 3		19	28	ns
t_{PHL}					17	25	
t_{PLH}	Strobe	W			10	15	ns
t_{PHL}					14	21	
t_{PLH}	Any D	Y			12	18	ns
t_{PHL}					13	20	
t_{PLH}	Any D	W			7	12	ns
t_{PHL}					7	12	
t_{PLH}	Any Select	Y			20	30	ns
t_{PHL}					23	35	
t_{PLH}	Any Select	W			18	28	ns
t_{PHL}					16	25	

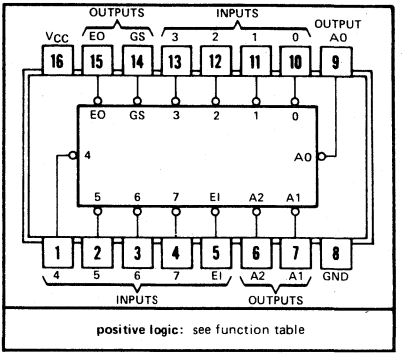
¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

TYPES SN29318, SN39318
8-LINE-TO-3-LINE PRIORITY ENCODERS

BULLETIN NO. DL-S 7211856, DECEMBER 1972

- Direct Replacement for Fairchild 9318
- For New Designs, SN74148 and SN54148 Are Recommended
- Encodes 8 Data Lines to 3-Line Binary (Octal)
- Applications Include:
  N-Bit Encoding
  Code Converters and Generators
- Typical Data Delay . . . 10 ns
- Typical Power Dissipation . . . 190 mW

SN29318 . . . J OR N DUAL-IN-LINE PACKAGE
SN39318 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)

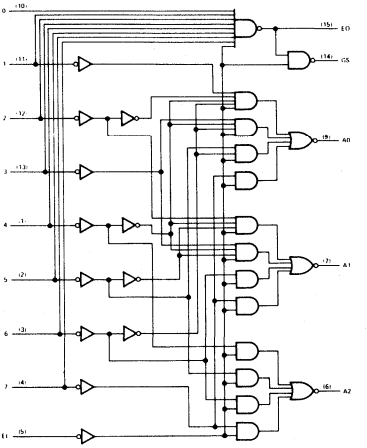


positive logic: see function table

description

The TTL encoder features priority decoding of the inputs to ensure that only the highest-order data line is encoded. The SN29318 and SN39318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. Data inputs and outputs are active at the low logic level.

functional block diagram



FUNCTION TABLE

INPUTS								OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = high level, L = low level, X = irrelevant

schematics of inputs and outputs

Same as SN54148/SN74148, see page 293.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: SN29318 . . . . . 0°C to 75°C
SN39318 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except intermitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between any two of the eight data lines, 0 through 7.

recommended operating conditions

	SN29318			SN39318			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	0 input	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Any input except 0					80	
I_{IL}	Low-level input current	0 input	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Any input except 0					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−35		−85	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3	Condition 1		40	60	mA
				Condition 2		35	55	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} (condition 1) is measured with inputs 7 and EI grounded, other inputs and outputs open; I_{CC} (condition 2) is measured with all inputs and outputs open.

5

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	WAVEFORM	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	0 thru 7	A0, A1, or A2	In-phase output	C_L = 15 pF, R_L = 400 Ω, See Note 4		10	15	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	A0, A1, or A2	Out-of-phase output			13	19	ns
t_{PHL}						10	15	
t_{PLH}	0 thru 7	EO	Out-of-phase output			6	10	ns
t_{PHL}						9	14	
t_{PLH}	0 thru 7	GS	In-phase output			14	21	ns
t_{PHL}						12	18	
t_{PLH}	EI	A0, A1, or A2	In-phase output			10	15	ns
t_{PHL}						10	15	
t_{PLH}	EI	GS	In-phase output			8	12	ns
t_{PHL}						10	15	
t_{PLH}	EI	EO	In-phase output			8	13	ns
t_{PHL}						13	19	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuits and waveforms are shown on page 148.

TYPES SN29322, SN39322
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS

BULLETIN NO. DL-S 7211855, DECEMBER 1972

features

- Direct Replacement for Fairchild 9322
- For New Designs, SN74157 and SN54157 Are Recommended
- Buffered Inputs and Outputs

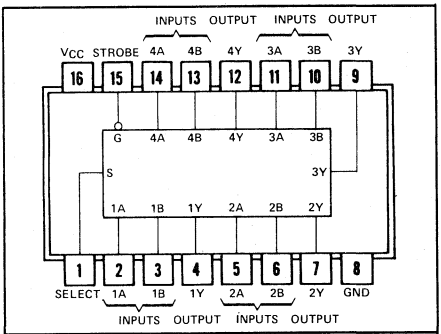
applications

- Expand Any Data Input Point
- Multiplex Dual-Data Buses
- Generate Four Functions of Two Variables (One Variable is Common)
- Source Programmable Counters

description

These monolithic data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

SN29322 . . . J OR N DUAL-IN-LINE PACKAGE
SN39322 . . . J DUAL-IN-LINE PACKAGE
(TOP VIEW)



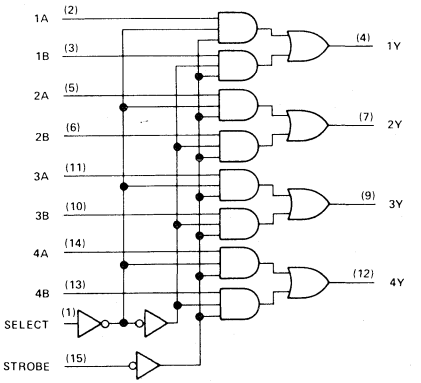
positive logic:
Low logic level at S selects A inputs.
High logic level at S selects B inputs.

FUNCTION TABLE

INPUTS				OUTPUT
STROBE	SELECT	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN29322 . . . . . 0°C to 75°C
SN39322 . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN29322			SN39322			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
High-level output current, I_{OH}			−800			−800	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	0		75	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN29322			SN39322			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−18		−55	−20		−55	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		30	48		30	48	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with 4.5 V applied to all inputs and all outputs open.

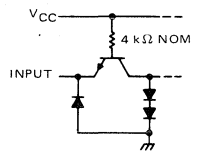
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	C_L = 15 pF, R_L = 400 Ω, See Note 3		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

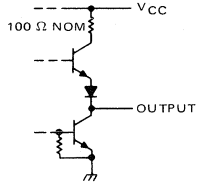
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 148.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS

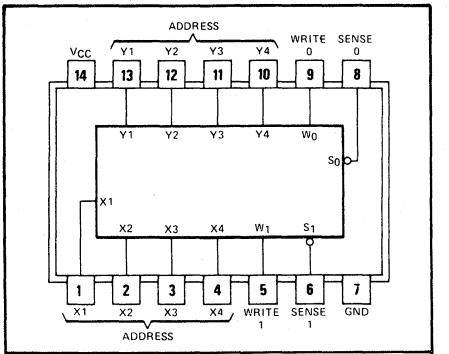


TYPES SN83433, SN93433
16-BIT ACTIVE-ELEMENT MEMORIES

BULLETIN NO. DL-S 7211859, DECEMBER 1972

- **Direct Replacement for Fairchild 93433**
- **For New Designs, SN7481A and SN5481A Are Recommended**

SN83433 . . . J DUAL-IN-LINE PACKAGE
SN93433 . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

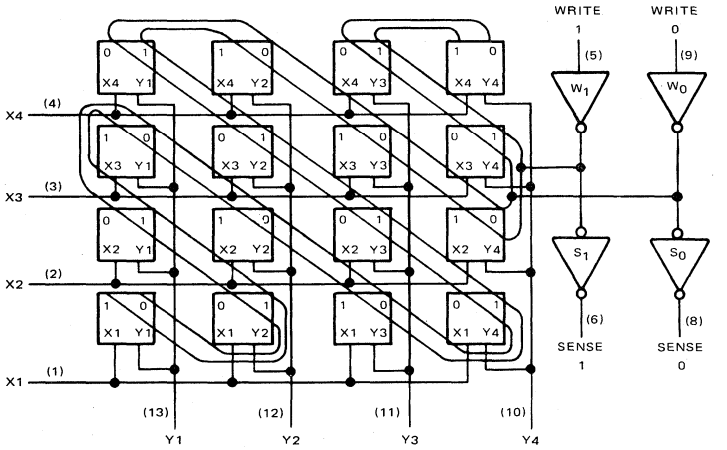


logic: see logic diagram

description

Each of these 16-bit active-element memories is a high-speed, monolithic, transistor-transistor-logic (TTL) array of 16 flip-flops and two write amplifiers interconnected to form a scratch-pad memory with direct-address and nondestructive read-out. For detailed descriptive information, see the description of SN5481A/SN7481A which is also applicable for these circuits.

logic diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Interemitter voltage (see Note 2)	5.5 V
High-level output voltage	5.5 V
Operating free-air temperature range: SN83433	−55°C to 125°C
SN93433	0°C to 75°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies to any X input in conjunction with any Y input.

recommended operating conditions

	SN83433			SN93433			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			20			40	mA
Width of write pulse, $t_{w(write)}$ (see Note 3)	20			20			ns
Address input setup time, t_{setup} (see Note 3)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN83433			SN93433			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level voltage at any input			2			2			V
V_{IL}	Low-level voltage at address inputs	to prevent writing				0.8			0.8	V
		to prevent sensing				1			1	
V_{IL}	Low-level voltage at write inputs					0.8			1	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
I_{OH}	High-level output current		V_{CC} = MIN, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX			0.4			0.4	V
I_I	Input current at maximum input voltage	Write	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
		Address				3			3	
I_{IH}	High-level input current	Write	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		Address	V_{CC} = MAX, V_I = 4.5 V			400			400	
I_{IL}	Low-level input current	Write	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		Address				−11			−11	
I_{CC}	Supply current		V_{CC} = MAX, All inputs at 0 V			65			65	mA
			V_{CC} = 5 V, All inputs at 0 V		45	60		45	60	

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switching characteristics, V_{CC} = 5 V, I_{OL} = MAX†, T_A = 25°C, see note 3

PARAMETER§	LOCATION ADDRESSED	TEST CONDITIONS	SN83433			SN93433			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{SR}	X1 – Y1	C_L = 30 pF		13			13		ns
		C_L = 200 pF		18	30		18	30	
t_{PHL}	X1 – Y1	C_L = 30 pF		11	19		12	20	ns
		C_L = 200 pF		17	26		18	27	
t_{PLH}		C_L = 30 pF		13	20		12	19	
		C_L = 200 pF		27	40		18	27	
t_{PHL}	X1 thru X4 and Y1	C_L = 30 pF		10	18		11	19	ns
		C_L = 200 pF		16	25		17	26	
t_{PLH}		C_L = 30 pF		13	20		13	20	
		C_L = 200 pF		27	40		19	28	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C.
§t_{SR} ≡ Sense recovery time after writing
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PLH} ≡ Propagation delay time, low-to-high-level output
NOTE 3: See Figure 1 for SN5481A/SN7481A, page 194.

54/74 Family Beam-Lead TTL Circuits

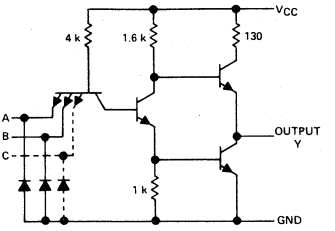
6

TYPES BL5400Y, BL5410Y, BL7400Y, BL7410Y
QUADRUPLE 2-INPUT, TRIPLE 3-INPUT POSITIVE-NAND GATES

BULLETIN NO. DL-S 7211864, DECEMBER 1972

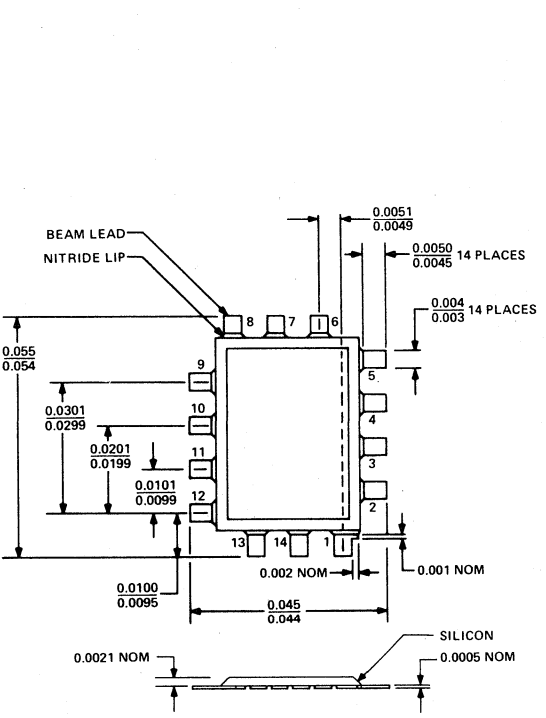
- BL5400Y/BL7400Y Chips When Assembled Display Characteristics Similar to SN5400/SN7400
- BL5410Y/BL7410Y Chips When Assembled Display Characteristics Similar to SN5410/SN7410
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

schematic (each gate)



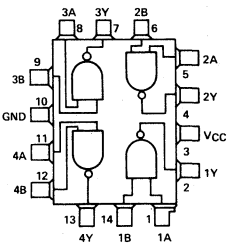
Resistor values shown are nominal and in ohms.

mechanical data and logic



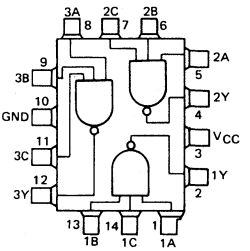
FORMAT 45

BL5400Y, BL7400Y



CHIP SHOWN
DIFFUSED SIDE DOWN
positive logic: $Y = \overline{AB}$

BL5410Y, BL7410Y



NC—No internal connection
CHIP SHOWN
DIFFUSED SIDE DOWN
positive logic: $Y = \overline{ABC}$

NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L' Circuits . . . . . −55°C to 125°C
BL74L' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54'			BL74'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.8 V, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	BL54'	−20		−55	mA
			BL74'	−18		−55	
I_{CCH}	Supply current, outputs high (average per gate)	V_{CC} = MAX, All inputs at 0 V			1	2	mA
I_{CCL}	Supply current, outputs low (average per gate)	V_{CC} = MAX, All inputs at 5 V			3	5.5	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

6

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Note 3		11	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 148.

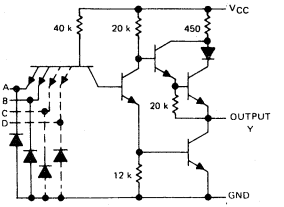
BEAM-LEAD LOW-POWER TTL CHIPS

TYPES BL54L00Y, BL54L20Y, BL74L00Y, BL74L20Y POSITIVE-NAND GATES

BULLETIN NO. DL-S 7211863, DECEMBER 1972

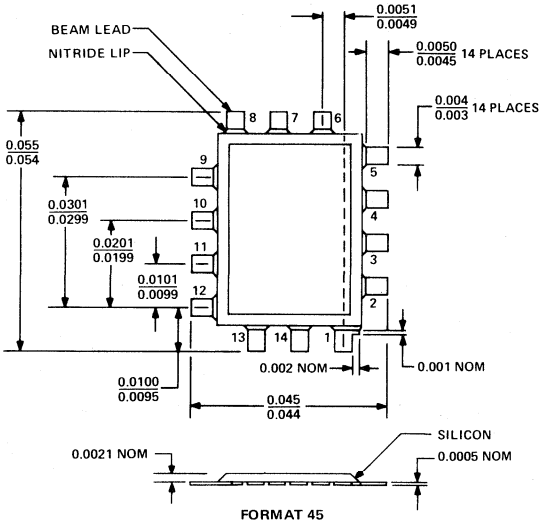
- BL54L00Y/SN74L00Y Chips When Assembled Display Characteristics Similar to SN54L00/SN74L00
- BL54L20Y/SN74L20Y Chips When Assembled Display Characteristics Similar to SN54L20/SN74L20
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

schematic (each gate)



Resistor values shown are nominal and in ohms.

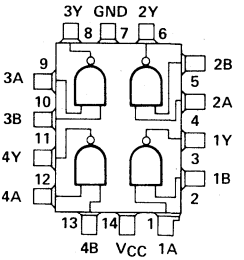
mechanical data and logic



FORMAT 45

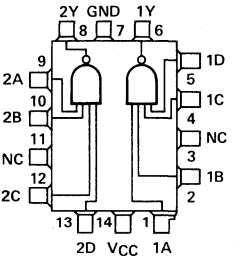
NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

BL54L00Y, BL74L00Y



CHIP SHOWN
DIFFUSED SIDE DOWN
positive logic: $Y = \overline{AB}$

BL54L20Y, BL74L20Y



NC—No internal connection
CHIP SHOWN
DIFFUSED SIDE DOWN
positive logic: $Y = \overline{ABCD}$

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L' Circuits . . . . . −55°C to 125°C
BL74L' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54L'			BL74L'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	BL54L'			BL74L'			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	−3		−15	−3		−15	mA
I_{CCH}	Supply current, all outputs high (average per gate)	V_{CC} = MAX, All inputs at 0 V		0.11	0.2		0.11	0.2	mA
I_{CCL}	Supply current, all outputs low (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.29	0.51		0.29	0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Note 3		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			31	60	ns

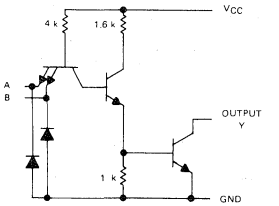
NOTE 3: Load circuit and voltage waveforms are shown on page 149.

TYPES BL5401Y, BL7401Y
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
(WITH OPEN-COLLECTOR OUTPUTS)

BULLETIN NO. DL-S 7211760, SEPTEMBER 1972

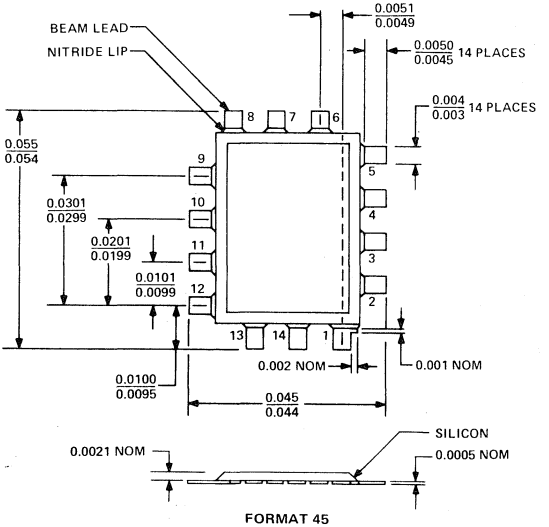
- BL5401Y/BL7401Y Chips When Assembled Display Characteristics Similar to SN5401/SN7401
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

schematic (each gate)

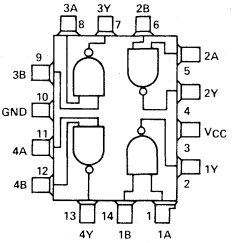


Resistor values shown are nominal and in ohms.

mechanical data and logic



FORMAT 45



CHIPS SHOWN
DIFFUSED SIDE DOWN
positive logic: $Y = \overline{AB}$

NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

6

TYPES BL5401Y, BL7401Y
QUADRUPLE 2-INPUT POSITIVE-NAND GATES
(WITH OPEN-COLLECTOR OUTPUTS)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54' Circuits . . . . . −55°C to 125°C
BL74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL5401Y			BL7401Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

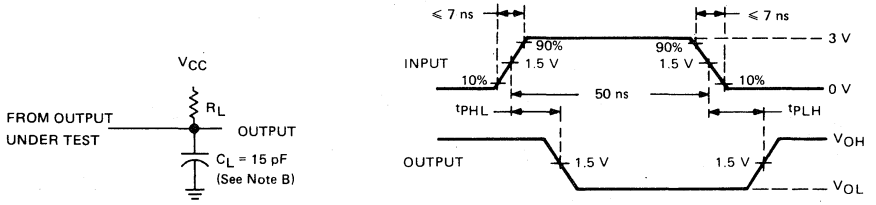
PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, outputs high	V_{CC} = MAX, All inputs at 0 V		4	8	mA
I_{CCL}	Supply current, outputs low	V_{CC} = MAX, All inputs at 5 V		12	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		35	45	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15	ns

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator having the following characteristics: PRR = 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1–PROPAGATION DELAY TIMES

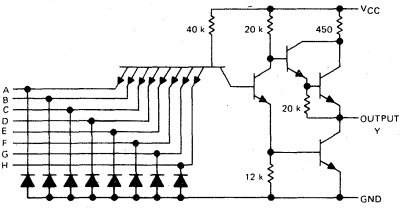
TEXAS INSTRUMENTS

TYPES BL54L30Y, BL74L30Y
8-INPUT POSITIVE-NAND GATES

BULLETIN NO. DL-S 7211584, DECEMBER 1971—REVISED DECEMBER 1972

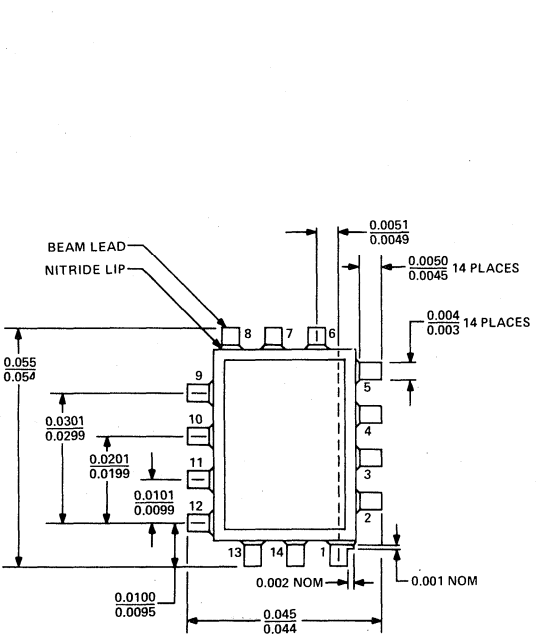
- BL54L30Y/BL74L30Y Chips When Assembled Display Characteristics Similar to SN54L30/SN74L30
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

schematic

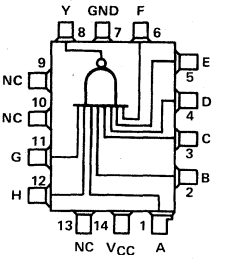


Resistor values are nominal in ohms.

mechanical data and logic



FORMAT 45



NC—No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN

positive logic: $Y = \overline{ABCDEFGH}$

NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L' Circuits . . . . . −55°C to 125°C
BL74L' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54L30Y			BL74L30Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	BL54L30Y			BL74L30Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_I = 0	−3		−15	−3		−15	mA
I_{CCH}	Supply current, output high	V_{CC} = MAX, All inputs at 0 V		0.11	0.33		0.11	0.2	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, All inputs at 5 V		0.29	0.51		0.29	0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Note 3		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			70	100	ns

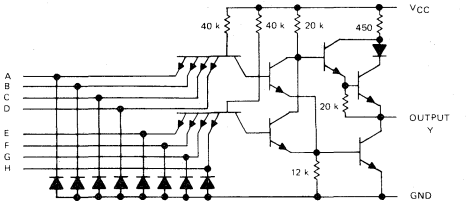
NOTE 3: Load circuit and voltage waveforms are shown on page 149.

TYPES BL54L55Y, BL74L55Y
2-WIDE 4-INPUT AND-OR-INVERT GATES

BULLETIN NO. DL-S 7211585, DECEMBER 1971—REVISED DECEMBER 1972

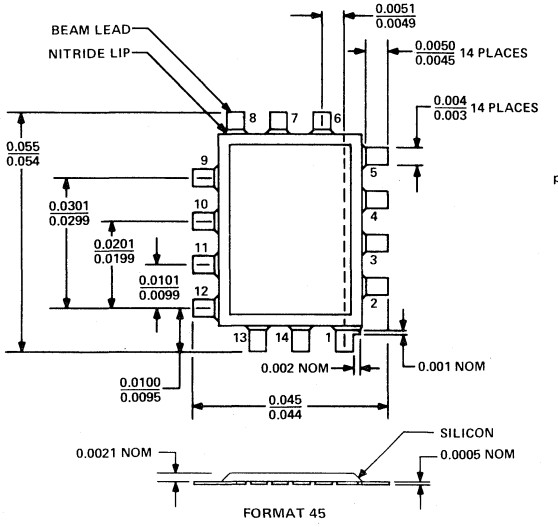
- BL54L55Y/BL74L55Y Chips When Assembled Display Characteristics Similar to SN54L55/SN74L55
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

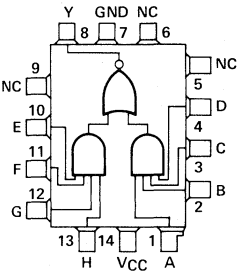
schematic



Resistor values are nominal in ohms

mechanical data and logic





NC—No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN

positive logic: $Y = \overline{(ABCD) + (EFGH)}$

NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L' Circuits . . . . . −55°C to 125°C
BL74L' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54L55Y			BL74L55Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	BL54L55Y			BL74L55Y			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_I = 0	−3		−15	−3		−15	mA
I_{CCH}	Supply current, output high	V_{CC} = MAX, All inputs at 0 V		0.22	0.4		0.22	0.4	mA
I_{CCL}	Supply current, output low	V_{CC} = MAX, All inputs at 5 V		0.38	0.65		0.38	0.65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Note 3		50	90	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	ns

NOTE 3: Load circuit and voltage waveforms are shown on page 149.

BEAM-LEAD LOW-POWER TTL CHIPS

TYPES BL54L67Y, BL74L67Y J-K EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7211635, JANUARY 1972—REVISED DECEMBER 1972

- BL54L67Y/BL74L67Y Chips When Assembled Can Replace SN54L72/SN74L72 in Most Applications
- Silicon-Nitride-Sealed Junctions
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

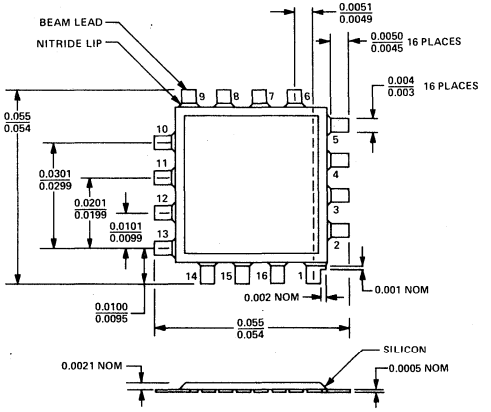
H = high level (steady state), L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

description

These edge-triggered flip-flop circuits feature gated J and K inputs and asynchronous preset and clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change while the clock pulse is high and the bistable will perform according to the truth table, provided that minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

The BL54L67Y chip is characterized for operation over the full military temperature range of −55°C to 125°C; the BL74L67Y is characterized for operation from 0°C to 70°C.

mechanical data



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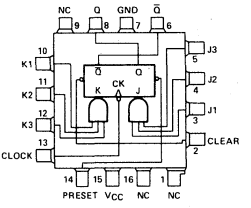


NC—No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN

↓.. Dynamic input activated by a transition from a high level to a low level.

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

'2 PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L67Y . . . . . −55°C to 125°C
BL74L67Y . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54L67Y			BL74L67Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Width of clock pulse, $t_{w(clock)}$	200			200			ns
Width of preset pulse, $t_{w(preset)}$	100			100			ns
Width of clear pulse, $t_{w(clear)}$	100			100			ns
Input setup time, t_{setup}	30			30			ns
Input hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	BL54L67Y			BL74L67Y			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	Any J or K	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		Preset, clear, or clock				200			200	
I_{IH}	High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		Preset or clear				30			30	
		Clock				40			40	
I_{IL}	Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
		Preset or clear				−0.54			−0.54	
		Clock				−0.72			−0.72	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		0.76	1.44		0.76	1.44	mA

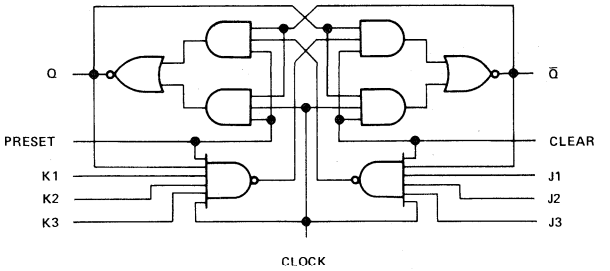
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, clock grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 4

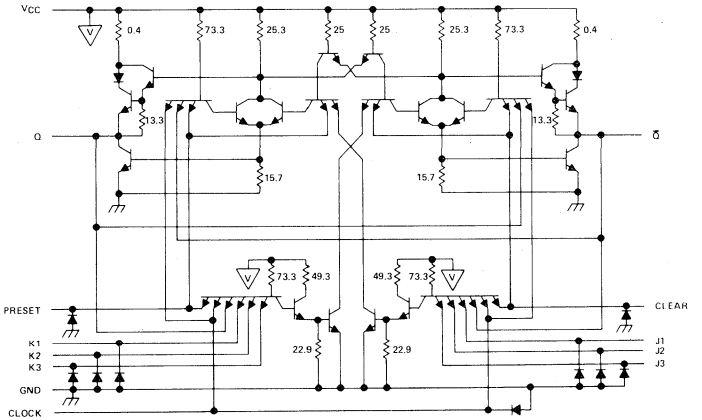
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			C_L = 50 pF, R_L = 4 kΩ		2.5	10		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ			35	75	ns
t_{PHL}	Preset or clear	$\overline{Q}$ or Q	C_L = 50 pF, R_L = 4 kΩ	$V_{I(clock)}$ = 2.4 V		60	150	ns
				$V_{I(clock)}$ = 0			200	
t_{PLH}	Clock	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ		10	35	75	ns
t_{PHL}	Clock	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ		10	60	150	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 149.

functional block diagram



schematic



▽ . . . V_{CC} bus

Resistor values shown are nominal in kilohms.

BEAM-LEAD LOW-POWER TTL CHIPS

TYPES BL54L68Y, BL74L68Y DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7211634, JANUARY 1972—REVISED DECEMBER 1972

- BL54L68Y/BL74L68Y Chips When Assembled Can Replace SN54L73/SN74L73 in Most Applications
- Silicon-Nitride-Sealed Junctions
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

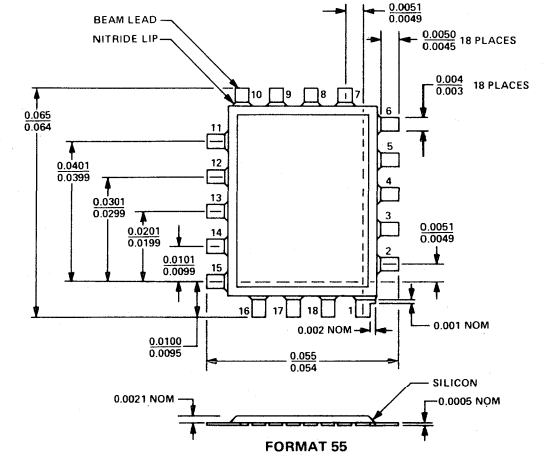
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were establsihed
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.

description

These edge-triggered dual flip-flop circuits feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change while the clock pulse is high and the bistable will perform according to the truth table, provided that minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

The BL54L68Y chip is characterized for operation over the full military temperature range of −55°C to 125°C; the BL74L68Y is characterized for operation from 0°C to 70°C.

mechanical data



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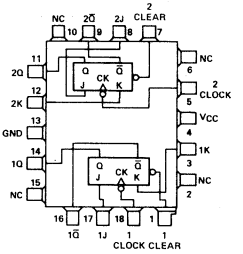


NC—No internal connection

CHIP SHOWN DIFFUSED SIDE DOWN

Dynamic input activated by a transition from a high level to a low level.

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L68Y . . . . . −55°C to 125°C
BL74L68Y . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54L68Y			BL74L68Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Width of clock pulse, $t_{w(clock)}$	200			200			ns
Width of clear pulse, $t_{w(clear)}$	100			100			ns
Input setup time, t_{setup}	30			30			ns
Input hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	BL54L68Y			BL74L68Y			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	Any J or K	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		Clear or clock				200			200	
I_{IH}	High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		Clear				30			30	
		Clock				40			40	
I_{IL}	Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	mA
		Clear				−0.54			−0.54	
		Clock				−0.72			−0.72	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 3		0.76	1.44		0.76	1.44	mA

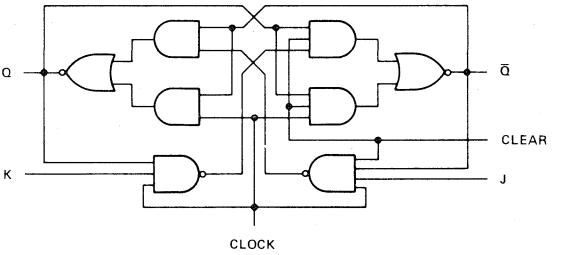
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, clocks grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 4

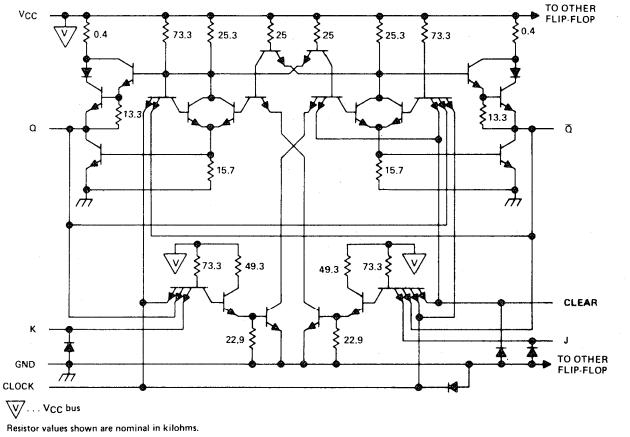
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			C_L = 50 pF, R_L = 4 kΩ		2.5	10		MHz
t_{PLH}	Clear	$\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ			35	75	ns
t_{PHL}	Clear	Q	C_L = 50 pF, R_L = 4 kΩ	$V_{I(clock)}$ = 2.4 V		60	150	ns
				$V_{I(clock)}$ = 0			200	
t_{PLH}	Clock	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ		10	35	75	ns
t_{PHL}	Clock	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ		10	60	150	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 149.

functional block diagram (each flip-flop)



schematic (each flip-flop)



Resistor values shown are nominal in kilohms.

TEXAS INSTRUMENTS

BEAM-LEAD LOW-POWER TTL CHIPS

TYPES BL54L69Y, BL74L69Y DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7211661, JANUARY 1972—REVISED DECEMBER 1972

- BL54L69Y/BL74L69Y Chips When Assembled Can Replace SN54L78/SN74L78 in Most Applications
- Silicon-Nitride-Sealed Junctions
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

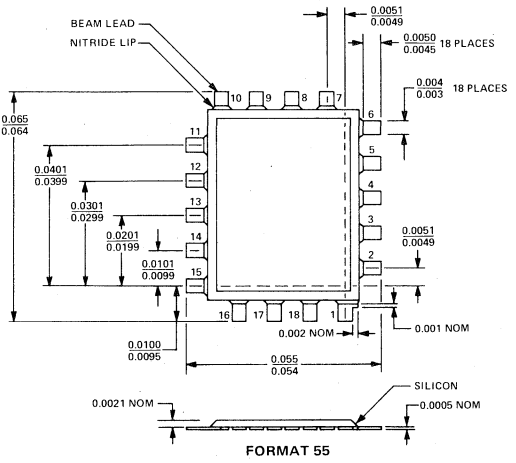
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each ↓ clock transition.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

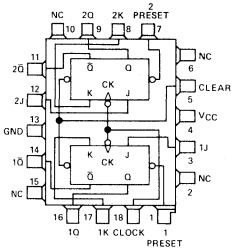
description

These edge-triggered dual flip-flop circuits feature individual J, K, and preset inputs to each flip-flop and a common clock and clear. When the clock goes high, the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change while the clock pulse is high and the bistable will perform according to the truth table, provided that minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse. Preset and clear inputs operate independently of the clock.

The BL54L69Y chip is characterized for operation over the full military temperature range of −55°C to 125°C; the BL74L69Y is characterized for operation from 0°C to 70°C.

mechanical data





CHIP SHOWN
DIFFUSED SIDE DOWN

Dynamic input activated by a transition from a high level to a low level.

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L69Y . . . . . −55°C to 125°C
BL74L69Y . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL54L69Y			BL74L69Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−100			−200	μA
Low-level output current, I_{OL}			2			3.6	mA
Width of clock pulse, $t_{w(clock)}$	200			200			ns
Width of preset pulse, $t_{w(preset)}$	100			100			ns
Width of clear pulse, $t_{w(clear)}$	100			100			ns
Input setup time, t_{setup}	30			30			ns
Input hold time, t_{hold}	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	BL54L69Y			BL74L69Y			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.7	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4	3.3		2.4	3.2		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX		0.15	0.3		0.2	0.4	V
I_I	Input current at maximum input voltage	Any J or K	V_{CC} = MAX, V_I = 5.5 V			100			100	μA
		Preset				200			200	
		Clear or clock				400			400	
I_{IH}	High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V			10			10	μA
		Preset				30			30	
		Clear				60			60	
		Clock				80			80	
I_{IL}	Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.3 V			−0.18			−0.18	μA
		Preset				−0.54			−0.54	
		Clear or clock				−1.44			−1.44	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−3		−15	−3		−15	mA
I_{CC}	Supply current (average per flip-flop)		V_{CC} = MAX, See Note 3		0.76	1.44		0.76	1.44	mA

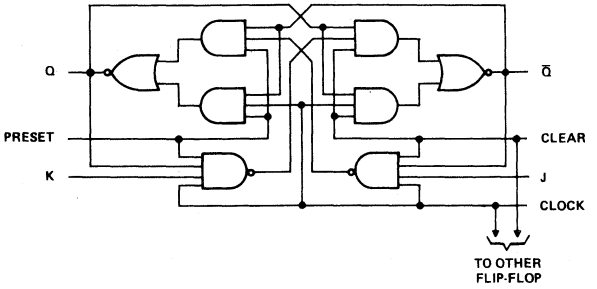
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, clock grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, see note 4

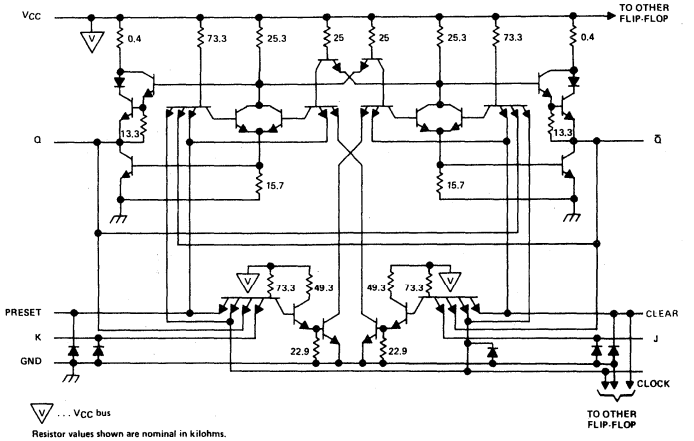
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			C_L = 50 pF, R_L = 4 kΩ		2.5	10		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ			35	75	ns
t_{PHL}	Preset or clear	$\overline{Q}$ or Q	C_L = 50 pF, R_L = 4 kΩ	$V_{I(clock)}$ = 2.4 V		60	150	ns
				$V_{I(clock)}$ = 0			200	
t_{PLH}	Clock	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ		10	35	75	ns
t_{PHL}	Clock	Q or $\overline{Q}$	C_L = 50 pF, R_L = 4 kΩ		10	60	150	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 149.

functional block diagram (each flip-flop)



schematic (each flip-flop)



6

TYPES BL5473Y, BL7473Y
DUAL J-K MASTER-SLAVE FLIP-FLOPS

BULLETIN NO. DL-S 7211762, NOVEMBER 1972

- BL5473Y/BL7473Y Chips When Assembled Can Replace SN5473/SN7473 in Most Applications
- Silicon Nitride Sealed Junctions
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

FUNCTION TABLE
(EACH FLIP-FLOP)

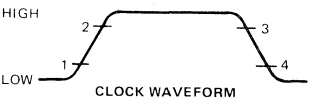
INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

H = high level (steady state), L = low level (steady state)
X = irrelevant
⎍ = high level pulse; other inputs should be held constant while the clock is high.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each high-to-low clock transition.

description

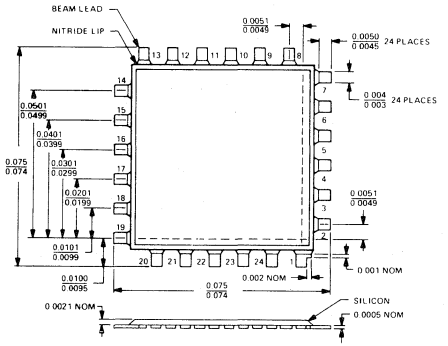
These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.



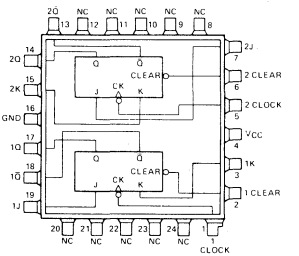
CLOCK WAVEFORM

mechanical data



FORMAT 70

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.



NC-No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN

Dynamic input activated by a transition from a high level to a low level.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54' Circuits . . . . . −55°C to 125°C
BL74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL5473Y			BL7473Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		15	0		15	MHz
Width of clock pulse, $t_{w(clock)}$	20			20			ns
Width of clear pulse, $t_{w(clear)}$	25			25			ns
Input setup time, t_{setup}	0↑			0↑			ns
Input hold time, t_{hold}	0↓			0↓			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	J or K	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Clear or clock					80	
I_{IL}	Low-level input current	J or K	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Clear or clock					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	BL5473Y	−20		−57	mA
				BL7473Y	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			20	40	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

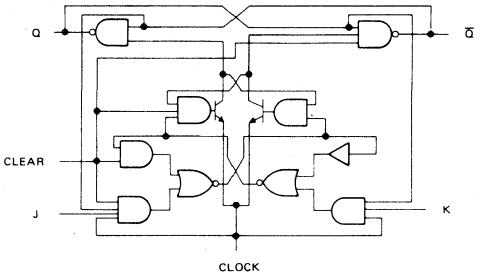
NOTE 3. I_{CC} is measured with outputs open, clocks grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

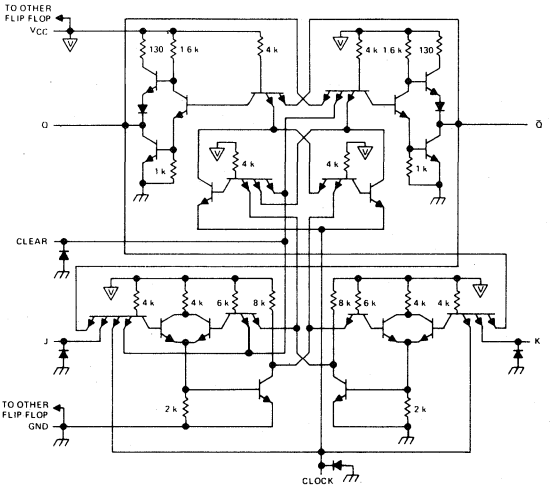
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 4	15	20		MHz
t_{PLH}	Clear	$\overline{Q}$			16	25	ns
t_{PHL}	Clear	Q			25	40	ns
t_{PLH}	Clock	Q or $\overline{Q}$		10	16	25	ns
t_{PHL}	Clock	Q or $\overline{Q}$		10	25	40	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

functional block diagram (each flip-flop)



schematic (each flip-flop)



▽ . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

TYPES BL5474Y, BL7474Y
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

BULLETIN NO. DL-S 7211761, SEPTEMBER 1972

- BL5474Y/BL7474Y Chips When Assembled Can Replace SN5474/SN7474 in Most Applications
- Silicon-Nitride-Sealed Junctions
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

FUNCTION TABLE
(EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

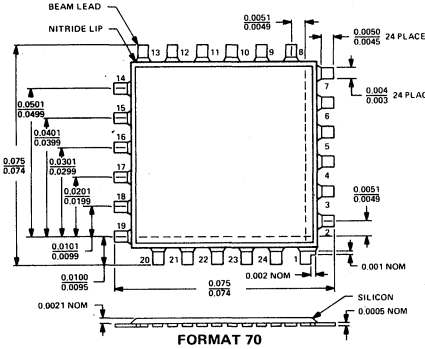
H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

description

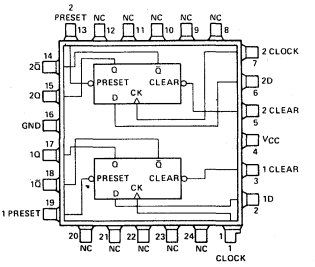
These dual D-type edge-triggered flip-flop circuits feature individual preset, clear, clock, and D inputs and complementary outputs for each flip-flop. Preset and clear inputs are independent of the clock. When the preset and clear inputs are inactive (high), data at the D input meeting the setup time requirements is transferred to the outputs on the positive transition of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

The BL5474Y chip is characterized for operation over the full military temperature range of −55°C to 125°C; the BL7474Y is characterized for operation from 0°C to 70°C.

mechanical data



FORMAT 70



NC—No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN

. . . Dynamic input activated by a transition from a low level to a high level.

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

6

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54' Circuits . . . . . −55°C to 125°C
BL74' Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	BL5474Y			BL7474Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		15	0		15	MHz
Width of clock, preset, or clear pulse, t_w	30			30			ns
Input setup time, t_{setup}	20			20			ns
Input hold time, t_{hold}	5			5			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −400 μA		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA			0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	D	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Preset or clock					80	
		Clear					120	
I_{IL}	Low-level input current	D or preset	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Clear or clock					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	BL5474Y	−20		−57	mA
				BL7474Y	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 3			17	30	mA

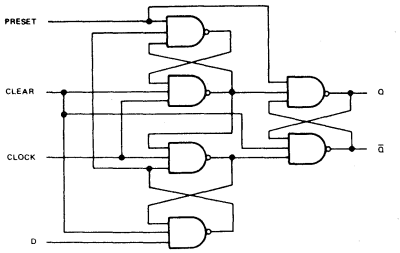
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, clock grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

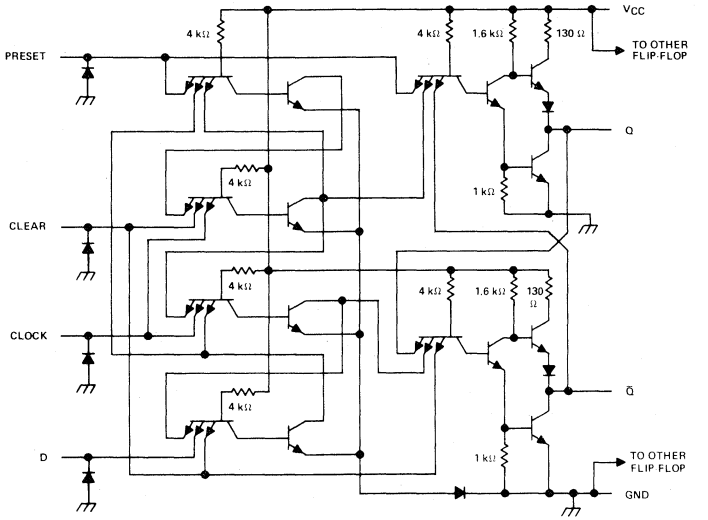
PARAMETER §	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 4	15	25		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$				25	ns
t_{PHL}	Preset or clear	$\overline{Q}$ or Q				40	ns
t_{PLH}	Clock	Q or $\overline{Q}$		10	14	25	ns
t_{PHL}	Clock	Q or $\overline{Q}$		10	20	40	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output, t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 148.

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Resistor values shown are nominal.

6

BEAM-LEAD LOW-POWER *SCHOTTKY*† CHIPS

SERIES BL54LS, BL74LS

BULLETIN NO. DL-S 7211870, DECEMBER 1972

- Silicon-Nitride-Sealed Junctions
- Gold Beams
- Available in Two Temperature Ranges:
  Series BL54LS . . . −55°C to 125°C
  Series BL74LS . . . 0°C to 70°C

description

Series BL54LS/BL74LS integrated circuit chips comprise a family of TTL designed for general purpose and military high-reliability applications and feature low power with medium operating speed. These chips utilize beam-lead sealed-junction technology and may be combined to form more complex beam-lead assemblies. The chips when assembled exhibit characteristics comparable to the Series 54LS/74LS devices of the same type number.

DEVICE TYPES		FUNCTION	TYPICAL AVERAGE PROPAGATION DELAY TIME	TYPICAL TOTAL POWER DISSIPATION
BL54LS00	BL74LS00	Quadruple 2-Input NAND Gates	9.5 ns	8 mW
BL54LS01	BL74LS01	Quadruple 2-Input NAND Gates with Open-Collector Outputs	16 ns	8 mW
BL54LS02	BL74LS02	Quadruple 2-Input NOR Gates	10 ns	11 mW
BL54LS03	BL74LS03	Quarduple 2-Input NAND Gates with Open-Collector Outputs	16 ns	8 mW
BL54LS04	BL74LS04	Hex Inverters	9.5 ns	12 mW
BL54LS05	BL74LS05	Hex Inverters with Open-Collector Outputs	16 ns	12 mW
BL54LS08	BL74LS08	Quadruple 2-Input AND Gates	12 ns	23 mW
BL54LS09	BL74LS09	Quadruple 2-Input AND Gates with Open-Collector Outputs	20 ns	17 mW
BL54LS10	BL74LS10	Triple 3-Input NAND Gates	9.5 ns	6 mW
BL54LS11	BL74LS11	Triple 3-Input AND Gates	12 ns	13 mW
BL54LS15	BL74LS15	Triple 3-Input AND Gates with Open-Collector Outputs	20 ns	13 mW
BL54LS20	BL74LS20	Dual 4-Input NAND Gates	9.5 ns	4 mW
BL54LS21	BL74LS21	Dual 4-Input AND Gates	12 ns	8.5 mW
BL54LS22	BL74LS22	Dual 4-Input NAND Gates with Open-Collector Outputs	16 ns	4 mW
BL54LS28	BL74LS28	Quadruple 2-Input NOR Buffers	12 ns	22 mW
BL54LS30	BL74LS30	8-Input NAND Gates	17 ns	2 mW
BL54LS32	BL74LS32	Quadruple 2-Input OR Gates	14 ns	20 mW
BL54LS33	BL74LS33	Quadruple 2-Input NOR Buffers with Open-Collector Outputs	19 ns	22 mW
BL54LS37	BL74LS37	Quadruple 2-Input NAND Buffers	12 ns	17 mW
BL54LS38	BL74LS38	Quadruple 2-Input NAND Buffers with Open-Collector Outputs	19 ns	17 mW
BL54LS51	BL74LS51	Dual 2-Wide 2-Input AND-OR-INVERT Gate	12.5 ns	5.5 mW
BL54LS54	BL74LS54	4-Wide 2-3-3-2-Input AND-OR-INVERT Gates	12.5 ns	4.5 mW
BL54LS55	BL74LS55	2-Wide 4-Input AND-OR-INVERT Gates	12.5 ns	2.75 mW
BL54LS95A	BL74LS95A	4-Bit Right-Shift Left-Shift Registers	33 ns	50 mW
BL54LS138	BL74LS138	3-Line-to-8-Line Decoders/Demultiplexers	20 ns	32 mW
BL54LS139	BL74LS139	Dual 2-Line-to-4-Line Decoders/Demultiplexers	19 ns	34 mW
BL54LS153	BL74LS153	Dual 4-Line-to-1-Line Data Selectors/Multiplexers	20 ns	31 mW
BL54LS155	BL74LS155	Dual 2-Line-to-4-Line Decoders/Demultiplexers	17 ns	31 mW
BL54LS181	BL74LS181	Arithmetic Logic Units/Function Generators	21 ns	105 mW
BL54LS194	BL74LS194	4-Bit Bidirectional Universal Shift Registers	31 ns	60 mW
BL54LS195	BL74LS195	4-Bit Parallel-Access Shift Registers	24 ns	50 mW
BL54LS196	BL74LS196	30-MHz Presettable Decade Counters/Latches	25 ns	60 mW
BL54LS197	BL74LS197	30-MHz Presettable Binary Counters/Latches	30 ns	60 mW
BL54LS253	BL74LS253	Dual 4-Line-to-1-Line Data Selectors/Multiplexers with Three-State Outputs	16 ns	35 mW
BL54LS295	BL74LS295	4-Bit Right-Shift Left-Shift Registers with Three-State Outputs	44 ns	60 mW

In addition, other circuits with any combination of 60 gates can be supplied by implementing a design on a random logic bar. These circuits have a typical propagation delay time of eight to ten nanoseconds per gate and a typical power dissipation of one to two milliwatts per gate and are supplied on a Format-135 beam-lead chip.

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

GATES

BEAM ASSIGNMENTS

TYPE	BL54LS01Y BL54LS02Y BL74LS01Y BL74LS02Y	BL54LS00Y BL54LS03Y BL74LS00Y BL74LS03Y	BL54LS04Y BL54LS05Y BL74LS04Y BL74LS05Y	BL54LS08Y BL54LS09Y BL74LS08Y BL74LS09Y	BL54LS10Y BL74LS10Y	BL54LS11Y BL54LS15Y BL74LS11Y BL74LS15Y	BL54LS20Y BL54LS22Y BL74LS20Y BL74LS22Y
FORMAT / BEAM	50	50	50	50	50	50	50
1	1A	1A	1Y	1A	1A	1A	1A
2	1Y	1B	1A	1Y	1B	2A	1B
3	V_{CC}	V_{CC}	V_{CC}	NC	V_{CC}	NC	V_{CC}
4	NC	NC	2A	2A	NC	2B	NC
5	2Y	2A	NC	2B	1C	2C	2A
6	2A	2B	2Y	2Y	1Y	2Y	2B
7	2B	2Y	3A	GND	2A	GND	NC
8	3Y	3A	3Y	3Y	2B	3Y	2C
9	3A	3B	4A	3A	2C	3A	2D
10	3B	3Y	4Y	3B	2Y	3B	2Y
11	GND	GND	GND	NC	GND	NC	GND
12	4A	NC	NC	4Y	NC	3C	NC
13	4B	4Y	5Y	4A	3Y	1Y	1Y
14	NC	4A	5A	4B	3A	1B	1C
15	4Y	4B	6Y	V_{CC}	3B	V_{CC}	1D
16	1B	1Y	6A	1B	3C	1C	NC

BEAM ASSIGNMENTS

TYPE	BL54LS21Y BL74LS21Y	BL54LS28Y BL54LS33Y BL74LS28Y BL74LS33Y	BL54LS30Y BL74LS30Y	BL54LS32Y BL54LS37Y BL54LS38Y BL74LS32Y BL74LS37Y BL74LS38Y	BL54LS51Y BL74LS51Y	BL54LS54Y BL74LS54Y	BL54LS55Y BL74LS55Y
FORMAT / BEAM	50	50	50	50	50	50	50
1	1A	1A	NC	1A	1A	A	A
2	NC	1B	A	1Y	1B	B	B
3	NC	NC	V_{CC}	NC	V_{CC}	V_{CC}	V_{CC}
4	1B	2Y	B	2A	1C	C	E
5	1C	2A	C	2B	2A	D	F
6	1Y	2B	D	2Y	NC	NC	G
7	GND	GND	E	GND	2B	E	H
8	2Y	3A	F	3Y	2C	F	NC
9	2A	3B	G	3A	2D	G	NC
10	2B	3Y	NC	3B	2Y	Y	NC
11	NC	NC	GND	NC	GND	GND	GND
12	NC	4A	NC	4Y	NC	NC	NC
13	2C	4B	Y	4A	1Y	NC	Y
14	2D	4Y	NC	4B	1D	H	NC
15	V_{CC}	V_{CC}	NC	V_{CC}	1E	I	C
16	1D	1Y	H	1B	1F	J	D

NC—No internal connection

See logic equations on page 573.

MSI

BEAM ASSIGNMENTS

A Y suffix, omitted here for the sake of space, should be used with all chip type numbers.

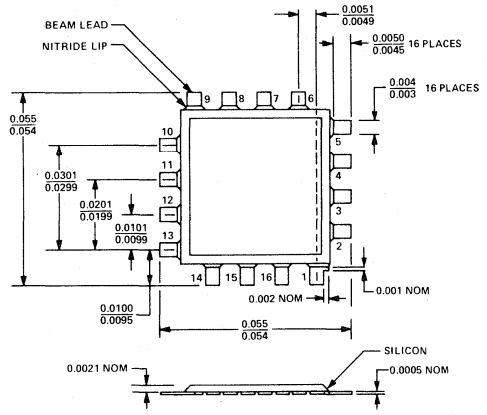
TYPE	BL54LS95A BL74LS95A	BL54LS138 BL74LS138	BL54LS139 BL74LS139	BL54LS153 BL74LS153	BL54LS155 BL74LS155	BL54LS181 BL74LS181	BL54LS194 BL74LS194	BL54LS195 BL74LS195	BL54LS196 BL54LS197 BL74LS196 BL74LS197	BL54LS253 BL74LS253	BL54LS295 BL74LS295
FORMAT / BEAM	65	65	65	60	65	75	65	65	65	60	65
1	Serial input	G2A†	Select 1A	B Select	Strobe 1G	S3	Shift R serial in	Serial in J	NC	B Select	Serial input
2	Input A	G1	NC	1C3	NC	S2	Parallel input A	Serial in $\overline{K}$	Q_C	1C3	Input A
3	Input B	NC	Select 1B	1C2	Select B	S1	Parallel input B	Parallel input A	Data C	1C2	Input B
4	NC	Y7	NC	1C1	NC	S0	NC	NC	NC	1C1	NC
5	Input C	Gnd	1Y0	1C0	1Y3	C_n	Parallel input C	Parallel input B	Data A	1C0	Input C
6	Input D	Y6	1Y1	NC	1Y2	M	Parallel input D	Parallel input C	Q_A	NC	Input D
7	NC	Y5	1Y2	1Y	1Y1	NC	Shift L serial in	Parallel input D	NC	1Y	NC
8	Mode control	NC	NC	NC	NC	F0	Gnd	Gnd	NC	NC	Mode control
9	Gnd	Y4	1Y3	Gnd	1Y0	F1	S0	NC	Clock 2	Gnd	Gnd
10	NC	NC	Gnd	NC	Gnd	NC	NC	NC	Gnd	NC	NC
11	Clock 2 L-shift	Y3	2Y3	2Y	2Y0	F2	S1	Shift/ load	Clock 1	2Y	Output control
12	Clock 1 R-shift	Y2	2Y2	2C0	2Y1	Gnd	NC	Clock	NC	2C0	Clock
13	NC	Y1	2Y1	2C1	2Y2	F3	Clock	$\overline{Q}_D$	Q_B	2C1	NC
14	Q_D	Y0	2Y0	2C2	2Y3	A = B	Q_D	Q_D	Data B	2C2	Q_D
15	Q_C	V_{CC}	Select 2B	2C3	Select A	P	Q_C	Q_C	Data D	2C3	Q_C
16	Q_B	A Select	NC	A Select	NC	C_{n+4}	Q_B	Q_B	Q_D	A Select	Q_B
17	NC	B Select	Select 2A	Strobe 2G	Strobe 2G	G	NC	NC	NC	Control 2G	NC
18	Q_A	NC	NC	V_{CC}	NC	B3	Q_A	Q_A	NC	V_{CC}	Q_A
19	V_{CC}	C Select	2G	NC	Data 2C	A3	V_{CC}	V_{CC}	Clear	NC	V_{CC}
20	NC	NC	V_{CC}	Strobe 1G	V_{CC}	B2	NC	NC	V_{CC}	Control 1G	NC
21	NC	G2B†	NC		NC	A2	NC	NC	NC		NC
22	NC	NC	1G		Data 1C	B1	Clear	Clear	Count/ load		NC
23						A1					
24						V_{CC}					
25						B0					
26						A0					

NC—No internal connection

†Inputs G2A and G2B of 'LS138 chips are interchangeable.

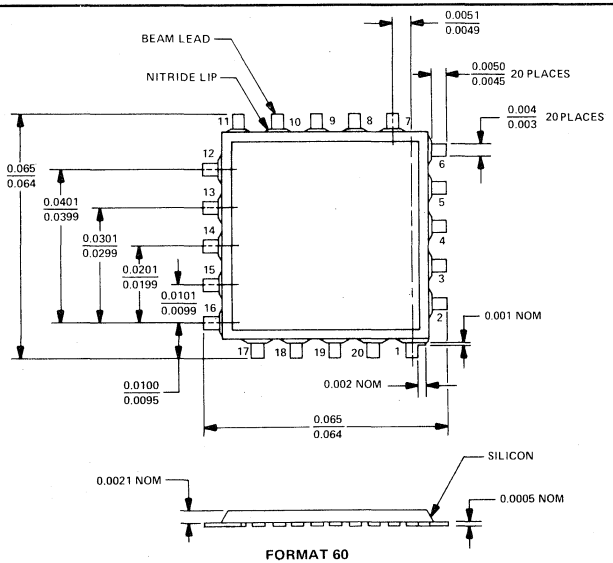
6

MECHANICAL DATA FOR BEAM-LEAD CHIPS



FORMAT 50

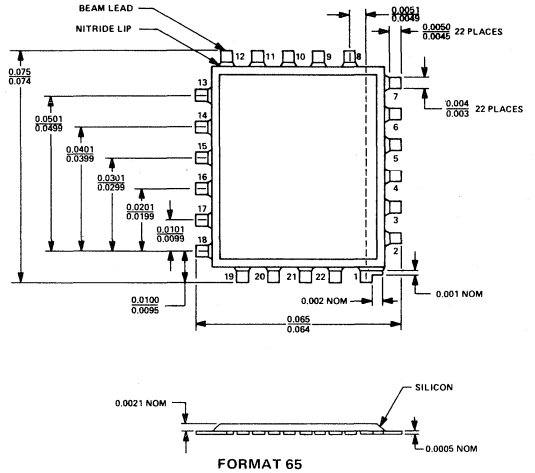
NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.



FORMAT 60

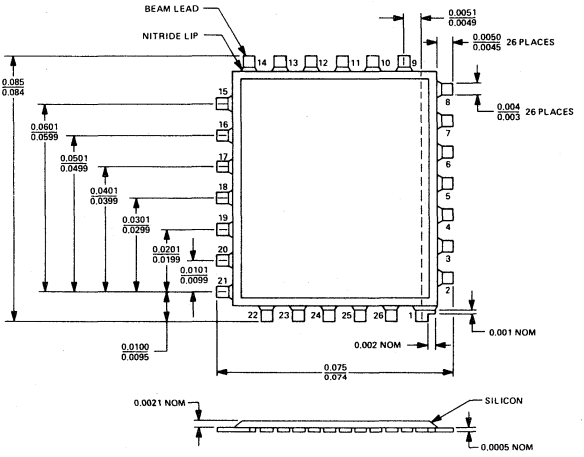
NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

MECHANICAL DATA FOR BEAM-LEAD CHIPS



FORMAT 65

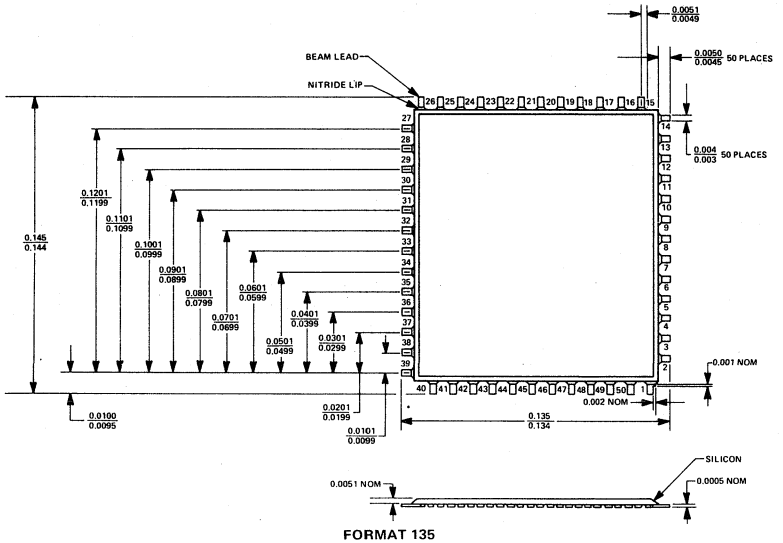
NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.



FORMAT 75

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

MECHANICAL DATA FOR BEAM-LEAD CHIPS



FORMAT 135

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

SSI LOGIC EQUATIONS

positive logic:	
'LS00Y, 'LS01Y, 'LS03Y	$Y = \overline{AB}$
'LS02Y	$Y = \overline{A+B}$
'LS04Y, 'LS05Y	$Y = \overline{A}$
'LS08Y, 'LS09Y	$Y = AB$
'LS10Y	$Y = \overline{ABC}$
'LS11Y, 'LS15Y	$Y = ABC$
'LS20Y, 'LS22Y	$Y = \overline{ABCD}$
'LS21Y	$Y = ABCD$
'LS28Y	$Y = \overline{A+B}$
'LS30Y	$Y = \overline{ABCDEFGH}$
'LS32Y	$Y = A+B$
'LS33Y	$Y = \overline{A+B}$
'LS37Y, 'LS38Y	$Y = \overline{AB}$
'LS51Y	$1Y = \overline{(1A \cdot 1B \cdot 1C)+(1D \cdot 1E \cdot 1F)}$
	$2Y = \overline{(2A \cdot 2B)+(2C \cdot 2D)}$
'LS54Y (See Note)	$Y = \overline{AB+CD+EFG+HIJ}$
'LS55Y	$Y = \overline{ABCD+EFGH}$

NOTE: The difference between this logic equation and the one published for the SN54LS54/SN74LS54, $Y = \overline{AB+CDE+FGH+IJ}$, is caused only by the fact that the inputs of the two different circuits are each designated starting with A at beam 1 or lead 1. If the input at beam 4 is bonded to pin 1 of a package with the other connections made in sequence, then the 2-3-3-2 input configuration of the SN versions will be achieved.

6

54/74 Family Radiation-Hardened Circuits

SERIES RSN54, RSN54H, RSN54L
RADIATION-HARDENED TTL INTEGRATED CIRCUITS

BULLETIN NO. DL-S 7211868, DECEMBER 1972

TTL INTEGRATED CIRCUITS WITH HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- High D-C Noise Margin . . . 1 Volt Typical
- Low Output Impedance Provides Low A-C Noise Susceptibility
- Waveform Integrity Maintained over Full Range of Loading and Temperature Conditions
- Normalized Fan-Out to Ten Loads

SERIES	TYPICAL NAND-GATE POWER DISSIPATION (50% DUTY CYCLE)	TYPICAL GATE PROPAGATION DELAY TIMES (C_L = 50 pF)
RSN54	10 mW	10 ns
RSN54H	23 mW	7.5 ns
RSN54L	1 mW	45 ns

description

Series RSN54, RSN54H, and RSN54L TTL integrated circuits are specifically designed and fabricated for operation and survivability in nuclear-radiation environments. The basic Series 54/74 configuration, desirable for its "natural" hardness, has been coupled with a state-of-the-art circuit-hardening process. This technology, compatible for use in high-volume production, employs:

- dielectric isolation
- thin-film resistors
- small transistor geometries
- shallow base diffusions
- heavy gold doping
- minimum collector thickness and resistivity
- aluminum interconnection system

Series RSN54, RSN54H, and RSN54L logic families are completely compatible with one another and with most other TTL and DTL circuits. These circuits are designed to operate at the same supply voltages and logic levels with the high d-c noise margins which are characteristic of Texas Instruments Series 54/74 circuits. These families of radiation-hardened circuits include the gates and flip-flops needed to perform functions within present-day digital electronic systems. And, since these three families are compatible with one another, selective use can be made of Series RSN54H high-speed circuits in system locations requiring minimal propagation delay time and of Series RSN54L circuits to minimize power dissipation. In other locations, Series RSN54 circuits may be used.

Series RSN54, RSN54H, and RSN54L are designed for operation over the full military temperature range of −55°C to 125°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

7

input-current requirements

Input-current requirements reflect worst-case conditions for $T_A = -55°C$ to $125°C$ and $V_{CC} = 4.5$ V to 5.5 V. Currents into the input terminals are specified as positive values. Arrows on the d-c test circuits indicate the actual direction of current flow.

Each input takes current into the input at a high voltage level. This is I_{IH}. For each emitter connected to an input, I_{IH} is a maximum of 40 μA for Series RSN54, 50 μA for Series RSN54H, and 10 μA for Series RSN54L.

Currents must flow out of the inputs to pull them to a low voltage level. This is I_{IL}. For each emitter connected to an input, I_{IL} is a maximum of -1.6 mA for Series RSN54, -2 mA for Series RSN54H, and -0.18 mA for Series RSN54L.

A normalized load for a family is an input for which maximum I_{IH} and I_{IL} are as defined above for single-emitter inputs.

drive capability

The maximum value of I_{OL} given under "recommended operating conditions" reflects the ability of an output to sink current from a number of loads at a low voltage level and maximum I_{OH} reflects the ability of the output to supply current at a high voltage level. Each output is capable of sinking current from or supplying current to 10 normalized loads within the same series. Alternatively, Series RSN54 will drive 8 RSN54H loads or 80 RSN54L loads. Series RSN54H will drive 12 RSN54 loads or 100 RSN54L loads. Series RSN54L will drive one RSN54H load or one RSN54 load plus two RSN54L loads.

The loads may be intermixed in any desired combination so long as the load totals for I_{IH} and I_{IL} are less than the maximum recommended values of I_{OH} and I_{OL}, respectively, for the driving circuit.

unused inputs

For optimum switching times and minimum noise susceptibility, unused inputs of AND or NAND gates should be maintained at a positive voltage greater than 2.4 V but not to exceed the absolute maximum rating of 5.5 V. This eliminates the distributed capacitance associated with the floating-input-transistor emitter, bond wire, and package lead, and ensures that no degradation will occur in the propagation delay times. Some possible ways of handling unused input emitters are:

a. Connect unused inputs to an independent supply voltage. Preferably this voltage should be between 2.4 V and 3.5 V.

b. Connect unused inputs to a used input if maximum drive capability of the driving output will not be exceeded. Each input presents a full load to the driving output at a high-level voltage but adds no loading at a low-level voltage.

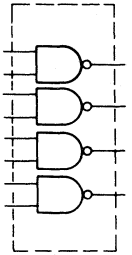
c. Connect unused inputs to V_{CC} through a 1-kΩ resistor so that if a transient which exceeds the 5.5-V maximum rating should occur, the impedance will be high enough to protect the input. One-to-25 unused inputs may be connected to each 1-kΩ resistor.

d. Connect unused inputs to any fixed-high-level compatible output such as the output of an inverter or NAND gate that has its input(s) grounded. Maximum high-level drive capability of the output should not be exceeded.

standard line summary

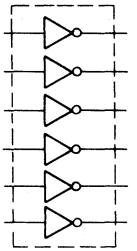
GATE CIRCUITS

RSN5400
RSN54H00
RSN54L00



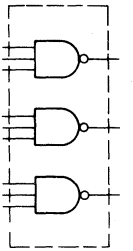
QUADRUPLE 2-INPUT
POSITIVE-NAND GATES

RSN5404
RSN54H04



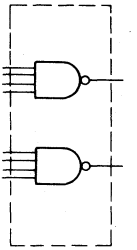
HEX INVERTERS

RSN5410
RSN54H10
RSN54L10



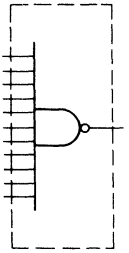
TRIPLE 3-INPUT
POSITIVE-NAND GATES

RSN5420
RSN54H20
RSN54L20



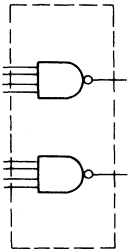
DUAL 4-INPUT
POSITIVE-NAND GATES

RSN5431
RSN54H31



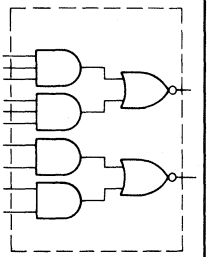
11-INPUT
POSITIVE-NAND GATES

RSN5440
RSN54H40



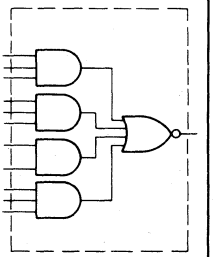
DUAL 4-INPUT
POSITIVE-NAND BUFFERS

RSN5456
RSN54H56



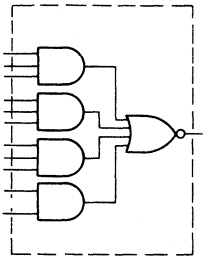
2-WIDE 3-INPUT
2-WIDE 2-INPUT, DUAL
AND-OR-INVERT GATES

RSN5457
RSN54H57



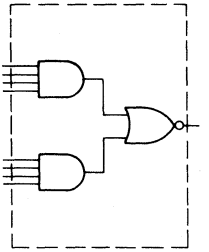
3-3-2-3 INPUT
AND-OR-INVERT GATES

RSN54L57



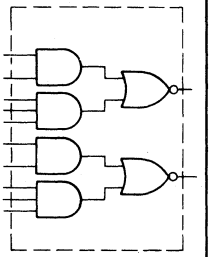
3-3-3-2 INPUT
AND-OR-INVERT GATE

RSN5458
RSN54H58



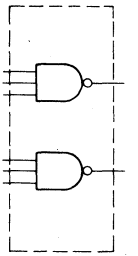
2-WIDE 4-INPUT
AND-OR-INVERT GATES

RSN54H66



DUAL 2-3 INPUT
AND-OR-INVERT GATE

RSN54L130



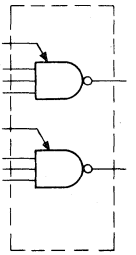
DUAL 3-INPUT
POSITIVE-NAND GATE

7

standard line summary (continued)

GATE CIRCUITS

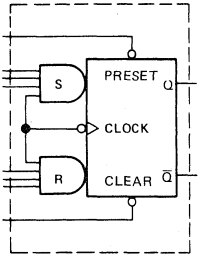
RSN54L131



DUAL EXPANDABLE 3-INPUT POSITIVE-NAND GATE

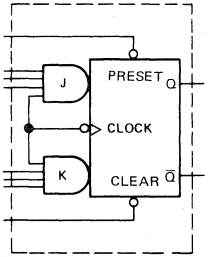
FLIP-FLOPS

RSN54L71



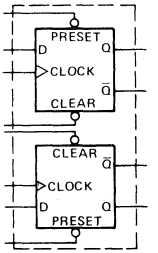
S-R MASTER-SLAVE FLIP-FLOP

RSN54L72



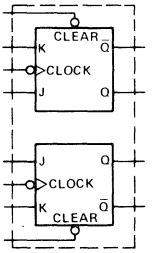
J-K MASTER-SLAVE FLIP-FLOP

RSN5474
RSN54H74
RSN54L74



DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

RSN54H103

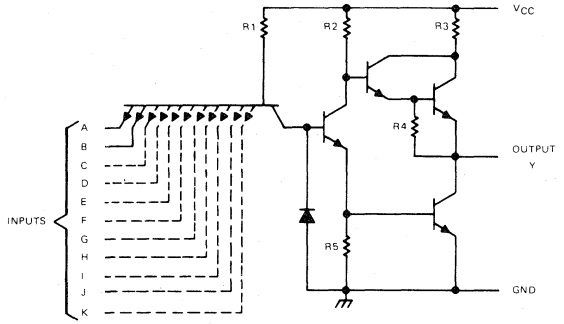


DUAL J-K EDGE-TRIGGERED FLIP-FLOP

MSI FUNCTION

RSN54H149 — 3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER See page 603

schematic (each NAND gate)



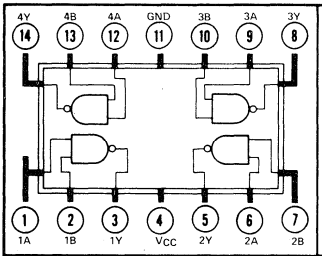
NOMINAL RESISTOR VALUES

RESISTOR	RSN5400 RSN5410 RSN5420 RSN5431	RSN54H00 RSN54H10 RSN54H20 RSN54H31
R1	4 kΩ	2.8 kΩ
R2	1.6 kΩ	760 Ω
R3	58 Ω	58 Ω
R4	1 kΩ	1 kΩ
R5	1 kΩ	470 Ω

logic

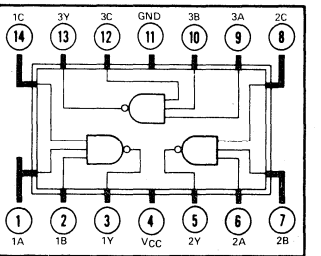
H FLAT PACKAGE (TOP VIEWS)

RSN5400, RSN54H00



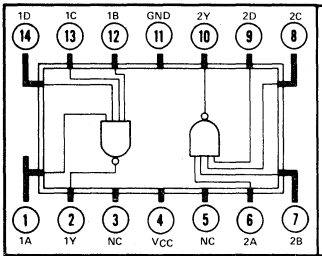
positive logic: $Y = \overline{AB}$

RSN5410, RSN54H10



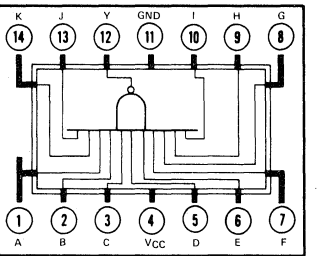
positive logic: $Y = \overline{ABC}$

RSN5420, RSN54H20



positive logic: $Y = \overline{ABCD}$

RSN5431, RSN54H31



positive logic: $Y = \overline{ABCDEFGHIJK}$

NC—No internal connection

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recommended operating conditions

	RSN5400 RSN5410 RSN5420 RSN5431			RSN54H00 RSN54H10 RSN54H20 RSN54H31			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5400 RSN5410 RSN5420 RSN5431		RSN54H00 RSN54H10 RSN54H20 RSN54H31		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1, 2		2		2		V
V_{IL}	Low-level input voltage	1, 2			0.8		0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
I_{OS}	Short-circuit output current‡	6	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output (average per gate)	7	V_{CC} = MAX, V_I = 0		1.75		2.5	mA
I_{CCL}	Supply current, low-level output (average per gate)	7	V_{CC} = MAX, V_I = 4.5 V		5.7		10.8	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

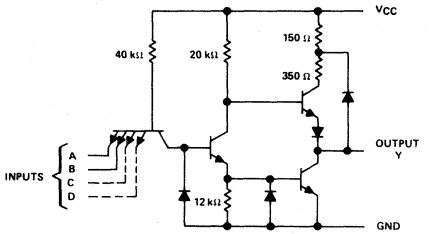
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	RSN5400 RSN5410 RSN5420		RSN5431		RSN54H00 RSN54H10 RSN54H20		RSN54H31		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 400 Ω for RSN54', R_L = 280 Ω for RSN54H', See Note 1		15		18		12		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18		25		12		20	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 148.

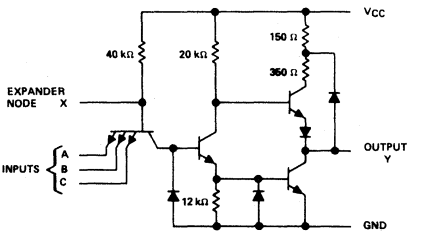
schematics (each gate)

RSN54L00, RSN54L10, RSN54L20, RSN54L130



Component values shown are nominal.

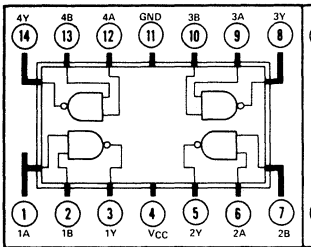
RSN54L131



logic

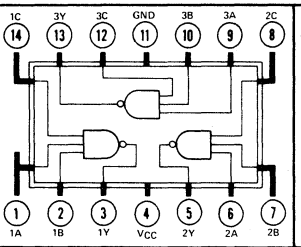
H FLAT PACKAGE (TOP VIEWS)

RSN54L00



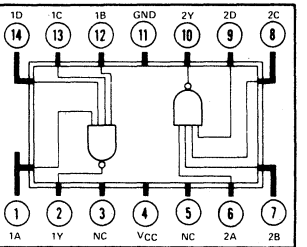
positive logic: $Y = \overline{AB}$

RSN54L10



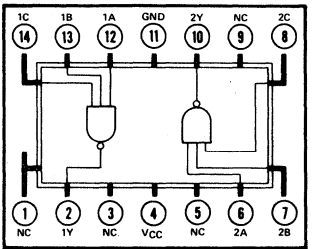
positive logic: $Y = \overline{ABC}$

RSN54L20



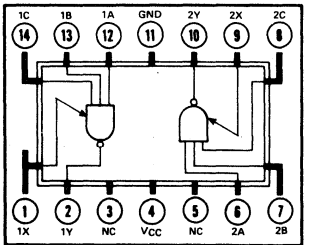
positive logic: $Y = \overline{ABCD}$

RSN54L130



positive logic: $Y = \overline{ABC}$

RSN54L131



positive logic: $Y = \overline{ABCX}$

NC—No internal connection

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−100	μA
Low-level output current, I_{OL}			2	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1, 2		1.9		V
V_{IL}	Low-level input voltage	1, 2			0.8	
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	6	V_{CC} = MAX	−1	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	7	V_{CC} = MAX, V_I = 0		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	7	V_{CC} = MAX, V_I = 4.5 V		0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

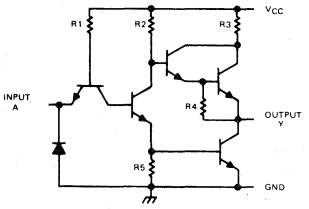
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Note 1		60	ns
t_{PLH}	Propagation delay time, high-to-low-level output			60	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 149.

7

schematic (each inverter)

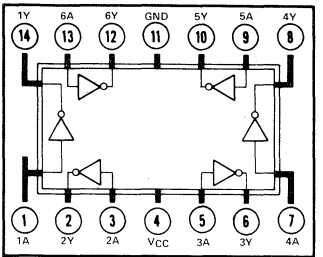


NOMINAL RESISTOR VALUES

RESISTOR	RSN5404	RSN54H04
R1	4 kΩ	2.8 kΩ
R2	1.6 kΩ	850 Ω
R3	58 Ω	58 Ω
R4	1 kΩ	1 kΩ
R5	1 kΩ	500 Ω

logic

H FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

recommended operating conditions

	RSN5404			RSN54H04			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5404		RSN54H04		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1, 2		2		2		V
V_{IL}	Low-level input voltage	1, 2			0.8		0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.4 V		40		50	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.4 V		−1.6		−2	mA
I_{OS}	Short-circuit output current‡	6	V_{CC} = MAX	−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output (average per inverter)	7	V_{CC} = MAX, V_I = 0		3.2		3.8	mA
I_{CCL}	Supply current, low-level output (average per inverter)	7	V_{CC} = MAX, V_I = 4.5 V		5.6		9.7	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	RSN5404		RSN54H04		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 400 Ω for RSN54', R_L = 280 Ω for RSN54H', See Note 1		15		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18		12	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 148.

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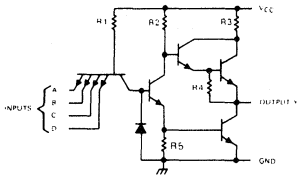
TYPES RSN5440, RSN54H40
DUAL 4-INPUT POSITIVE-NAND BUFFERS

schematic (each NAND buffer)

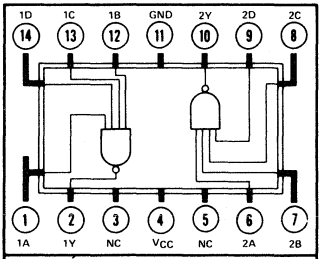


NOMINAL RESISTOR VALUES

RESISTOR	RSN5440	RSN54H40
R1	4 kΩ	1.4 kΩ
R2	600 Ω	316 Ω
R3	45 Ω	45 Ω
R4	1 kΩ	600 Ω
R5	400 Ω	200 Ω

logic

H FLAT PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

NC—No internal connection

recommended operating conditions

	RSN5440			RSN54H40			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}			−1.5			−3	mA
Low-level output current, I_{OL}			48			60	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†	RSN5440		RSN54H40		UNIT
				MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1, 2		2		2		V
V_{IL}	Low-level input voltage	1, 2			0.8		0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{OL} = 0.8 V, I_{OH} = MAX	2.4		2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{OH} = 2 V, I_{OL} = MAX		0.4		0.4	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V		1		1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.4 V		50		100	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.4 V		−1.6		−4	mA
I_{OS}	Short-circuit output current‡	6	V_{CC} = MAX	−40	−125	−40	−125	mA
I_{CCH}	Supply current, high-level output (average per gate)	7	V_{CC} = MAX, V_I = 0		1.75		5	mA
I_{CCL}	Supply current, low-level output (average per gate)	7	V_{CC} = MAX, V_I = 4.5 V		12.6		27	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡Not more than one output should be shorted at a time, and the duration of the short-circuit test should not exceed one second.

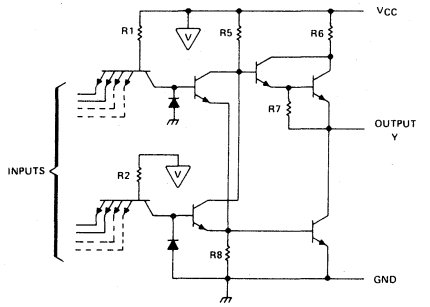
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	RSN5440		RSN54H40		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 400 Ω for RSN54', R_L = 280 Ω for RSN54H', See Note 1		15		12	ns
t_{PHL}	Propagation delay time, high-to-low-level output			18		12	ns

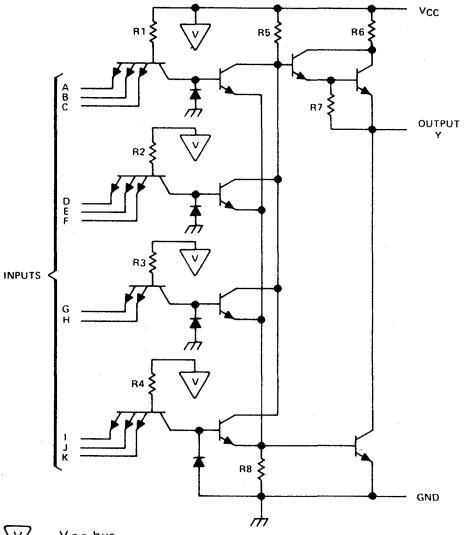
NOTE 1: Load circuit and voltage waveforms are shown on page 148.

schematics

RSN5456, RSN5458,
RSN54H56, RSN54H58, RSN54H66



RSN5457, RSN54H57



V . . . V_{CC} bus

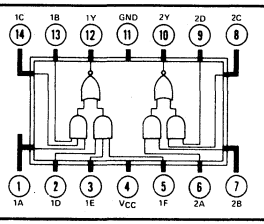
NOMINAL RESISTOR VALUES

RESISTOR	RSN5456 RSN5457 RSN5458	RSN54H56 RSN54H57 RSN54H58 RSN54H66
R1, R2, R3, R4,	4 kΩ	2.8 kΩ
R5	1.6 kΩ	760 Ω
R6	58 Ω	58 Ω
R7	1 kΩ	1 kΩ
R8	1 kΩ	470 Ω

logic

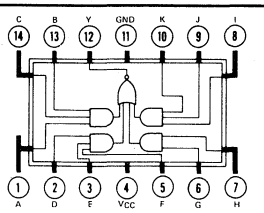
H FLAT PACKAGE (TOP VIEW)

RSN5456, RSN54H56



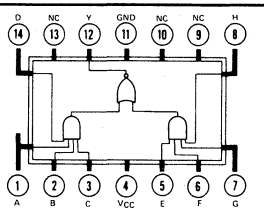
positive logic: $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

RSN5457, RSN54H57



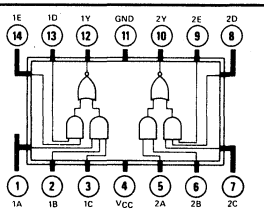
positive logic: $Y = \overline{(ABC) + (DEF) + (GH) + (IJK)}$

RSN5458, RSN54H58



positive logic: $Y = \overline{(ABCD) + (EFGH)}$

RSN54H66



positive logic: $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1\overline{E})}$
$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D \cdot 2\overline{E})}$

NC—No internal connection

7

recommended operating conditions

	SERIES RSN54			SERIES RSN54H			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}			−400			−500	μA
Low-level output current, I_{OL}			16			20	mA
Operating free-air temperature, T_A	−55		125	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SERIES RSN54		SERIES RSN54H		UNIT
					MIN	MAX	MIN	MAX	
V_{IH}	High-level input voltage	1, 2			2		2		V
V_{IL}	Low-level input voltage	1, 2				0.8		0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = MAX		2.4		2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = MAX			0.4		0.4	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V			1		1	mA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.4 V			40		50	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.4 V			−1.6		−2	mA
I_{OS}	Short-circuit output current‡	6	V_{CC} = MAX		−40	−120	−40	−120	mA
I_{CCH}	Supply current, high-level output	7	V_{CC} = MAX, V_I = 0	'56		7			mA
				'57		7			
				'58		3.5			
				'H56, 'H66				10	
				'H57				10	
				'H58				5	
I_{CCL}	Supply current, low-level output	7	V_{CC} = MAX, V_I = 4.5 V	'56		14			mA
				'57		10			
				'58		7			
				'H56, 'H66				25	
				'H57				16	
				'H58				13	

7

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

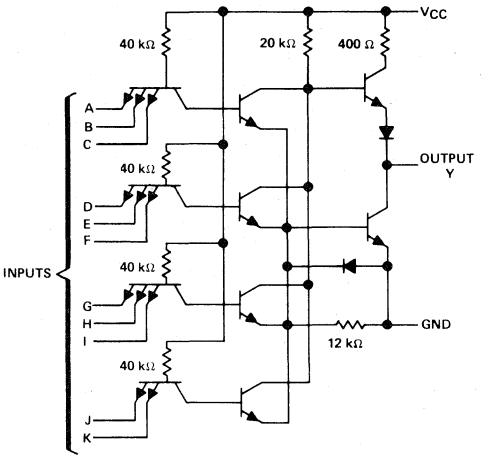
‡Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

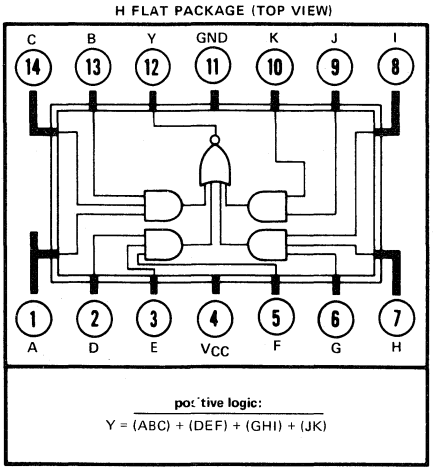
PARAMETER		TEST CONDITIONS	SERIES RSN54		SERIES RSN54H		UNIT
			MIN	MAX	MIN	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 400 Ω for RSN54', R_L = 280 Ω for RSN54H', See Note 1		20		15	ns
t_{PHL}	Propagation delay time high-to-low-level output			15		12	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 148.

schematic



logic



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−100	μA
Low-level output current, I_{OL}			2	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage	1, 2		1.9		V
V_{IL}	Low-level input voltage	1, 2			0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, I_{IH} = 1.9 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	4	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	4	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	5	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current	6	V_{CC} = MAX	−1	−15	mA
I_{CCH}	Supply current, high-level output	7	V_{CC} = MAX, V_I = 0		0.8	mA
I_{CCL}	Supply current, low-level output	7	V_{CC} = MAX, V_I = 4.5 V		0.99	mA

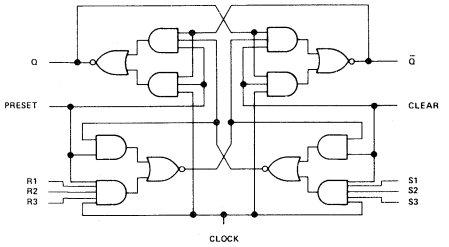
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Note 1		90	ns
t_{PHL}	Propagation delay time, high-to-low-level output			60	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 149.

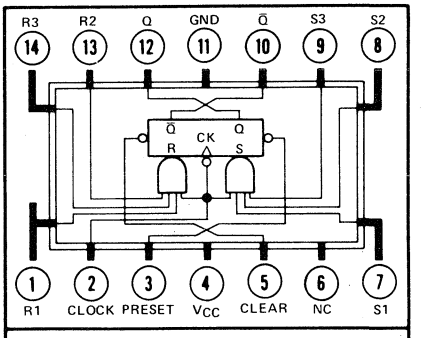
TYPE RSN54L71
S-R MASTER-SLAVE FLIP-FLOP

functional block diagram



logic

H FLAT PACKAGE (TOP VIEW)



positive logic: see function table

NC—No internal connection

description

These S-R flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

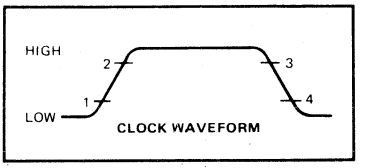
1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	S	R	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	INDETERMINATE	

R = R1·R2·R3
S = S1·S2·S3
H = high level (steady state)
L = low level (steady state)
X = irrelevant
⎍ = high-level pulse; R and S inputs should be held constant while clock is high.
Q_0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



7

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−100	μA
Low-level output current, I_{OL}			2	mA
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Setup time, t_{setup}	0↑			ns
Hold time, t_{hold}	0↓			ns
Operating free-air temperature, T_A	−55		125	°C

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage			1.9		V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any S or R	V_{CC} = MAX, V_I = 5.5 V		100	μA
		Preset, clear, or clock			200	
I_{IH}	High-level input current	Any S or R	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset, clear, or clock			20	
I_{IL}	Low-level input current	Any S or R	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Preset, clear, or clock			−0.4	
I_{OS}	Short-circuit output current		V_{CC} = MAX	−1	−15	mA
I_{CC}	Supply current		V_{CC} = MAX		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

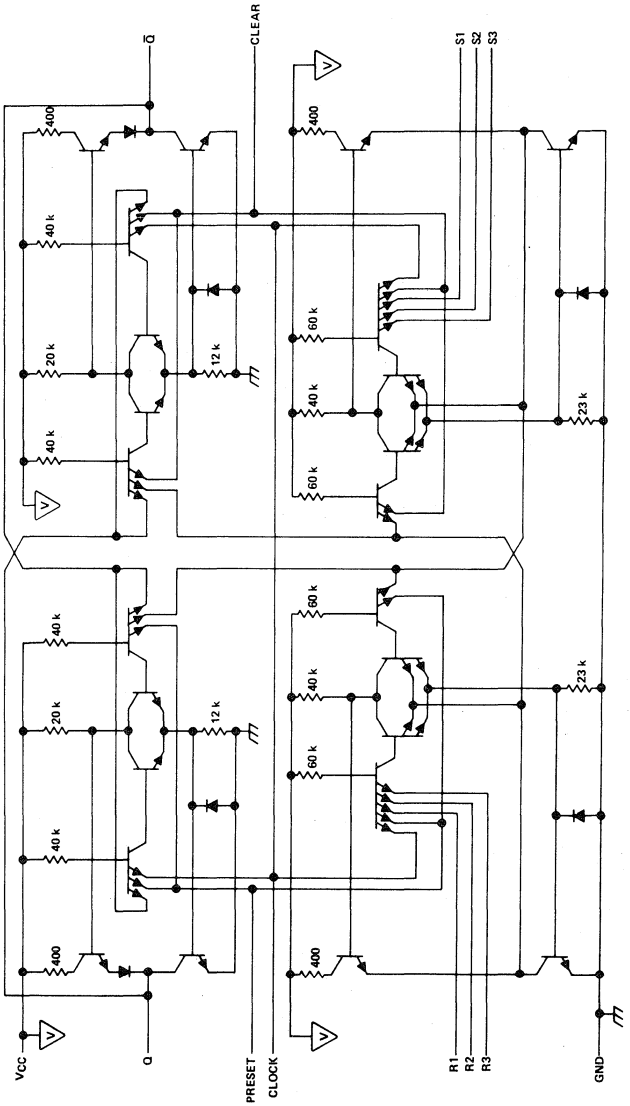
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 4 kΩ, See Note 1		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear				75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear				150	
t_{PLH}	Propagation delay time, low-to-high-level output from clock		10		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		10		150	

NOTE 1: Load circuit and voltage waveforms are shown on page 149.

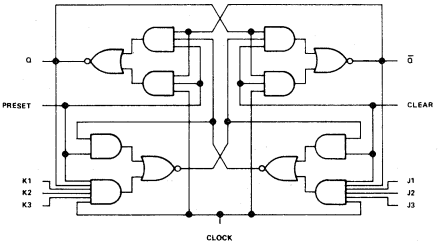
7

schematic



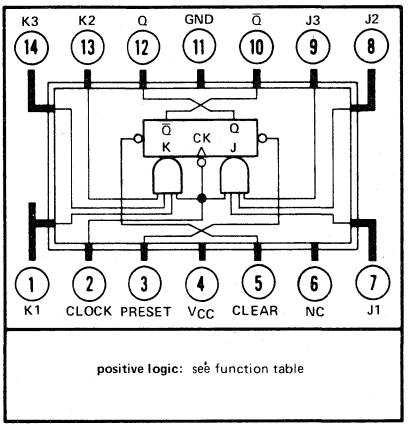
▽ . . . V_{CC} bus
Resistor values shown are nominal and in ohms.

functional block diagram



logic

H FLAT PACKAGE (TOP VIEW)



NC—No internal connection

description

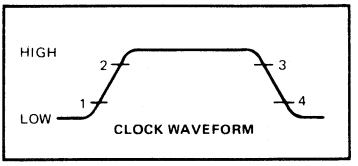
These J-K flip-flops are based on the master-slave principle. The AND-OR gate inputs for entry into the master section are controlled by the clock pulse. The clock pulse also regulates the circuitry which connects the master and slave sections. The sequence of operation is as follows:

1. Isolate slave from master
2. Enter information from AND gate inputs to master
3. Disable AND-OR gate inputs
4. Transfer information from master to slave

FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\bar{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	TOGGLE	

J = J1·J2·J3; K = K1·K2·K3
H = high level (steady state), L = low level (steady state)
X = irrelevant
⎍ = high-level pulse; J and K inputs should be held constant while clock is high.
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level after each clock pulse.
*This configuration is nonstable; that it, it will not persist when preset and clear inputs return to their inactive (high) level.



recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−100	μA
Low-level output current, I_{OL}			2	mA
Width of clock pulse, $t_{w(clock)}$	200			ns
Width of preset pulse, $t_{w(preset)}$	100			ns
Width of clear pulse, $t_{w(clear)}$	100			ns
Setup time, t_{setup}	0↑			ns
Hold time, t_{hold}	0↓			ns
Operating free-air temperature, T_A	−55		125	°C

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage			1.9		V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 1.9 V, V_{IL} = 0.8 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any J or K	V_{CC} = MAX, V_I = 5.5 V		100	μA
		Preset, clear, or clock			200	
I_{IH}	High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset, clear, or clock			20	
I_{IL}	Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Preset, clear, or clock			−0.4	
I_{OS}	Short-circuit output current		V_{CC} = MAX	−1	−15	mA
I_{CC}	Supply current		V_{CC} = MAX		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

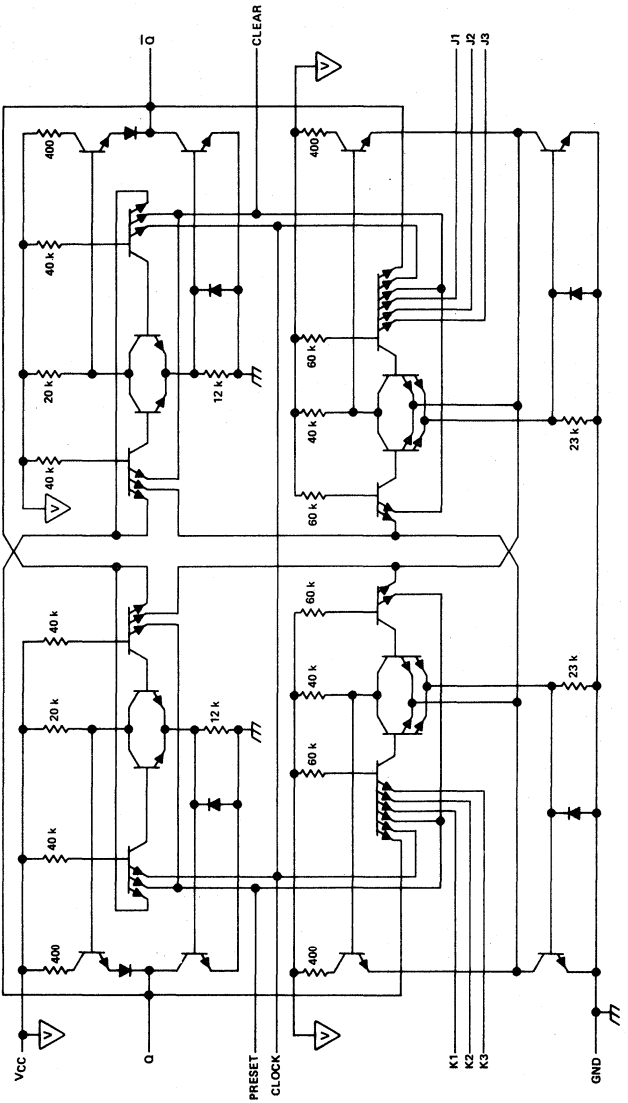
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 4 kΩ, See Note 1		3		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from preset or clear				75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from preset or clear				150	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		10		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		10		150	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 149.

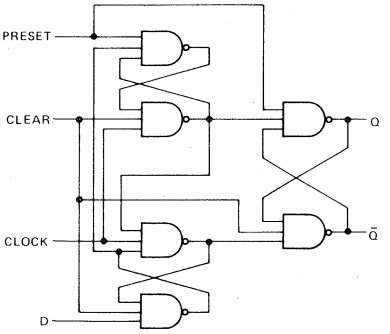
7

schematic


IO
CLEAR
J1
J2
J3
400
40 k
20 k
12 k
40 k
60 k
40 k
60 k
23 k
VCC
Q
PRESET
CLOCK
K1
K2
K3
GND
. . . VCC bus
Resistor values shown are nominal and in ohms.

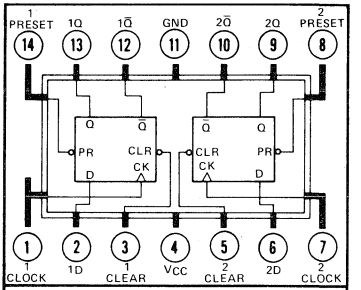
TYPES RSN5474, RSN54H74, RSN54L74
DUAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

functional block diagram (each flip-flop)



logic

H FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These monolithic, high-speed, dual, edge-triggered flip-flops utilize TTL circuitry to perform D-type flip-flop logic. Each flip-flop has individual clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

recommended operating conditions

	RSN5474			RSN54H74			RSN54L74			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
High-level output current, I_{OH}			−400			−500			−100	μA
Low-level output current, I_{OL}			16			20			2	mA
Clock frequency, f_{clock}	0		20	0		30	0		1	MHz
Width of clock pulse, $t_{w(clock)}$	30			20			200			ns
Width of preset pulse $t_{w(preset)}$	30			20			100			ns
Width of clear pulse, $t_{w(clear)}$	30			20			100			ns
Setup time, t_{setup}	20↑			15↑			30↑			ns
Hold time, t_{hold}	5↑			0↑			0↑			ns
Operating free-air temperature T_A	−55		125	−55		125	−55		125	°C

↑The arrow indicates that the rising edge of the clock pulse is used for reference.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		RSN5474 MIN	RSN5474 MAX	RSN54H74 MIN	RSN54H74 MAX	RSN54L74 MIN	RSN54L74 MAX	UNIT
V_{IH}	High-level input voltage				2		2		1.9		V
V_{IL}	Low-level input voltage					0.8		0.8		0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = V_{IH} min,	I_{OH} = MAX, V_{IL} = 0.8 V	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = V_{IH} min,	I_{OL} = MAX, V_{IL} = 0.8 V		0.4		0.4		0.3	V
I_I	Input current at maximum input voltage	D input	V_{CC} = MAX,	V_I = 5.5 V		1		1		0.1	mA
		Preset or clock				1		1		0.2	
		Clear				1		1		0.3	
I_{IH}	High-level input current	D input	V_{CC} = MAX,	V_I = 2.4 V		40		50		10	μA
		Preset or clock				80		100		20	
		Clear				120		150		30	
I_{IL}	Low-level input current	Preset or D	V_{CC} = MAX	V_I = 0.3 V						−0.18	mA
				V_I = 0.4 V		−1.6		−2			
		Clock or clear		V_I = 0.3 V						−0.36	
				V_I = 0.4 V		−3.2		−4			
I_{OS}	Short-circuit output current‡		V_{CC} = MAX		−40	−120	−40	−120	−1	−15	mA
I_{CC}	Supply current		V_{CC} = 5 V			28		45		3	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡For '54 and 'H74, not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	RSN5474 MIN	RSN5474 MAX	RSN54H74 MIN	RSN54H74 MAX	RSN54L74 MIN	RSN54L74 MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 400 Ω for RSN54', R_L = 280 Ω for RSN54H', R_L = 4 kΩ for RSN54L', See Note 1	20		30		1		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			25		20		75	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			35		30		150	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			25		20		100	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			30		25		150	ns

NOTE 1: Load circuit and waveforms are shown on pages 148 and 149.

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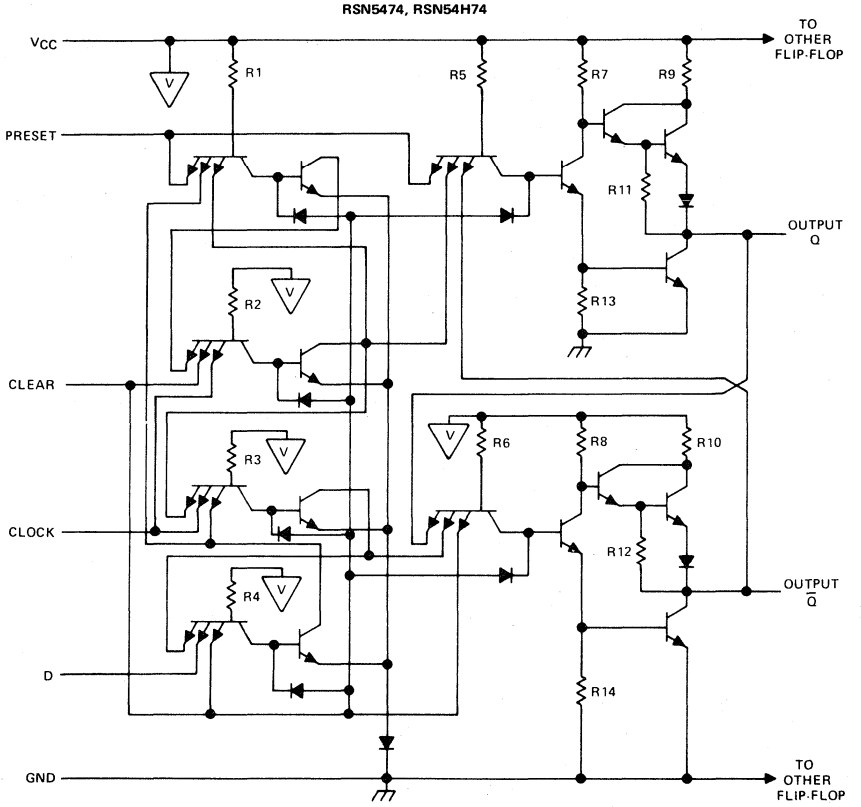
schematic (each flip-flop)



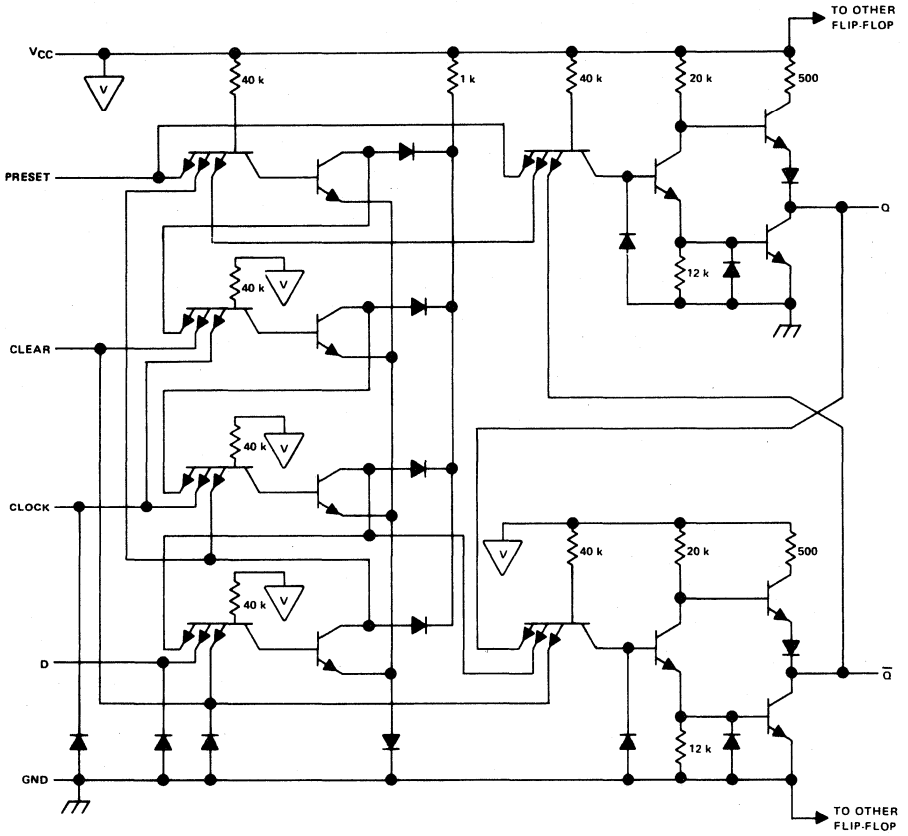
V . . . V_{CC} bus

NOMINAL RESISTOR VALUES

RESISTOR	RSN5474	RSN54H74
R1,R2,R3,R4,R5,R6	4 kΩ	2.8 kΩ
R7,R8,	1.6 kΩ	760 Ω
R9,R10	58 Ω	58 Ω
R11,R12	1 kΩ	1 kΩ
R13,R14	1 kΩ	470 Ω

schematic (each flip-flop)

RSN54L74



V . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

TYPE RSN54H103
DUAL J-K EDGE-TRIGGERED FLIP-FLOP

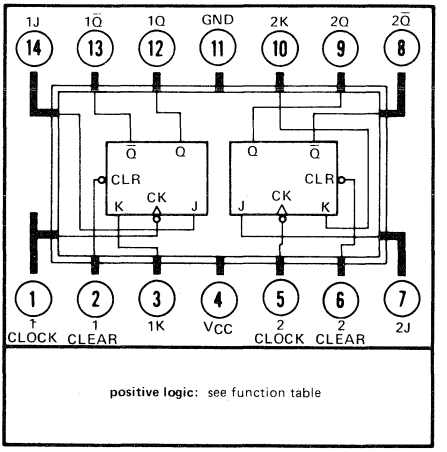
logic

FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady state), L = low level (steady state)
X = irrelevant
↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each input changes to the complement of its previous level on each ↓ transition of the clock.

H FLAT PACKAGE (TOP VIEW)



positive logic: see function table

description

These monolithic J-K flip-flops are negative-edge-triggered. The inputs are inhibited while the clock input is low. When the clock goes high, the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change when the clock input is high and the function table will be observed as long as the minimum setup times are maintained. Input data is transferred to the outputs on the negative edge of the clock pulse. A low input to clear resets Q to the low logic level independently of the clock.

recommended operating conditions

		RSN54H103			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level output current, I_{OH}				−500	μA
Low-level output current, I_{OL}				20	mA
Clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$		15			ns
Width of clear pulse, $t_{w(clear)}$		15			ns
Setup time, t_{setup}	High-level data	10↓			ns
	Low-level data	15↓			
Hold time, t_{hold}		0↓			ns
High-to-low-level transition time of clock pulse, $t_{THL(clock)}$				150	ns
Operating free-air-temperature, T_A		−55		125	°C

↓The arrow indicates that the falling edge of the clock pulse is used for reference.

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electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS†	RSN54H103 MIN	RSN54H103 MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V	2.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = MAX, V_{IH} = 2 V, V_{IL} = 0.8 V		0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V		1	mA
I_{IH}	High-level input current	J or K input	V_{CC} = MAX, V_I = 2.4 V		50	µA
		Clock or clear			100	
I_{IL}	Low-level input current	J or K input	V_{CC} = MAX, V_I = 0.4 V		−2	mA
		Clock or clear			−4	
I_{OS}	Short-circuit output current‡		V_{CC} = MAX	−40	−100	mA
I_{CC}	Supply current		V_{CC} = MAX		52	mA

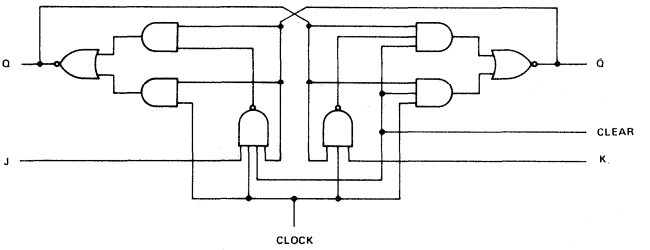
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second. Only the $\overline{Q}$ outputs are tested.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

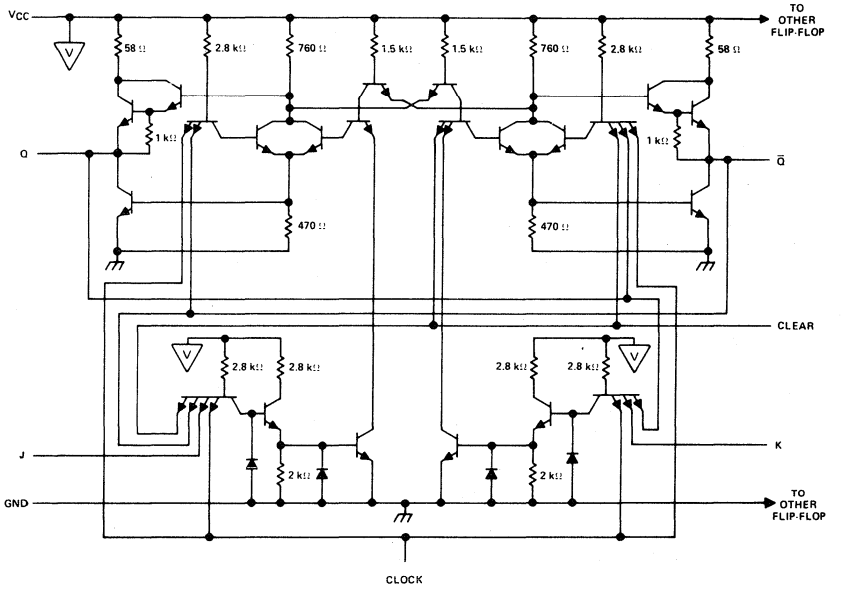
PARAMETER		TEST CONDITIONS	RSN54H103 MIN	RSN54H103 MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 50 pF, R_L = 280 Ω, See Note 1	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear to $\overline{Q}$			15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear to Q			15	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			15	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			15	ns

NOTE 1: Load circuit and voltage waveforms are shown on page 148.

functional block diagram (each flip-flop)



schematic (each flip-flop)



▽ . . . V_{CC} bus
Resistor values shown are nominal.

TEXAS INSTRUMENTS

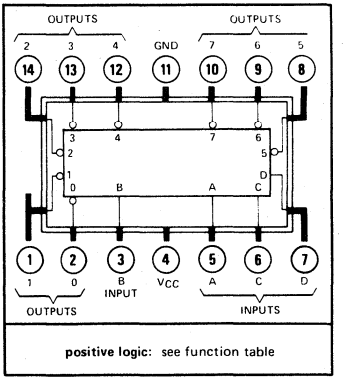
TYPE RSN54H149
3-LINE-TO-8-LINE DECODER/DEMULTIPLEXER

BULLETIN NO. DL-S 7211867, DECEMBER 1972

TTL INTEGRATED CIRCUITS WITH HIGH TOLERANCE TO GAMMA AND NEUTRON IRRADIATION

- **High Speed: Maximum Propagation Delay Time . . . 20 ns**
- **Fully Compatible with Most TTL and DTL Circuits**
- **For Applications as:**
  - **3-Line-to-8-Line Decoder with Strobe**
  - **4-Line-to-16-Line Decoder (Uses Two 'H149's)**
  - **1-Line-to-8-Line Demultiplexer**

H FLAT PACKAGE (TOP VIEW)



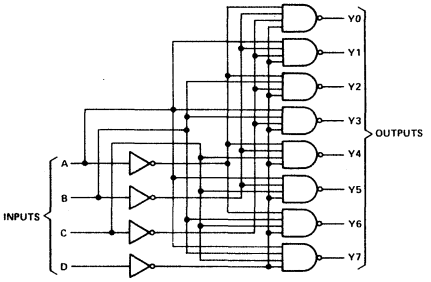
positive logic: see function table

description

This monolithic 3-line-to-8-line decoder is designed and fabricated for operation and survivability in nuclear-radiation environments with the same supply voltage, logic levels, and high d-c noise margins as standard Series 54/74 and Series 54H/74H circuits.

The RSN54H149 may be used as a 3-line-to-8-line decoder with the D input used as a strobe (low level to enable, high level to disable). Two of these decoders may be utilized to perform 4-line-to-16-line decoding when connected as shown in Figure A of this data sheet. The demultiplexing function is performed by using the A, B, and C inputs to address the output line and entering data at the D input. The RSN54H149 is characterized for operation over the full military temperature range of −55°C to 125°C.

functional block diagram



FUNCTION TABLE

INPUTS				OUTPUTS							
D	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	H	H	H	H	H	L	H	H
L	H	H	L	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	L
H	L	L	L	H	H	H	H	H	H	H	H
H	L	L	H	H	H	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−500	μA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.8	V
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −500 μA	2.4		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 20 mA		0.4	V
I_I	Input current at maximum input voltage	A, B, or C input	V_{CC} = 5.5 V, V_I = 5.5 V		5	mA
		D input			1	
I_{IH}	High-level input current	A, B, or C input	V_{CC} = 5.5 V, V_I = 2.4 V		250	μA
		D input			50	
I_{IL}	Low-level input current	A, B, or C input	V_{CC} = 5.5 V, V_I = 0.4 V		−10	mA
		D input			−2	
I_{OS}	Short-circuit output current†		V_{CC} = 5.5 V	−40	−125	mA
I_{CC}	Supply current		V_{CC} = 5.5 V, See Note 3		60	mA

†Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed one second.
NOTE 3: I_{CC} is measured with A, B, and C at 4.5 V, D grounded, and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 280 Ω, See Note 4		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	

NOTE 4: Load circuit and voltage waveforms are shown on page 148.

TYPICAL APPLICATION DATA

Figure A shows a method for utilizing two RSN54H149 decoders to perform 4-wire-to-16-wire (1-of-16) decoding. Input D is applied to one decoder and its inverse is applied to the other thus enabling the first decoder for binary inputs 0 through 7 and the other decoder for binary inputs 8 through 15.

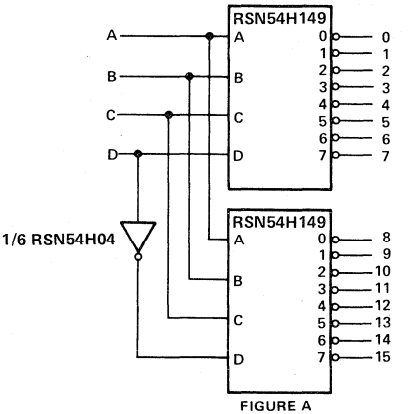


FIGURE A

38510/MACH IV

High Reliability Microelectronics Procurement Specifications

MIL-STD-883

CONTENTS

38510/MACH IV PROGRAM

The Texas Instruments 38510/MACH IV Program includes a complete procurement document encompassing general specification MIL-M-38510 and MIL-STD-883. The 38510/MACH IV Program is a realistic cost-effective supplement to JAN, offering 38510/883 screening for those device types not yet covered by JAN specifications or those JAN circuits without adequate availability. The 38510/MACH IV Program device types may be cross-referenced to JAN circuit types, class, package and finish codes on pages 638 through 640. The 38510/MACH IV Program places major emphasis on designing and building quality and reliability into the device, realizing that no specification or screening procedure can substitute for inherent reliability. It is realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure ("infant mortality"). The 38510/MACH IV screening will eliminate these early failures and serve to demonstrate with a high degree of statistical confidence that the required levels of quality and reliability have in fact been built into the device. The program is backed up by factory and distributor stocking programs on standard 38510/MACH IV Class B (SNC) devices, allowing quick delivery on most popular device types.

The 38510/MACH IV Program establishes the following reliability screening levels.

CLASS	NUMBER	ESTIMATED FAILURE RATE
Class C	SNM54XX	0.010 – 0.020% per 1000 hours
Industrial Hi Rel	SNA54XX	0.007 – 0.020% per 1000 hours
Class B	SNC54XX	0.004 – 0.008% per 1000 hours
Class A	SNH54XX	0.002 – 0.005% per 1000 hours

Each reliability screening level is tested to the following method of MIL-STD-883 test methods and procedures.

TEST METHOD	CLASS C SNM	INDUSTRIAL HI-REL SNA	CLASS B SNC	CLASS A SNH
Precap Visual, 2010	Cond B	TI Defined	Cond B	NASA Class A
Stab. Bake, 1008	100%	100%	100%	100%
Temp. Cycle, 1010	100%	100%	100%	100%
Centrifuge, 2001	100%	100%	100%	100%
Fine Leak, 1014	100%	Sample	100%	100%
Gross Leak, 2001	100%	Sample	100%	100%
Burn-In, 1015	——	168 hours	168 hours	240 hours
Mech Shock, 2002	——	——	——	100%
Thermal Shock, 1011	——	——	——	100%
X-Ray, 2021	——	——	——	100%

The 38510/MACH IV Program also offers an aid to specification writing by providing a base 38510 and 883 document, whereby special device program specifications may be written invoking any additional testing options unique to a specific program. The 38510/MACH IV specification is organized and written per MIL-STD-100 to allow its use as a program specification by merely adding the user's company name and drawing number, as well as any required additions or deletions necessary to meet the specific program goals.

38510/MACH IV PROGRAM

1.0 SCOPE

1.1 This specification establishes standards for materials, workmanship, performance capabilities, identification and processing of high-reliability bipolar monolithic integrated circuits.

1.2 Intent

The intent of this document is such as to recognize that quality and reliability are *built* into, not *tested* into, a product. There is no specification or screening procedure that can substitute for inherent, built-in reliability. However, it must be realized that irrespective of lot quality, there will always be some small percentage of devices that are subject to early failure (infant mortality). A well engineered screening procedure will eliminate most, if not all, of these early failures. Secondly, the screening and acceptance testing described herein will also serve to demonstrate, with a high degree of statistical confidence, that the required levels of quality and reliability have, in fact, been built into the product.

2.0 APPLICABLE DOCUMENTS

2.1 The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein:

2.2 Specifications

Military/NASA

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	Microcircuits devices, general specification for
NASA 85M03766	Microcircuit, Monolithic Silicon TTL Family of Devices, Specification Control Drawing for

2.3 Standards

Military/NASA

MIL-STD-105	Sampling Procedures and Tables for Inspection by Attributes
MIL-STD-883	Test Methods and Procedures for Microelectronics
MIL-STD-790	Reliability Assurance Program for Electronic Parts Specification
MIL-STD-1276	Leads, Weldable, for Electronic Components Parts
MIL-STD-1313	Microelectronics Terms and Definitions
MSFC-STD-355	Radiographic Inspection Standard for Electronic Parts

Detail Specifications

SNXXXX	Detail Specification for a Particular Part Type (e.g., Manufacturer's Data Sheet)

2.4 Precedence of Documents

For the purpose of interpretation, in case of any conflicts, the following order of precedence shall apply:

a)	Purchase Order	—The purchase order shall have precedence over any referenced specification.
b)	Detail Specification	—The detail specification shall have precedence over this specification and other referenced specifications.
c)	This Specification	—This specification shall have precedence over all referenced specifications.
d)	Referenced Specifications	—Referenced Specifications shall apply to the extent specified herein.

2.5 Federal and/or military specifications and standards required shall be obtained from the usual government sources.

3.0 GENERAL REQUIREMENTS

The individual item requirements shall be as specified herein and in accordance with the applicable detail specification. In the event of any conflict between the requirements of this specification and the detail specification, the latter shall govern. The static and dynamic electrical performance requirements of the integrated circuits plus absolute maximum ratings and test methods shall be as specified in the detail specifications.

3.1.1 Definitions

a)	LTPD	Lot Tolerance Percent Defective shall be as defined by MIL-M-38510.
b)	λ	Lambda, stated in percent per 1000 hours as defined by MIL-M-38510.
c)	MRN	Minimum reject number as defined by MIL-M-38510.
d)	Production Lot	For the purpose of this specification, a production lot shall be defined per MIL-M-38510.
e)	Inspection Lot	An inspection lot shall be as defined in MIL-M-38510.
f)	C	Acceptance number as defined by MIL-M-38510.

3.1.2 Terms and Definitions

Terms and definitions shall be as defined in MIL-STD-1313.

3.1.3 Classification of Requirements

The requirements for the integrated circuits are classified herein as follows:

Requirement	Paragraph
Process Conditioning, Testing and Screening	3.2
Qualification	3.3
Design and Construction	3.4

8

3.2 Process Conditioning, Testing and Screening

Four levels of screening and quality assurance for integrated circuits are provided for in this specification. Process conditioning, testing and screening shall be as specified in 4.3 and the applicable figure for the appropriate quality assurance level stated on the purchase order and defined as follows:

Screening Level	Part Number Prefix	Applicable Process Flow Chart
38510/883A	SNH (Level IV)	Figure 4
38510/883B	SNC (Level III)	Figure 3
38510/883C	SNM (Level I)	Figure 1
Industrial High Reliability	SNA (Level II)	Figure 2

3.3 Qualification

Vendor qualification for delivery of integrated circuits to this specification shall be as specified in paragraph 4.2.

3.4 Design and Construction

Integrated circuit design and construction shall be in accordance with the requirements specified herein and in the applicable detail specification.

3.4.1 Topography

Integrated circuits furnished under this specification shall have topography information available for review by procuring activity. The information made available shall provide sufficient data for thorough circuit design, application, performance, and failure analysis studies.

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3.4.1.1 Monolithic Die Topography

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the topography of elements formed on the silicon monolithic die shall be available for review. This shall be identified with the specific detail integrated circuit part-type in which it is used and the applicable detail specification.

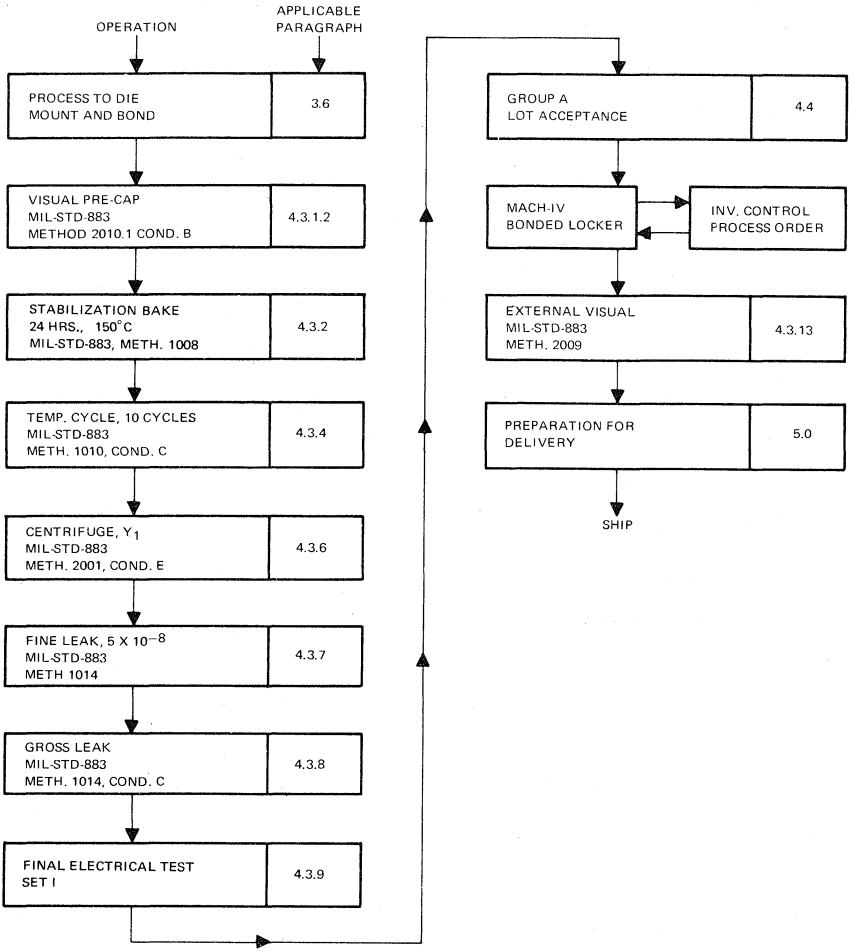
OPERATION
APPLICABLE PARAGRAPH
PROCESS TO DIE MOUNT AND BOND
3.6
VISUAL PRE-CAP MIL-STD-883 METHOD 2010.1 COND. B
4.3.1.2
STABILIZATION BAKE 24 HRS., 150°C MIL-STD-883, METH. 1008
4.3.2
TEMP. CYCLE, 10 CYCLES MIL-STD-883 METH. 1010, COND. C
4.3.4
CENTRIFUGE, Y_1 MIL-STD-883 METH. 2001, COND. E
4.3.6
FINE LEAK, 5×10^{-8} MIL-STD-883 METH 1014
4.3.7
GROSS LEAK MIL-STD-883 METH. 1014, COND. C
4.3.8
FINAL ELECTRICAL TEST SET I
4.3.9
GROUP A LOT ACCEPTANCE
4.4
MACH-IV BONDED LOCKER
INV. CONTROL PROCESS ORDER
EXTERNAL VISUAL MIL-STD-883 METH. 2009
4.3.13
PREPARATION FOR DELIVERY
5.0
SHIP

FIGURE 1

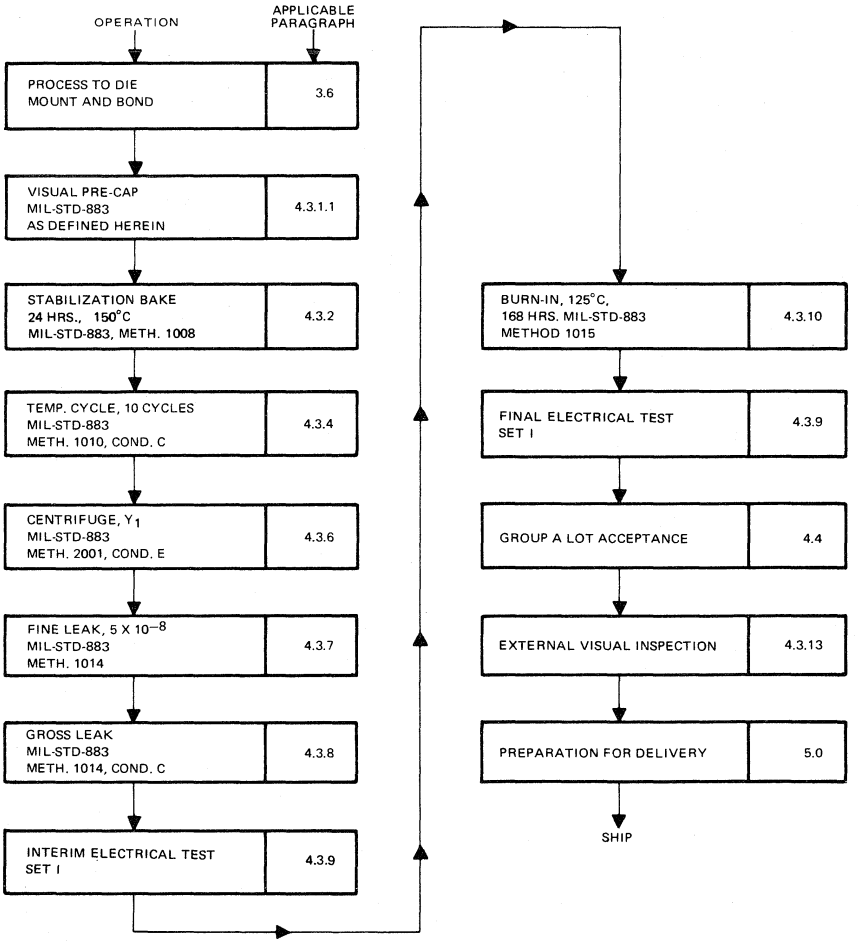
OPERATION
APPLICABLE PARAGRAPH
PROCESS TO DIE MOUNT AND BOND
3.6
VISUAL PRE-CAP MIL-STD-883 AS DEFINED HEREIN
4.3.1.1
STABILIZATION BAKE 24 HRS., 150°C MIL-STD-883, METH. 1008
4.3.2
TEMP. CYCLE, 10 CYCLES MIL-STD-883 METH. 1010, COND. C
4.3.4
CENTRIFUGE, Y_1 MIL-STD-883 METH. 2001, COND. E
4.3.6
FINE LEAK, 5×10^{-8} MIL-STD-883 METH. 1014
4.3.7
GROSS LEAK MIL-STD-883 METH. 1014, COND. C
4.3.8
INTERIM ELECTRICAL TEST SET I
4.3.9
BURN-IN, 125°C, 168 HRS. MIL-STD-883 METHOD 1015
4.3.10
FINAL ELECTRICAL TEST SET I
4.3.9
GROUP A LOT ACCEPTANCE
4.4
EXTERNAL VISUAL INSPECTION
4.3.13
PREPARATION FOR DELIVERY
5.0
SHIP

FIGURE 2

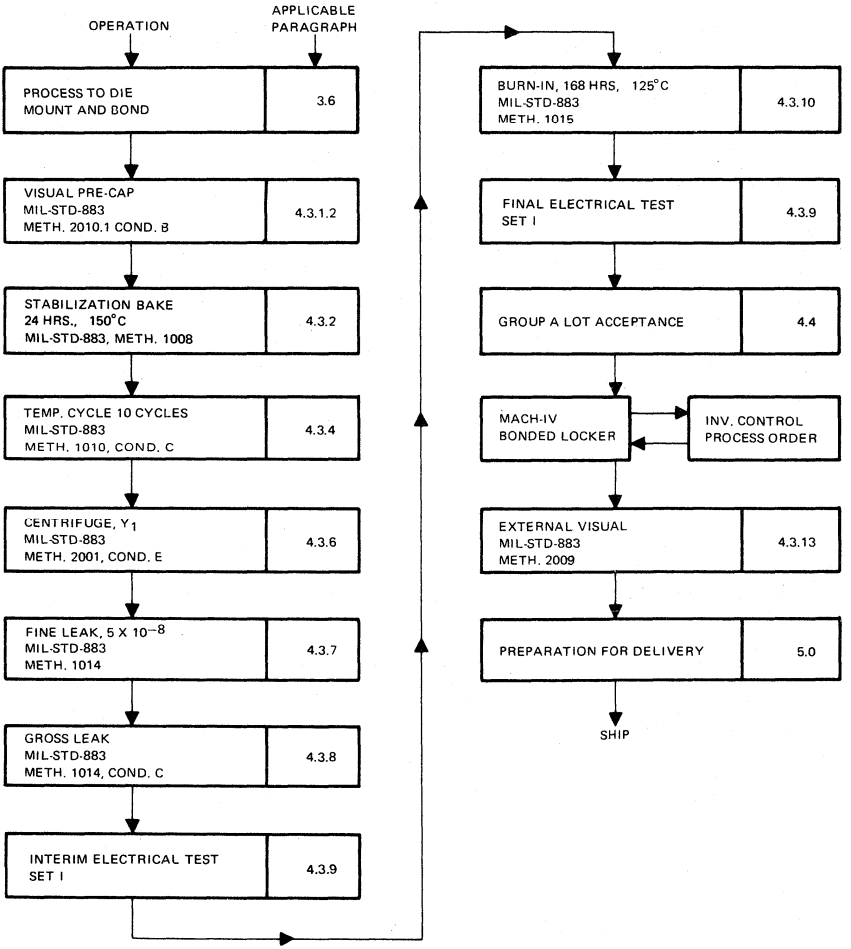
OPERATION
APPLICABLE PARAGRAPH
PROCESS TO DIE MOUNT AND BOND
3.6
VISUAL PRE-CAP MIL-STD-883 METH. 2010.1 COND. B
4.3.1.2
STABILIZATION BAKE 24 HRS., 150°C MIL-STD-883, METH. 1008
4.3.2
TEMP. CYCLE 10 CYCLES MIL-STD-883 METH. 1010, COND. C
4.3.4
CENTRIFUGE, Y_1 MIL-STD-883 METH. 2001, COND. E
4.3.6
FINE LEAK, 5×10^{-8} MIL-STD-883 METH. 1014
4.3.7
GROSS LEAK MIL-STD-883 METH. 1014, COND. C
4.3.8
INTERIM ELECTRICAL TEST SET I
4.3.9
BURN-IN, 168 HRS, 125°C MIL-STD-883 METH. 1015
4.3.10
FINAL ELECTRICAL TEST SET I
4.3.9
GROUP A LOT ACCEPTANCE
4.4
MACH-IV BONDED LOCKER
INV. CONTROL PROCESS ORDER
EXTERNAL VISUAL MIL-STD-883 METH. 2009
4.3.13
PREPARATION FOR DELIVERY
5.0
SHIP

FIGURE 3

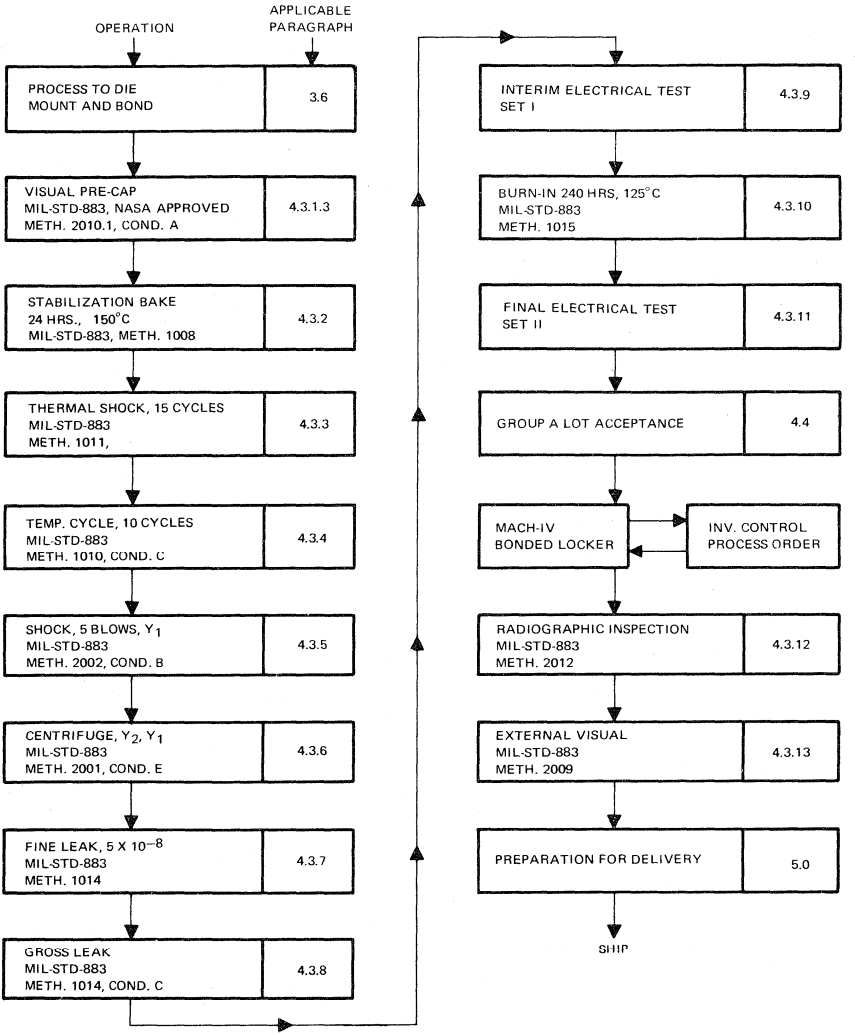
OPERATION
APPLICABLE PARAGRAPH
PROCESS TO DIE MOUNT AND BOND
3.6
VISUAL PRE-CAP MIL-STD-883, NASA APPROVED METH. 2010.1, COND. A
4.3.1.3
STABILIZATION BAKE 24 HRS., 150°C MIL-STD-883, METH. 1008
4.3.2
THERMAL SHOCK, 15 CYCLES MIL-STD-883 METH. 1011,
4.3.3
TEMP. CYCLE, 10 CYCLES MIL-STD-883 METH. 1010, COND. C
4.3.4
SHOCK, 5 BLOWS, Y_1 MIL-STD-883 METH. 2002, COND. B
4.3.5
CENTRIFUGE, Y_2, Y_1 MIL-STD-883 METH. 2001, COND. E
4.3.6
FINE LEAK, 5 X 10^{-8} MIL-STD-883 METH. 1014
4.3.7
GROSS LEAK MIL-STD-883 METH. 1014, COND. C
4.3.8
INTERIM ELECTRICAL TEST SET I
4.3.9
BURN-IN 240 HRS, 125°C MIL-STD-883 METH. 1015
4.3.10
FINAL ELECTRICAL TEST SET II
4.3.11
GROUP A LOT ACCEPTANCE
4.4
MACH-IV BONDED LOCKER
INV. CONTROL PROCESS ORDER
RADIOGRAPHIC INSPECTION MIL-STD-883 METH. 2012
4.3.12
EXTERNAL VISUAL MIL-STD-883 METH. 2009
4.3.13
PREPARATION FOR DELIVERY
5.0
SHIP

FIGURE 4

3.4.1.2 Die Intraconnection Pattern

An enlarged photograph or drawing (to scale) with a minimum magnification of 80 times the die (chip) size showing the specific intraconnection pattern utilized to intraconnect the elements in the circuit. This shall be in the same scale as the die topography 3.4.1.1 so that the elements utilized and those not being used can easily be determined.

3.4.2 Materials

Materials shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit other immediate or latent defects that adversely affect storage, operation or environmental capabilities of integrated circuits.

3.4.2.1 Material Selection

Materials selected for use in the construction of the integrated circuits shall be chosen for maximum suitability for the application. This shall include consideration of the best balance for:

a) Electrical performance

b) Thermal compatibility and conductivity

c) Chemical stability including resistance to deleterious interactions with other materials

d) Metallurgical stability with respect to adjacent materials and change in crystal configuration

e) Maximum stability with regard to continued uniform performance through the specified environmental conditions and life.

3.4.2.2 Foreign Materials

No lacquer, grease, paste, desiccant or other similar foreign encapsulant or coating material shall be included in the circuit enclosure nor applied to any part of the internal circuit assembly.

3.4.3 Mechanical

3.4.3.1 Case

Each integrated circuit shall be securely mounted and hermetically sealed within a case designed and constructed to conform to the outline and physical dimensions shown in the detailed specification. External surfaces of the integrated circuit case shall be unpainted except for markings.

3.4.3.2 Interconnections

Interconnections within the integrated circuit case shall be minimized and there shall be no wire crossovers. Circuit intraconnections by means of wire jumpers shall not be used. (See Note 6.2)

3.4.3.3 Leads

Lead material, construction, and outline shall be as specified on the detail specification and shall be capable of meeting the solderability test of MIL-STD-883, Method 2003. (See note 6.4).

3.4.3.3.1 Lead Size

Lead outline and dimensions shall be as specified in the detail specification.

3.4.3.3.2 Lead Surface Condition

Leads shall be free of the following defects over their entire length when inspected under a minimum of 4X magnification:

a) Foreign materials adhering to the leads such as paint, film, deposits and dust. Where adherence of such foreign materials is in question, leads may be subjected to a clean, contaminant-free (e.g., oil, dust, etc.), filtered air stream (suction or expulsion) of 88 feet per second maximum, or a wash/rinse as necessary and reinspected.

b) Nicks, cuts, scratches or other surface defacing defects which expose the base metal.

3.4.3.3.3 Lead Straightness

Leads shall be aligned within a 0.050-inch diameter, 0.050-inch length cylinder concentric to the point of lead emergence from the case and the X-axis (the axis parallel to the lead axis). Along the remaining lead length, there shall be no unspecified bend whose radius is less than 0.10 inch and no twist whose angle is greater than 30° (ribbon leads, only).

3.4.3.3.4 Preformed Leads

Preformed leads, when specified, shall be in accordance with the detail specification. The part number of the integrated circuit shall remain as specified in the applicable detail specification or purchase order, the applicable suffix designation shall appear on the purchase order but shall not be marked on the device.

3.4.3.3.5 Carriers (Mech-Pak Carrier)

Carrier-matrix assemblies consisting of individually mounted integrated circuits shall be furnished when so specified by purchase order. The individual carriers shall have provisions for use with automatic test equipment contacts. Devices supplied "clipped-out" of the Mech-Pak Carrier shall be supplied in the Barnes Carrier type 029-188 or equivalent. (Applicable to Flat Packs only.)

3.5 Marking of Integrated Circuits

3.5.1 Legibility

All marking shall be permanent in nature and remain legible when subjected to specified operating, storage, and environmental requirements. All markings shall be insoluble in standard solvents such as trichlorethylene, water and xylene.

3.5.2 Marking Details

Marking of the integrated circuits shall be located as follows unless otherwise specified in the detail specification:

a) TO-99, TO-100, and similar "can" cases shall be marked on the top of the case. Where space limitations exist, the side of the case may be used.

b) Flat Packs shall be marked on the top of the case. Where space limitation exists, the bottom of the package may be utilized as necessary. As a minimum the top of the package shall show the manufacturer's identification mark or symbol, the device part number, date code, and pin 1 orientation mark (where applicable).

c) Dual-in-line plug-in packages shall be marked in the same manner as flat packs.

3.5.3 Required Device Marking

a) Index point indicating the starting point for numbering of leads shall be as indicated in the detail specification. The indexing point may be a tab, color dot, or other suitable indicator.

b) Manufacturer's identification mark or symbol.

c) An alpha-numeric lot date code indicating the week of initial submission for screening or inspection. The date code shall be as follows:

1) EIA four-digit date code, the first two numbers shall be the last two digits of the year, the last two numbers shall indicate the calendar week.

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2) A Gothic letter which identifies separate lots of the same device type processed within the same calendar week. (If no more than one lot is processed through screening or inspection in a given calendar week, the Gothic letter may be omitted.)

d) Manufacturer's part number defining circuit type and applicable MACH IV screening level and MIL-M-38510 product assurance level as defined in paragraph 3.2.

e) Individual device serial number (if required)

f) A dot to indicate acceptance by Radiographic inspection

NOTE:

When a color dot is used to identify pin one, the radiographic inspection acceptance dot shall be placed on the bottom of the package.

3.6 Product Assurance

The manufacturer shall establish and maintain a reliability assurance program that complies with the basic intent of MIL-STD-790. Furthermore, it is intended that each integrated circuit delivered shall be free of any defect in design, material, manufacturing process, testing and handling, which would degrade or otherwise limit its performance when used within the specified limits.

3.6.1 Visual and Mechanical Examination

Integrated circuits shall be examined to verify that material, design, construction, physical dimensions, marking and workmanship are in accordance with the specified acceptance criteria.

3.6.2 Test Equipment

The manufacturer shall prepare and maintain a current list, by name and drawing number or other unique identification, of test equipment used in the manufacturing and testing of devices submitted for acceptance inspection under this specification. This list shall be made available to the procuring activity representative upon request.

3.6.3 Process Controls

Each integrated circuit shall be constructed by manufacturing processes which are under the surveillance of the manufacturer's Quality Control department. The processes shall be monitored and controlled by use of statistical techniques in accordance with published specifications and procedures. The manufacturer shall prepare and maintain suitable documentation (such as quality control manuals, inspection instructions, control charts, etc.) covering all phases of incoming part and material inspection and in-process inspections required to assure that product quality meets the requirements of this specification. The

procuring activity may verify, with the permission of and in the company of the manufacturer's designated representative, that suitable documentation exists and is being applied. Information designated as proprietary by the manufacturer will be made available to the procuring activity or its representative only with the written permission of the manufacturer.

Process control is recognized as being vital to the concept of "built-in" quality. Appendix A defines an acceptable process-control system. Devices delivered to this specification shall be manufactured in a controlled system similar to that set forth in Appendix A. The process control program shall include a scanning electron microscope (SEM) monitor program for evaluating the metal integrity over oxide step and oxide step contour. The SEM analysis will be defined in a Quality & Reliability Assurance document.

3.6.4 Production Changes

The manufacturer shall advise the procuring activity of the time at which any major change(s) in production or QC methods or documentation become effective during the period of device production for delivery against any given purchase order referencing this specification.

3.7 Workmanship

Integrated circuits shall be manufactured and processed in a careful and workmanlike manner, in accordance with the production processes, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the reliability assurance program established by paragraph 3.6.

3.7.1 Personnel Certification

The manufacturer shall be responsible for training, testing and certification of personnel involved in producing integrated circuits. Training shall be commensurate and consistent with the requirements of this specification and in conformance to the basic intent of MIL-STD-790. Training aids in the form of satisfactory criteria shall be available for operator and inspector review at any time.

3.7.2 Personnel Evaluation

The supplier shall maintain a continuous evaluation of the proficiency of personnel concerned with production and inspection. Retraining of an operator or inspector shall be required when this evaluation establishes that a degree of proficiency necessary to meet the requirements of this specificaiton is not being exercised.

3.7.3 Rework Provisions

3.7.3.1 Rework

All rework on micorcircuits manufactured under this specification shall be accomplished in accordance with paragraph 3.7.1 of MIL-M-38510 as defined herein.

3.7.3.2 Rebonding

Rebonding shall be in accordance with MIL-M-38510, with the total number of rebond attempts per microcircuit limited to a maximum of 10 percent of the total number of bonds in the microcircuit. The 10 percent limit on rebonds may be interpreted as the nearest whole number to the 10 percent value. A bond shall be defined as a wire to post or wire to pad bond (i.e., for a 14-lead wire-bonded package there are 28 bonds). Bond-offs required to clear the bonder after an unsuccessful first bond attempt need not be considered as rebonds provided they can be identified as bond-offs by being made physically off the plated post or if they contain a non-typical number of wedge marks. The initial bond attempt need not be visible. A replacement of one wire bonded at one end of an unsuccessful bond attempt at one end of the wire counts as one rebond; a replacement of a wire bonded at both ends counts as two rebonds. A ball bond on top of a ball bond is not permissible. No more than one rebond attempt shall be permitted at any pad or post and no rebonds shall be made where pad metallization has been lifted.

3.8 Performance Capabilities

The integrated circuits delivered to this specification shall be designed to be capable of meeting the environmental requirements specified in Table II. The manufacturer need not perform these tests specifically for the contract or specification, but shall provide data which demonstrates the ability of the integrated circuits to pass the environmental tests. The data shall have been generated on devices from the same generic family as the circuits being supplied to this specification, and the package configuration shall be the same as for the delivered parts (i.e., Flat Pack, TO-100, etc.).

3.9 Quality and Reliability Assurance Program Plan

The manufacturer shall establish and implement a Quality and Reliability Assurance Program Plan that meets the intent of MIL-M-38510, Appendix A. Submission of the program plan to the procuring activity shall not be a requirement of this specification, however, the program plan shall be maintained by the manufacturer and shall be available for review by the procuring activity.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection

Unless otherwise specified in the contract or purchase order, the manufacturer is responsible for the performance of all inspection requirements specified herein. Except as otherwise specified, the manufacturer may utilize his own facilities or any commercial laboratory acceptable to the procuring activity. The procuring activity may, at its discretion, perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements.

4.1.1 Inspection and Testing Procedures Coverage

Inspection and testing processes and procedures prepared in fulfillment of the reliability assurance program established per paragraph 3.6 shall be prescribed by clear, complete and current instructions. These instructions shall assure inspection and test of materials, work in process and completed integrated circuits as required by this specification. In addition, criteria for approval and rejection of materials and integrated circuits shall be included.

4.1.2 Inspection at Point of Delivery

The procuring activity may, at its discretion, reinspect any or all of the delivered parts. (Excluding Group B destructive samples as defined by MIL-STD-883). All parts, found to be defective and/or lacking specified documentation (such as test documentation) may be returned to the manufacturer at the manufacturer's expense.

4.1.3 Inspection Records

The manufacturer shall maintain a reliability data and records library. This library shall have on file, for review by the procuring activity, records of examination, qualification test results, variables data (when required) and all other pertinent data generated on devices manufactured to this specification.

4.1.4 Control of Procurement Sources

The manufacturer shall be responsible for assuring that all supplies and services conform to this specification, the detail specification and the manufacturer's procurement requirements.

4.1.4.1 Manufacturer's Receiving Inspection

Purchased supplies shall be subjected to inspection after receipt as necessary to ensure conformance to contract requirements. In selecting sampling plans, consideration shall be given to the controls exercised by the procurement source and evidence of sustained quality conformance.

4.1.4.2 The manufacturer shall provide procedures for withholding from use all incoming supplies pending completion of required tests or receipt of necessary certification or test records and their evaluation.

4.1.4.3 The manufacturer shall initiate corrective action with the procurement source depending upon the nature and frequency of receipt of nonconforming supplies.

4.1.5 Procuring Activity Quality Assurance Representative

The procuring activity, may, at its discretion, place quality assurance representatives in the manufacturer's plant as deemed necessary to assure conformance to contract requirements in any non-proprietary phase of design, fabrication, processing, inspection, testing, and reliability of the integrated circuits being produced. The manufacturer shall provide reasonable facilities and assistance for the safety and convenience of such personnel in the performance of their duties. Inspection and test procedures shall be made available for review by the quality assurance representative.

4.2 Qualification and Quality Conformance Inspection

4.2.1 Qualification

Manufacturer's qualification shall be based on compliance with the established reliability test program requirements of paragraph 4.2.1.1 herein. The manufacturer may, at his discretion, substitute the qualification test plan of paragraph 4.2.1.2 in order to establish initial qualification. However, the substitution of paragraph 4.2.1.2 does not relieve the manufacturer from the responsibility of establishing an in-house reliability evaluation program as defined by paragraph 4.2.1.1.

4.2.1.1 Established Reliability Test Program

The manufacturer shall have an established and well defined in-house reliability program. This program shall be so designed as to demonstrate that the manufacturer's product is capable of meeting, as a minimum, the environmental and minimum life requirements listed in Table I herein. The reliability program may be modeled after the test procedure of Table I or it may take the form of a step-stress testing program similar to that defined by

MIL-STD-883, Method 5006. The program shall be on-going in nature; that is, at specified intervals the manufacturer shall randomly select product that is representative of current production techniques, and subject the devices to the specified tests. Sampling shall be done on each generic family.

4.2.1.2 Qualification Test Program

In lieu of meeting the requirements of 4.2.1.1, the manufacturer may establish qualification by performing an initial, one-time qualification test in accordance with Table I herein. Qualification testing shall be performed on each generic family supplied to this specification. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 calendar months. Continued qualification shall then be based on compliance with the requirements of paragraph 4.2.1.1.

4.2.1.3 Procedures and Definitions

4.2.1.3.1 Sampling Procedure

Device selection for the qualification procedure of 4.2.1.1 or 4.2.1.2 shall be based on a random sampling technique. Linear sample shall be obtained from one generic family. Digital testing shall be done on a mixture of device types that adequately represent the entire generic family. The following is a recommended mix ratio:

Gates	:	65% of total sample
Flip-Flops	:	25% of total sample
MSI	:	10% of total sample

4.2.1.3.2 Generic Family

Electrically and structurally similar devices shall be said to comprise a generic family (e.g., TTL) if they meet the following criteria:

a) Are designed with the same basic circuit-element configuration such as TTL, DTL, ECL, or Linear, and differ only in the number or complexity of specified circuits which they contain.

b) Are designed for the same supply, bias and signal voltage, and for input/output capability with each other under an established set of loading rules.

c) Are enclosed in housings (packages) of the same basic construction (e.g., hermetically sealed flat packages, dual-in-line ceramic, dual-in-line plastic) and outline, differing only in the number of active housing terminals included and/or utilized.

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4.2.2 Quality Conformance Inspection (Groups B and C per Table II)

a) When specifically called out and funded on the purchase order or contract, the manufacturer shall perform the quality conformance inspections (Group B and/or Group C) on a lot-by-lot basis.

b) When specifically called out and funded on the purchase order or contract, the manufacturer shall provide quality conformance inspection and generic data from the previous quarterly test results.

4.2.2.1 Lot Acceptance Sampling

Statistical sampling for quality conformance inspections shall be in accordance with MIL-M-38510 Table B1.

Group B samples except bond strength samples shall be selected from sublots that have successfuliy completed all of the 100% processing steps specified on the applicable process flow chart.

4.2.2.2 Resubmission of Failed Lots

When any lot submitted for quality conformance inspection fails any subgroup requirement, it may be resubmitted a maximum of one time for that particular subgroup. One additional submission is permitted, provided an analysis is performed to determine the failure mechanism for each reject device in the subgroup, and that it is determined that the failures are due to one of the following:

a) Testing error resulting in electrical damage to devices

b) A defect that can effectively be removed by rescreening the lot

c) Random defects which do not reflect poor basic device designs or poor workmanship.

4.2.2.3 Early Shipments

When quality conformance inspection is being performed for a specific contract or purchase order, the accepted Group A devices that are awaiting shipment pending successful completion of Group B and/or Group C, shall be stored in the 38510/MACH IV bonded locker. Under no circumstances shall such parts be shipped prior to the successful completion of the Group B tests.

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4.2.2.4 Groups B and C Test Data

All lot-by-lot data generated by Group B and/or Group C testing shall accompany the initial shipment of devices. This data shall consist, at a minimum, of the following:

a) Attributes data for Group B. Endpoints for the subgroups are visual per the applicable MIL-STD-883 test method.

b) Attributes data for Group C subgroups 1, 2, 4 and 5. Endpoints for these subgroups shall be "critical electrical parameters" only.

4.2.2.5 Procedure in Case of Test Equipment Failure or Operator Error

Where an integrated circuit is believed to have failed as a result of faulty test equipment or operator error, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid. If it is determined that the failure is invalid, a replacement integrated circuit from the same inspection lot may be added to the sample. The replacement integrated circuit shall be subjected to all those tests to which the discarded integrated circuit was submitted prior to its failure, and any remaining specified test to which the discarded integrated circuit was not subjected prior to its failure.

4.3 Quality Assurance Processing, Methods and Procedures

This section establishes the test methods and conditions to be used for the 100% processing (screening) requirements specified by the applicable process flow chart.

4.3.1 Precap Visual Inspection

Each microcircuit shall be required to pass the appropriate precap visual inspection defined as follows. Precap Lot Acceptance shall be per paragraph 4.6.

4.3.1.1 Level II devices shall be visually inspected in accordance with the criteria listed in Section 6.1.2 of this specification. Inspection procedures and equipment requirements shall be as defined in MIL-STD-883.

4.3.1.2 38510C (Level I) and 38510B (Level III) devices shall be visually inspected in accordance with MIL-STD-883, Method 2010.1, Condition B (See Note 6.1.1).

4.3.1.3 38510A (Level IV) devices (designated for NASA type applications) shall be visually inspected in accordance with the NASA approved precap requirements of NASA specification 85MO3766 for digital circuits (Revision B applies for moly gold).

4.3.1.4 Complex MSI and LSI circuits as defined in Table III will be precap inspected per paragraph 6.1.2 in lieu of precap 2010.1, Condition A, paragraph 4.3.1.3, and 2010.1, Condition B, paragraph 4.3.1.2.

4.3.2 Stabilization Bake

The purpose of this test is to determine the effect on microelectronic devices of baking at elevated temperatures without electrical stress applied. Test shall be performed in accordance with MIL-STD-883, Method 1008, Condition C.

4.3.3 Thermal Shock

The purpose of this test is to determine the resistance of the device to sudden exposure to extreme changes in temperature. Test shall be performed in accordance with MIL-STD-883, Method 1011, Condition A.

4.3.4 Temperature Cycle

This test is conducted for the purpose of determining the resistance of a part to exposures at extremes of high and low temperatures, and to the effect of alternate exposures to these extremes, such as would be experienced when equipment or parts are transferred to and from heated shelters in arctic areas. Test shall be performed in accordance with MIL-STD-883, Method 1010, Condition C, minimum of 10 cycles.

4.3.5 Mechanical Shock

The shock test is intended to determine the suitability of the devices for use in electronic equipment which may be subjected to moderate severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Test shall be performed in accordance with MIL-STD-883, Method 2002, Condition B, five blows minimum.

4.3.6 Centrifuge (Constant Acceleration)

The centrifuge test is used to determine the effects on microelectronics devices of a centrifugal force. This test is designed to indicate structural and mechanical weaknesses not necessarily detected in shock and vibration tests. Test shall be performed in accordance with MIL-STD-883, Method 2001, Condition E.

4.3.7 Fine Leak Test

Each integrated circuit for 38510C (Level I), 38510B (Level III), and 38510A (Level IV) screens shall be subject to a fine leak test in accordance with paragraph 4.3.7.1 or 4.3.7.2. The method shall be optional providing it is consistent with and capable of detecting the specified leak rate of the applicable process flow chart. Level II devices will be sample tested to a 1% AQL.

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4.3.7.1 Helium Leak Test

Helium leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition A. Helium bomb pressure shall be 30 psig maximum, bomb time shall be 4 hours minimum.

4.3.7.2 Radiflo Leak Test

Radiflo leak test shall be performed in accordance with MIL-STD-883, Method 1014, Condition B. Krypton 85 bomb pressure and dwell time are a function of the radioactivity level and shall be selected so as to conform to the equations given in Condition B.

4.3.8 Gross-Leak Test

Each integrated circuit for 38510C (Level I), 38510B (Level III), and 38510A (Level IV) screens shall be subjected to the appropriate gross-leak test of paragraphs 4.3.8.1 or 4.3.8.2 or an approved equivalent. The manufacturer may, at his option, perform gross-leak testing after the Set I Electrical Tests of paragraph 4.3.9. Level II devices will be sample tested to a 1% AQL.

4.3.8.1 When specifically called out and funded on the purchase order or contract, units will be bombed 4 hours minimum at 30 psi in FC-78. Units will then be immersed in FC-40 or equivalent at +125°C ± 5°C for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles, MIL-STD-883, Method 1014, Condition C, Step 2.

4.3.8.2 Units will be immersed in FC-40 or equivalent at +125°C ± 5°C for 20 seconds minimum and observed for one large bubble or a continuous stream of small bubbles, MIL-STD-883, Method 1014, Condition C, Step 1.

4.3.9 Final Electrical Test (Set I)

Each integrated circuit shall be required to pass the electrical requirements of Subgroup 1 of the detail specification. The manufacturer shall also perform such additional testing necessary to assure the parts will meet the temperature extreme limits.

When specifically called out and funded on the purchase order or contract, the manufacturer shall perform subgroups 2, 3, and 4 of paragraph 4.4 in accordance with Method 5004 of MIL-STD-883, Notice 3.

4.3.10 Burn-In

The burn-in screen is performed for the purpose of eliminating marginal devices and early-life failures evidenced as time and stress dependent. Test shall be in accordance with MIL-STD-883, Method 1015, Condition A, D, or E at 125 ± 5°C for digital circuits and Conditions A, B, C, or D for linear circuits. The bias shall be removed from the devices prior to their return to 25°C. (See note 6.3)

4.3.11 Final Electrical Test (Set II)

Each integrated circuit shall be required to pass the electrical requirements of the detail specifications. The following tests shall be performed as a minimum. DC at maximum and minimum rated temperatures, and switching parameters at 25°C.

The manufacturer may, when deemed necessary, elect to perform additional electrical testing over and above the requirements stated herein.

4.3.12 Radiographic Inspection (X-ray)

Test shall be performed in accordance with MIL-STD-883, Method 2012, the integrated circuit shall be required to pass a radiographic inspection to these requirements. In addition, the acceptance criteria shall meet, as a minimum, the requirements of NASA MSFC specification MSFC-STD-355.

4.3.13 External Visual Inspection

The purpose of this examination is to verify that materials, construction, marking, and general workmanship are as specified. Examination shall be in accordance with MIL-STD-883, Method 2009.

4.4 Group A Conformance

Group A conformance shall consist of the electrical parameters in the manufacturer's data sheet. If an inspection lot is made up of a collection of sublots, each sublot shall conform to Group A, as specified.

SUBGROUP	LTPD (%) LEVEL I 38510C	LEVEL II	LEVEL III 38510B	LEVEL IV 38510A
Subgroup 1 25°C, dc	5	7	5	5
Subgroup 2 High Temperature, dc	10	10	7	5
Subgroup 3 Low Temperature, dc	10	10	7	5
Subgroup 4	10	10	7	5
Dynamic and Switching Tests @ 25°C,				

NOTE: Functional tests included in D.C. tests.

4.5 Certification

The manufacturer shall include a certificate of compliance with each shipment of parts if requested on the purchase order. This certificate shall indicate that all specified tests and requirements of this specification have been made or met, and that the lot of devices (identified by lot and/or batch number) are acceptable. The certificate shall bear the name and signature of the manufacturer's Quality Control representative, the date of acceptance or signing, and any pertinent notes as applicable.

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4.6 Precap Lot Acceptance

After each precap inspection the lot of devices shall be sampled by quality control and inspected for the specified visual criteria. The sampling plan shall be:

40X criteria – 1.0% AQL
100X criteria – 1.0% AQL

TABLE I
MANUFACTURERS QUALIFICATION PROCEDURE

TEST	MIL-STD-883 METHOD	CONDITIONS	LTPD
Subgroup 1			
Physical Dimensions Visual and Mechanical	2008	Condition A & B	15
Subgroup 2[1]			
Solderability	2003		15
Subgroup 3[2]			
Thermal Shock	1011	Condition B	
Temperature Cycling	1010	Condition C	
Moisture Resistance	1004	Omit step 7B and Initial Conditioning	
Critical Electrical Parameters	5004	25°C, DC	15
Subgroup 4[2]			
Mechanical Shock	2002	Condition B	
Vibration Variable Freq.	2007	Condition A	
Constant Acceleration	2001	Condition E	
Critical Electrical Parameters	5004	25°C, DC	15
Subgroup 5[1]			
Lead Fatigue	2004	Condition B2	
Fine Leak	1014	Condition A, Per Para. 4.3.7 Herein	
Gross Leak	1014	Condition C, Per Para. 4.3.7 Herein	15
Subgroup 6[1]			
Salt Atmosphere	1009	Condition A, Omit Initial Conditioning	15
Subgroup 7[2]			
Storage Life	1008	150°C, 1000 Hrs. Minimum	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 8[2]			
Operating Life	1005	125°C, 1000 Hrs. Minimum Return to 25°C without bias	
Critical Electrical Parameters	5004	25°C, DC	10
Subgroup 9[1]			
Bond Strength			10 devices
a. Thermocompressions	2011	Condition B, D	not greater
b. Ultrasonic	2011	Condition B, D	than 1% defective

1. Visual and/or hermetic end points hence electrical or visual rejects may be used, Reference MIL-STD-883, Method 5005, Para. 3.4.
2. Electrical end points only.

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TABLE II
LOT ACCEPTANCE/PERIODIC QUALIFICATION TESTS
(GROUP B/GROUP C)

GROUP B

TEST	MIL-STD-883 METHOD	CONDITIONS	LEVEL IV 38510A	LTPD LEVEL III 38510B	LEVEL I[1] 38510C
Subgroup 1					
Physical Dimensions Visual and Mechanical	2008	Condition A	10	15	20
Subgroup 2					
Marking Permanency	2008	Condition B, para. 3.2.1			
Visual and Mechanical	2008	Condition B per applicable detail specification			
Bond Strength 3[2]	2011	Condition B or D 2 grams for Au bonds 1 gram for Al bonds	10	15	20
Subgroup 3[3]					
Solderability	2003		10	15	15
Subgroup 4[3]					
Lead Fatigue	2004	Conditions B2			
Fine Leak	1014	Conditions A or B, per para. 4.3.7 of this spec.			
Gross Leak	1014	Condition C, per para. 4.3.8 of this spec.	10	15	15

GROUP C

Subgroup 1[4]					
Thermal Shock	1011	Condition B			
Temp. Cycle	1010	Condition C			
Moisture Resistance	1004	Omit Initial Cond. & step 7B			
Critical Electrical Parameters	5004	25°C, DC	10	15	15
Subgroup 2[4]					
Mechanical Shock	2002	Condition B			
Vibration Variable Freq.	2007	Condition A			
Constant Acceleration	2001	Condition E			
Critical Electrical Parameters	5004	25°C, DC	10	15	15
Subgroup 3					
Salt Atmosphere	1009	Condition A Omit Initial Conditioning	10	15	15
Subgroup 4[4]					
High Temp. Storage	1008	150°C, 1000 Hrs.			
Critical Electrical Parameters	5004	25°C, DC	7	7	7
Subgroup 5[4]					
Operating Life Test	1005	125°C, 1000 Hrs. Minimum			
Critical Electrical Parameters		25°C, DC	5	5	5

1. Also applicable for Level II.
2. Bond strength test may be performed on samples randomly selected immediately following internal visual prior to sealing
3. See footnote 1 in Table I
4. See footnote 2 in Table I

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5.0 PREPARATION FOR DELIVERY

5.1 Final Visual Shipping Inspection

Each lot of microcircuits and its associated documentation shall be sampled by Quality Control and visually inspected for the following:

a) Scratched, nicked or bent leads

b) Damaged header (packages)

c) All test data specified in section 4.0

d) Certificate of Compliance as specified in section 4.0

e) All other pertinent documentation required and specified by this specification.

5.2 Packing Requirements

Parts shall be packed in containers of the type, size, and kind commonly used which will ensure acceptance by common carriers and safe delivery at the destination and in accordance with MIL-M-55565, Level C. The containers shall be clearly marked with manufacturer's name or symbol. The manufacturer's FEDERAL SUPPLY CODE FOR MANUFACTURER (FSCM) shall be included if applicable.

5.3 Preservation and Package Identification

The package shall be marked with the following:

The country of origin if other than U.S.A.

Procuring activity parts number

Purchase order number

Material nomenclature

Quantity

Lot number

Date code

This information shall appear on the label or shall be directly marked on each container. Method is optional.

TABLE III
CIRCUITS CURRENTLY APPLICABLE TO PRECAP INSPECTION PER PARAGRAPH 4.3.1.4

5481A	16-bit random-access memory
5484A	16-bit random-access memory
5488A	256-bit read-only memory
5489†	64-bit random-access memory
54143	4-bit counter/latch, seven-segment LED driver
54144	4-bit counter/latch, seven-segment lamp driver
54154	4-line-to-16-line decoder/demultiplexer
54166	8-bit parallel-load shift register
54170	4-by-4 register file
54184	BCD-to-binary converter
54185A	Binary-to-BCD converter
54186	512-bit programmable read-only memory
54187	1024-bit read-only memory
54198	8-bit parallel-in, parallel-out bidirectional shift register
54S200	256-bit read/write memory with three-state output
54S206	256-bit read/write memory with open-collector output
54284 54285	4-bit-by-4-bit parallel binary multipliers
74188A	256-bit programmable read-only memory
74200	256-bit read/write memory

†54 version to be announced.

6.0 NOTES

6.1 Precap Visual Method 2010.1

The following precap criteria may be in conflict with the circuit design topology and construction techniques of some microcircuit manufacturers. Where such a conflict does exist, the inspection criteria listed herein may be waived. (Reference paragraph 3.0 of MIL-STD-883, Method 2010.1)

6.1.1 Preseal Visual Inspection, Test Condition B [38510C and 38510C (Levels I and III)].

6.1.1.1 Paragraph 3.2.1.7(b) delete the 40 percent perimeter requirement (selected devices only).

6.1.1.2 Paragraph 3.2.4.3(a) substitute the following criteria: "Bonds placed so that the wire exiting from the bond appears to come closer than two wire diameters to another wire, bonding pad, or package land, after a distance of 10 mils from the die surface.

6.1.1.3 Paragraph 3.2.4.3(c) delete. (Applicable to gold ball bonds only) "Bond in the fillet area (or the point where metallizations exit from the bonding pad) which do not exhibit a line of undisturbed metallization visible between the periphery of the bond and at least one side of the fillet (or one side of the connecting stripe) when viewed from above."

6.1.1.4 Paragraphs 3.2.1.1 and 3.2.1.2 are clarified as follows: when a bimetallic system is used (e.g., moly-gold), the scratch or void must penetrate entirely through the gold and expose moly or oxide.

6.1.2 Preseal Visual Inspection, Level II and Table III MSI and LSI circuits.

The same comments of 6.1.1 are applicable here plus the following:

6.1.2.1 Paragraph 3.2.1.1 and 3.2.1.2 delete and replace with: "Scratches or voids in the metallized lead exposing oxide for more than 50% of the lead width or 0.5 mils, whichever is less. Excluded from this criteria are peripheral ground metallization which may contain the defect for a maximum of 50% of its width. Bonding pad scratches or voids are acceptable provided a metal path equal to 1/2 of the width of the connecting lead exists between the bond and the lead."

6.1.2.2 Paragraph 3.2.2 delete.

6.1.2.3 Paragraph 3.2.3 delete and replace with: "Any chip or crack that intersects or crosses active metallization. Excluded from this criteria are peripheral ground metallization which may contain the defect for a maximum of 50% of its width."

6.1.2.4 Paragraph 3.2.4.3(a) delete and replace with: "For all bonds, a minimum of 2 mils separation between the bond wire and other wires, metallization stripes and edge of die. For ultrasonic bonds, this criteria will apply after a distance of 10 mils from the die surface."

Paragraph 3.2.4.3(c) delete.

Paragraph 3.2.4.3(d) delete and replace with: Wire tails which exceed 2 mils in length at the pad or 4 mils in length at the post.

6.1.2.5 Paragraph 3.2.5(d) delete.

6.1.2.6 Paragraph 3.2.6.1 delete and replace with: "Attached bonding wire or ball inside cavity, or on bar which exceeds one mil in length dimension. All unattached metallic particles or silicon chips."

6.1.2.7 Paragraph 3.2.6.2(c) delete.

6.2 Interconnections

Circuit intraconnections (metallization pattern) shall be designed so that no properly fabricated connection shall experience a current density greater than 5×10^5 amperes/cm^2, including allowances for worst-case conductor composition, normal production tolerances on design dimensions, and nominal thickness at critical areas such as contact windows.

6.3 Burn-in Method 1015

The requirement to return the device to 25°C room ambient temperature with bias still applied should be omitted. Indications are that for most saturated logic integrated circuits, the high temperature bake after bias has been removed does not allow defective devices to recover and become good.

6.4 Salt Atmosphere Test, Method 1009

Where package design considerations necessitate (such as .75" tip-to-tip metal flat packs), there may be a conformal coating applied prior to the salt atmosphere test.

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JAN MIL-M-38510
Integrated Circuits

The Texas Instruments JAN MIL-M-38510 Program provides production availability of Hi-Rel JAN ICs. MIL-M-38510 and MIL-STD-883 have been fully implemented to provide a broad product line of JAN microcircuits for both military original equipment and logistic requirements. When the contract specifies that JAN ICs be used, or that microcircuits shall meet the quality provisions of MIL-M-38510, rely on the industry's broadest line of JAN ICs.

Table I provides a convient cross reference from the JAN part number to the corresponding standard catalog part numbers for ease in locating the commercial equivalent. The cross reference from the catalog numbers to the JAN slash sheet numbers is provided in Table II. The asterisks in Table I indicate the JAN types currently qualified, or planned for future qualification, by Texas Instruments in both Class B and Class C.

The following figure defines the reliability classes of MIL-M-38510 JAN ICs, and the intended areas of application. MIL-M-38510 recommends that for original equipment complements, the device class appropriate to the need be used, while Class B is recommended for spare parts for logistic support.

RECOMMENDED USE	TYPICAL SYSTEM APPLICATIONS	MIL-STD-883 MIL-M-38510 CLASS
Where repair or replacement is readily accomplished and "down time" is not critical	Prototype, noncritical ground systems	Class C
Where repair or replacement is difficult or impossible and reliability is vital	Avionics systems, space satellite	Class B
Where repair or replacement is difficult or impossible and reliability is imperative	Manned Space Program-NASA	Class A

JAN RECOMMENDED USAGE

When system designs utilize ICs not listed on the QPL, for which no slash sheets exist, the TI 38510/MACH IV Program may be used as the detail procurement specification. The 38510/MACH IV Program implements the processing and screening requirements of MIL-M-38510 and MIL-STD-883, and is intended as a supplement to the JAN slash sheets. For more information on the 38510/MACH IV Procurement Specification, see Tab Section 8.

The complete JAN part number with the tables of class, case, and lead finish codes are given in Table III, along with a cross reference to the TI 38510/MACH IV part numbers. A table of standard TI JAN-qualified cases and lead finishes is also provided to assist in specifying the proper JAN part number. It is imperative that the proper case and lead finish shown in the table be specified on the parts list and procurement documentation. The specific package for each device is determined by referring to the proper data sheet.

The following military documents (see Note 1) establish the processing, quality and reliability assurance requirements for JAN integrated circuits. The detail requirements of each individual JAN device are specified in the slash sheets.

MIL-M-38510/XXX, Microcircuits, Digital, TTL, . . . , . . . ,
Monolithic Silicon (Slash Sheets)
MIL-M-38510, Microcircuits, General Specification for
MIL-STD-883, Test Methods and Procedures for Microelectronics
QPL-38510, Qualified Products List for MIL-M-38510

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NOTE 1: Copies of these documents may be requested from the Naval Publications and Forms Center, 5801 Tabor Avenue, Philadelphia, Pa. 19120.

TABLE I. JAN INTEGRATED CIRCUITS AND TI CIRCUIT-TYPE CROSS-REFERENCE

JAN NO.	CIRCUIT TYPE	JAN NO.	CIRCUIT TYPE	JAN NO.	CIRCUIT TYPE
001-01	5430*	010-05	54145*	023-01	54H30*
001-02	5420*	010-06	5446*	023-02	54H20*
001-03	5410*	010-07	5447*	023-03	54H10*
001-04	5400*	010-08	5448*	023-04	54H00*
001-05	5404*	010-09	5449*	023-05	54H04*
001-06	5412*	011-01	54181*	023-06	54H01*
001-07	5401*	012-01	54121*	023-07	54H22*
001-08	5405*	012-02	54122*	024-01	54H40*
001-09	5403*	012-03	54123*	025-01†	54L90*
002-01	5472*	013-01	5492*	025-02†	54L93*
002-02	5473*	013-02	5493*	026-01	54L86*
002-03	54107*	013-03	54160*	027-01	54L02*
002-04	5476*	013-04	54163*	028-01	54L95*
002-05	5474*	013-05	54162*	028-02	54L164*
002-06	5470*	013-06	54161*	028-03†	93L28‡
002-07	5479‡	013-07†	5490*	029-01	54L42*
003-01	5440*	013-08†	54192*	029-02	54L43*
003-02	5437*	013-09†	54193*	029-03	54L44*
003-03	5438*	014-01	54150*	029-04	54L46*
004-01	5402*	014-02	54151*	029-05	54L47*
004-02	5423*	014-03	54153*	030-01†	15930
004-03	5425*	014-04	29309	030-02†	15935
004-04	5427*	014-05	54157	030-03†	15936
005-01	5450*	015-01†	5475*	030-04†	15946
005-02	5451*	015-02†	5477*	030-05†	15962
005-03	5453*	016-01†	5408*	040-01†	54H50
005-04	5454*	016-02†	5409*	040-02†	54H51
006-01	5482	020-01	54L30*	040-03†	54H53
006-02	5483*	020-02	54L20*	040-04†	54H54
007-01	5486*	020-03	54L10*	101-01	52741*
008-01	5406*	020-04	54L00*	101-02	52747*
008-02	5416*	020-05	54L04*	101-03	52101A*
008-03	5407*	020-06	54L03*	101-04	54108A
008-04	5417*	021-01	54L71*	102-01	52723*
009-01	5495*	021-02	54L72*	103-01	52710
009-02	5496	021-03	54L73*	103-02	52711*
009-03	54164*	021-04	54L78*	103-03	52106*
009-04	54165*	021-05	54L74*	103-04†	52111*
009-05†	54194*	022-01	54H72*	104-01†	55107*
009-06†	54195*	022-02	54H73*	104-02†	55108*
010-01	5442*	022-03	54H74*	105-01†	52733*
010-02	5443*	022-04†	54H76*	106-01†	52102
010-03	5444*	022-05†	54H101*	107-01†	52107*
010-04	5445*	022-06†	54H103*	201-01	54186*
				201-02	MCM5304‡

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.

* Devices for which TI is currently conducting qualification testing, or plans for future qualification.

† Slash sheets not released as of date of this publication.

‡ No TI equivalent; not recommended for new designs.

TABLE II. TI CIRCUIT-TYPE AND JAN INTEGRATED CIRCUITS CROSS-REFERENCE

CIRCUIT TYPE	JAN NO.	CIRCUIT TYPE	JAN NO.	CIRCUIT TYPE	JAN NO.
5400	001-04	5486	007-01	54H103	022-06
5401	001-07	5490	013-07	54L00	020-04
5402	004-01	5492	013-01	54L02	027-01
5403	001-09	5493	013-02	54L03	020-06
5404	001-05	5495	009-01	54L04	020-05
5405	001-08	5496	009-02	54L10	020-03
5406	008-01	54107	002-03	54L20	020-02
5407	008-03	54121	012-01	54L30	020-01
5408	016-01	54122	012-02	54L42	029-01
5409	016-02	54123	012-03	54L43	029-02
5410	001-03	54145	010-05	54L44	029-03
5412	001-06	54150	014-01	54L46	029-04
5416	008-02	54151	014-02	54L47	029-05
5417	008-04	54153	014-03	54L71	021-01
5420	001-02	54157	014-05	54L72	021-02
5423	004-02	54160	013-03	54L73	021-03
5425	004-03	54161	013-06	54L74	021-05
5427	004-04	54162	013-05	54L78	021-04
5430	001-01	54163	013-04	54L86	026-01
5437	003-02	54164	009-03	54L90	025-01
5438	003-03	54165	009-04	54L93	025-02
5440	003-01	54181	011-01	54L95	028-01
5442	010-01	54186	201-01	54L164	028-02
5443	010-02	54192	013-08	15930	030-01
5444	010-03	54193	013-09	15935	030-02
5445	010-04	54194	009-05	15936	030-03
5446	010-06	54195	009-06	15946	030-04
5447	010-07	54H00	023-04	15962	030-05
5448	010-08	54H01	023-06	29309	014-04
5449	010-09	54H04	023-05	52101A	101-03
5450	005-01	54H10	023-03	52102	106-01
5451	005-02	54H20	023-02	52106	103-03
5453	005-03	54H22	023-07	52107	107-01
5454	005-04	54H30	023-01	52108A	101-04
5470	002-06	54H40	024-01	52111	103-04
5472	002-01	54H50	040-01	52710	103-01
5473	002-02	54H51	040-02	52711	103-02
5474	002-05	54H53	040-03	52723	102-01
5475	015-01	54H54	040-04	52733	105-01
5476	002-04	54H72	022-01	52741	101-01
5477	015-02	54H73	022-02	52747	101-02
5479†	002-07	54H74	022-03	55107	104-01
5482	006-01	54H76	022-04	55108	104-02
5483	006-02	54H101	022-05	93L28†	028-03
				MCM5304†	201-02

NOTE: Only the basic JAN and SN numbers are shown. Complete the numbers as shown in Table III.

† No TI equivalent; not recommended for new design.

TABLE III. TI JAN AND 38510/MACH IV INTEGRATED CIRCUITS

TI 38510/MACH IV INTEGRATED CIRCUITS

JAN P/N → M38510 / 001 01 B C B

†38510/MACH IV P/N → SN C 5430 J 00

CLASS	
JAN	38510/ MACH IV
A	H (LEVEL IV)
B	C (LEVEL III)
C	M (LEVEL I)

CIRCUIT TYPE
See Cross Reference Table

CASE OUTLINE *			
JAN	PACKAGE	38510 (APP. C)	38510/ MACH IV
A	1/4" X 1/4" FLAT-14	F-1	U
B	1/4" X 1/8" FLAT-14	F-3	S/T
C	DIP-14	D-1	J
D	1/4" X 3/8" FLAT-14	F-2	W
E	DIP-16	D-2	J
F	1/4" X 3/8" FLAT-16	F-5	W
G	TO-99	A-1	L
H	1/4" X 1/4" FLAT-10	F-4	U
I	TO-100	A-2	L
J	3/8" X 5/8" FLAT-24	F-6	W
K	DIP-24	D-3	J

LEAD FINISH*		
JAN	TYPE	38510/ MACH IV
A	SOLDER DIP	10
B	TIN-PLATE	00
C	GOLD-PLATE	00

† Texas Instruments 38510/ MACH IV program is available as a supplement to JAN and where specific circuit types are not covered by JAN data sheets.

* JAN CASE OUTLINE & FINISH FOR TI FAMILIES

PRODUCT	A	B	C	D	E	F	G	H	I	J	K
SERIES 54			X	X	X	X				X	X
SERIES 54H			X	X	X	X					
SERIES 54L		X	X								
SERIES 52	X		X				X	X	X		
SERIES 55			X								
LEAD FINISH A											
LEAD FINISH B	X			X	X	X	X		X		X	X
LEAD FINISH C		X						X		X		

TEXAS INSTRUMENTS INCORPORATED

NOTES:
1. Only the basic circuit type number is shown. Complete by adding prefix for class, and suffixes for case outline and lead finish as shown above. Example: SNC5430J-00
2. Complete the JAN number by adding a three letter suffix for class, case outline, and lead finish as shown above. Example: M38510/001-01BCB

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